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A New Off-Board Electrical Vehicle Battery Charger: Topology, Analysis and Design

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Abstract: The extensive use of electric vehicles (EVs) can reduce concerns about climate change and fossil fuel shortages. One of the main obstacles to accepting EVs is the limitation of charging stations, which consists of high-charge batteries and high-energy charging infrastructure. A new transformer-less topology for boost dc-dc converters with higher power density and lower switch stress is proposed in this paper, which may be a suitable candidate for high-power fast-charging battery chargers of EVs. Throughout this paper, two operating modes of the proposed converter, continuous current mode (CCM) and discontinuous current mode (DCM), are analyzed in detail. Additionally, critical inductances and design considerations for the proposed converter are calculated. Finally, real-time verifications based on hardware-in-loop (HiL) simulation are carried out to assess the correctness of the proposed theoretical concepts.

Keywords: electric vehicle; battery charger; dc-dc converter; boost converter; off-board charger

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1. Introduction

Environmental considerations, the problem of air pollution, the reduction of fossil energy levels, and their cost are the most critical concerns facing governments [1,2]. The use of EVs can solve some of these problems. In some cases, these vehicles can inject electricity into the grid (vehicle-to-grid (V2G) technology) and thus play an essential role in decommissioning [3]. Battery chargers, the cable between vehicle and charger, feeder, material type and cost, connector, transformer, condition of the ground surface, and peak voltage control are among the challenges facing EVs [4,5]. Electric car battery charging systems can be divided into two groups: on-board and off-board [6]. On-board systems, which are themselves subdivided into subcategories of AC level 1 and AC level 2, are installed on electric cars. The ability to connect to the distribution power system directly, no need to build a charging station, and its cost are the advantages of this category. However, the need to install a battery charging system in each car, increasing the cost of the car production, low power, and duration time of battery charging are the disadvantages of this type of charging system. Charging of EVs in off-board systems is carried out by charging stations [7]. In other words, the equipment related to the charging section of EVs, except for the battery, is only at the charging station. Therefore, the cost of producing electric cars is reduced compared to on-board ones. On the other hand, the power density and efficiency are improved compared to on-board systems, and the charging time is significantly reduced. This type of electric vehicle charging system, also known as DC fast charger (level 3), is classified into two types: ac-connected and dc-connected [8]. In ac-connected systems, power is supplied from the grid by a transformer, and other equipment

is transferred to ac-bus by an ac/dc converter and a dc/dc converter for each output port. Ac-connected systems are categorized into two categories: extreme fast charging stations and grid-facing ac/dc converters. Dc-connected systems provide the required energy of dc-bus by a transformer and an ac/dc converter. In these systems, dc/dc converters offer the possibility of connecting EVs. In both systems, energy storage systems and renewable energy sources may be used in some applications. In general, dc-connected systems have high efficiency, simple control, and fewer conversion steps compared to ac-connected ones while ac-connected systems have more straightforward protection and more standard measuring equipment. Dc-connected systems are installed in two types: isolated and non-isolated. If the isolation of the charging system is provided by the transformers before the ac/dc converter, it can use non-isolated converters. Although the bidirectional non-isolated boost converters have higher efficiency and easier control systems than most unidirectional non-isolated converters, the simple structure in unidirectional converters has driven research. For EV charging applications, depending on the battery voltage, a unidirectional boost converter can be a suitable and straightforward choice. The power of this type of converter is limited via the current passing through the switches and the inductor size for low current ripple. Various techniques have been introduced to increase the capability of this type of converter.

One of the essential techniques for this type of converter is the switched-capacitor (SC) technique [9,10]. In the SC technique, adequate voltage gains, high density, and higher efficiency are provided for this technique. However, the stresses among the semiconductors have limited its use. The interleaving technique is also one of the other techniques introduced. In this technique, several converters can be located in series-parallel to each other to provide more suitable conditions on the output side [11,12]. In [11], an interleaved boost dc-dc converter with three-phase legs is introduced. Simple structure, convenient performance, and high power density are its advantages. In [13], the proposed converter in [11] was extended to six phase legs. In [14], a three-phase interleaved boost converter under discontinuous current mode (DCM) has been designed while its small inductor size causes the ability to change the direction of the inductor current and provides zero-voltage switching conditions. In [15], an interleaved boost converter in DCM utilized partial power concepts, and low voltage rates for switches and reduced losses are introduced. The drawback of this structure is the need for a lot of hardware equipment and inner dc-bus balancing. The voltage-lift technique is another popular method for non-isolated boost converters [16,17]. In this technique, the voltage is increased step by step, using the energy storage feature in the inductor and capacitor. Losses of semiconductor elements are the most critical drawback of this technique.

In this paper, a new topology for a non-isolated boost dc-dc converter is proposed for the EV charger. First, the topology of the proposed converter is analyzed in detail. Next, the critical inductances are calculated to determine its operating condition, especially for designing for DCM operating as in [15]. Then, the designing considerations are carried out for choosing better switches, and a comparison between some literature is presented. Real-time examinations are presented to verify the theoretical concepts. Finally, some concluding remarks are given.

2. The Proposed Converter Topology Analysis

The proposed converter topology is shown in Figure 1. As observed from this figure, the proposed structure consists of two power electronic switches, two inductors, three capacitors, and three diodes. The switching of the proposed topology is carried out by the PWM technique, where their turning on/off switches are complementary. High voltage gain and high-frequency transformer-less are the proposed topology's advantages, whereas its hard switching condition are the main drawback. The proposed converter voltage gain is carried out using the energy storage (inductors and capacitors) element feature. To simplify the analysis, it is assumed that: (a) the converter is in steady state, so the output voltage V_o is constant, (b) the capacitors are large enough and therefore their voltage in each

switching period remains unchanged, (c) all switches and diodes are ideal, (d) equivalent series resistance(ESR) ESR is neglected, and (e) the isolation of the system is carried out before the converter. In the following, equations of the current and voltage of each element in CCM and DCM are discussed.

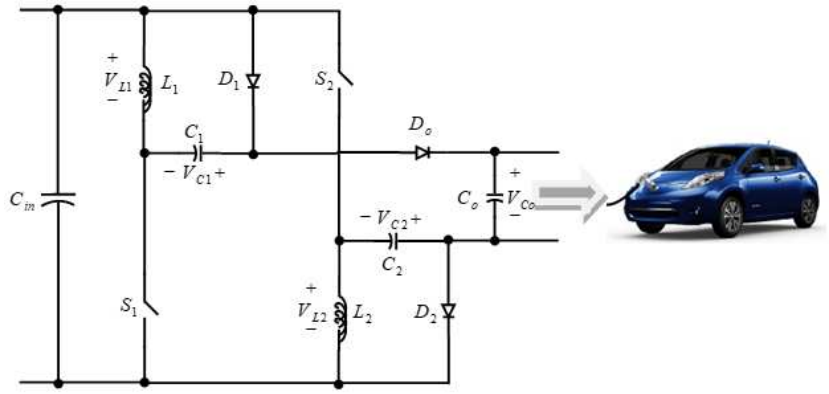

Figure 1. The proposed topology for the boost dc-dc converter.

2.1. Analysis of the Proposed Converter in CCM

In the time interval of T_{on}, the switch of S_1 is turned on and the switch of S_2 is turned off. Then, the inductor L_1 is connected to the input voltage source (V_i) and its through pass current is increased to its maximum value (I_{LP1}) from its minimum value (I_{LV1}). During this time interval, the diode of D_2 is reversely biased and the diodes D_1 and D_o are forward biased. In this time interval, the stored energy of the inductor L_2 is decreased to its minimum value (I_{LV2}) from its maximum value (I_{LP2}). The equivalent circuit of the proposed topology is shown in Figure 2a.

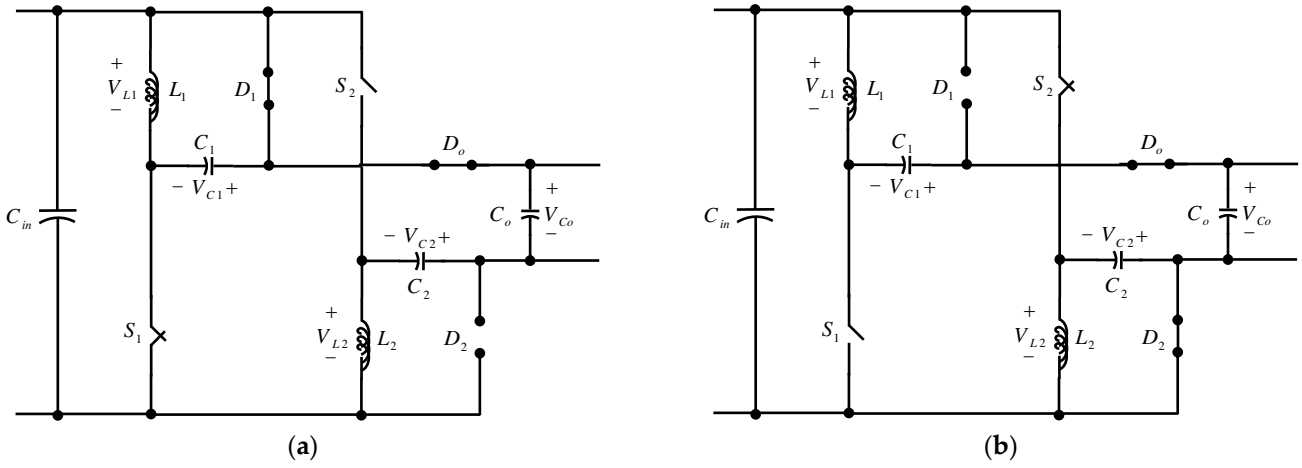

Figure 2. The equivalent circuit of the proposed topology in CCM; (**a**) at T_{on}, (**b**) at T_{off}.

This time interval of T_{off} begins when the switch of S_1 is turned off and the switch of S_2 is turned on. In this situation, the diodes of D_2 and D_o are turned on and the diode of D_1 is turned off. So, the inductor L_2 is connected to V_i; therefore, its stored energy is increased. Additionally, the stored energy of the capacitor C_o is increased, then it is charged. The equivalent circuit of the proposed topology is shown in Figure 2b. Some key waveforms of the proposed topology in CCM are illustrated in Figure 3a.

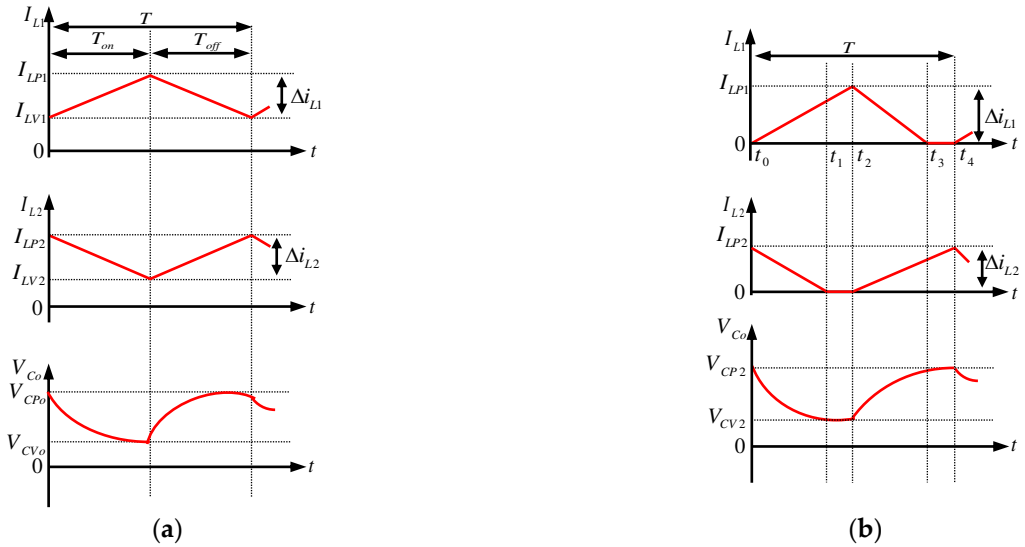

Figure 3. Some key waveforms of the proposed topology; (**a**) at CCM, (**b**) at DCM.

Here, some critical relations of the proposed converter are illustrated. The first index shows the component number and second part is used for time intervals, whereas 1 and 2 show T_{on} and T_{off} in CCM, respectively, and 1, 2, 3, and 4 show (t_0, t_1), (t_1, t_2), (t_2, t_3), and (t_3, t_4) at DCM, respectively.

By applying the Kirchhoff voltage law (KVL) to the circuit of Figure 2a, the following equation is obtained:

$$V_{L1,1} = V_i = L_1 \frac{di_{L1,1}}{dt}, \tag{1}$$

Additionally, the equation below can be determined by Figure 2b:

$$V_{L1,2} = V_{C1} = L_1 \frac{di_{L1,2}}{dt}, \tag{2}$$

The equation below is also written for the inductor L_2:

$$V_{L2,1} = -V_{C2,1} = L_2 \frac{di_{L2,1}}{dt}, \tag{3}$$

$$V_{L2,2} = V_i = L_2 \frac{di_{L2,2}}{dt}, \tag{4}$$

By considering $T = T_{on} + T_{off}$ and $D = T_{on}/T$, the voltage gain of the proposed converter in CCM can be extracted by substitution (1) and (2) into voltage balance law for on inductor as follows:

$$\frac{V_o}{V_i} = \frac{2 - D}{1 - D}, \tag{5}$$

Finally, D is obtained from (5) as follows:

$$D = \frac{2V_i - V_o}{V_i - V_o}, \tag{6}$$

The voltage and current relation of semiconductors and current ripples of inductors in CCM are shown in Table 1.

Table 1. Comparison between proposed converter and the existing topologies.

Elements/Time Interval	CCM		DCM			
	T_{on}	T_{off}	t_0-t_1	t_1-t_2	t_2-t_3	t_3-t_4
D_1	$i_{C1}+I_o+i_{Co}$	$V_{L1}-V_{C1}$	$i_{C1}+I_o+i_{Co}$	$i_{C1}+I_o+i_{Co}$	$V_{L1}-V_{C1}$	$i_{C1}+I_o+i_{Co}$
D_2	$V_{L2}+V_{C2}$	$I_o+i_{Co}-i_{C2}$	$V_{L2}+V_{C2}$	$I_o+i_{Co}-i_{C2}$	$I_o+i_{Co}-i_{C2}$	$I_o+i_{Co}-i_{C2}$
D_o	I_o+i_{Co}		I_o+i_{Co}	V_i-V_o	I_o+i_{Co}	V_i-V_o
S_1	$i_{L1}+i_{C1}$	V_i-V_{L1}	$i_{L1}+i_{C1}$		V_i-V_{L1}	V_i
S_2	V_i-V_{L2}	I_i-i_{L1}	V_i-V_{L2}	V_i	I_i-i_{L1}	I_i-i_{D1}
Δi_{L1}	$\left\lvert\frac{V_i}{L_1}T_{on}\right\rvert=\left\lvert-\frac{V_{C1}}{L_1}T_{off}\right\rvert$		$\left\lvert\frac{V_i}{L_1}\Delta t\right\rvert=\left\lvert-\frac{V_i+V_{C1,3}-V_o}{L_1}\Delta t\right\rvert$			
Δi_{L2}	$\left\lvert\frac{V_{C2,1}}{L_2}T_{on}\right\rvert=\left\lvert\frac{V_i}{L_2}T_{off}\right\rvert$		$\left\lvert-\frac{V_i+V_{C2,1}-V_o}{L_2}\Delta t\right\rvert=\left\lvert\frac{V_i}{L_2}\Delta t\right\rvert$			

2.2. Analysis of the Proposed Converter in DCM

At (t_0, t_1), the switch S_1 is turned on and the switch S_2 is turned off. Additionally, the diodes D_1 and D_o are on and the diode D_2 is off. Then, the inductor L_1 is connected to V_i and its stored energy is increased. Another side, the inductor L_2 is the load path, and its stored energy is decreased. Therefore, the inductor current is reached to the minimum value. The equivalent circuit of the proposed topology is shown in Figure 4a.

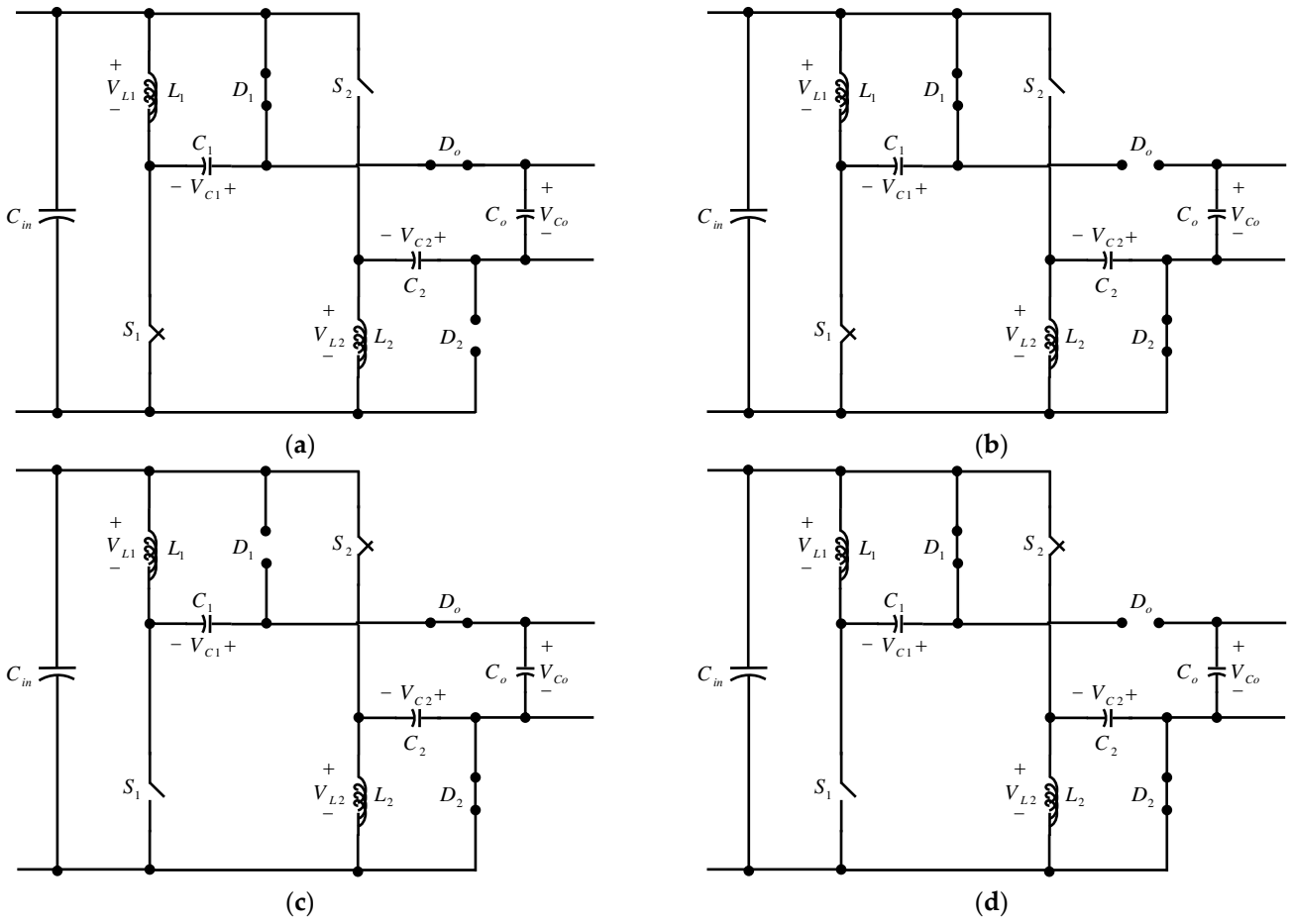

Figure 4. The equivalent circuit of the proposed topology in DCM; (**a**) at (t_0, t_1), (**b**) at (t_1, t_2), (**c**) at (t_2, t_3), (**d**) at (t_3, t_4).

The time interval of (t_1, t_2) begins when the diode D_o is turned off, whereas the switch S_1 is turned on and the switch S_2 is turned off. In this condition, the diode D_2 is on. So,

the discharge current of the capacitor C_o provides the load current and its stored energy is decreased. The equivalent circuit of the proposed topology is shown in Figure 4b.

At (t_2, t_3), the switch S_1 is turned off and the switch S_2 is turned on. Additionally, the diodes D_2 and D_o are on and the diode D_1 is off. Then, the inductor L_2 is connected to V_i and its stored energy is increased. The store energy of the inductor L_1 is decreased due to its location at the load path. Therefore, the current thorough pass L_1 is reached to its minimum value. The equivalent circuit of the proposed topology is shown in Figure 4c.

At (t_3, t_4), the switch S_1 is still turned off and the switch S_2 is turned on. Meanwhile, the diode D_2 is on, whereas the diode of D_o is turned off and the diode D_1 is turned on. During this time interval, the inductor L_2 is connected to V_i and is charged. Additionally, the load current is provided by the capacitor C_o. The equivalent circuit of the proposed topology is shown in Figure 4d. Figure 3b shows some key waveforms of the proposed topology in DCM.

By applying KVL on Figure 4a,b, we have:

$$V_{L1,2} = V_i = L_1 \frac{di_{L1,2}}{dt}, \tag{7}$$

Additionally, the following equation can be written for the inductor L_1:

$$V_{L1,3} = V_i + V_{C1,3} - V_o = L_1 \frac{di_{L1,3}}{dt}, \tag{8}$$

$$V_{L1,4} = 0, \tag{9}$$

From Figure 4, the equation below also results for the inductor L_2:

$$V_{L2,1} = V_i + V_{C2,1} - V_o = L_2 \frac{di_{L1,1}}{dt}, \tag{10}$$

$$V_{L2,2} = 0, \tag{11}$$

$$V_{L2,4} = V_i = L_2 \frac{di_{L2,4}}{dt}, \tag{12}$$

By applying the voltage balance law for the inductor L_2 and replacing (7) to (9) into it, and considering $D = (t_0, t_2)/T$ as the duty cycle in DCM, the voltage gain of the proposed converter in DCM is calculated as follows:

$$\frac{V_o}{V_i} = 1 + \sqrt{1 + \frac{D^2 R}{Lf}}, \tag{13}$$

Therefore, one obtains that:

$$D = \sqrt{\frac{V_o(2V_i - V_o)Lf}{RV_i^2}}, \tag{14}$$

Table 1 shows the voltage and current of the semiconductors and the ripple current of the inductors in this operating mode briefly.

3. Critical Inductance Calculation

In a dc-dc converter, the CCM and DCM are determined based on the values of the inductors, and the critical inductance determines the boundary between the CCM and DCM. If the inductance value of the inductors is greater than the critical inductance value, the converter will operate in CCM, and if the inductance value of the inductors is less than the critical inductance value, the converter will operate in DCM.

By replacing critical conditions into (7), the following equation is obtained:

$$I_{LP1} = \frac{V_i}{L_1} DT + I_{LV1}, \tag{15}$$

The equation below can be written for the capacitor:

$$\frac{1}{T}\int_0^T i_{Co} dt = 0, \tag{16}$$

The current of the capacitor C_o is equal to:

$$i_{Co,1} = -I_o, \tag{17}$$

$$i_{Co,2} = i_{L1,2} - I_o, \tag{18}$$

Assuming a new time-off set for T_{off}, the current of the inductor L_1 is equal to the following:

$$i_{L1,2} = \frac{2V_i - V_o}{2L} t + I_{LP1}, \tag{19}$$

By replacing (18) and (17) into (16) and considering (19), the equation below is resulted:

$$I_{LP1} = \frac{I_o}{1-D} + \frac{V_o - 2V_i}{4Lf}(1-D), \tag{20}$$

The above equation can be written as:

$$I_{LP1} = I_o \left[\frac{1}{1-D} + \frac{D(1-D)R}{2Lf(2-D)} \right], \tag{21}$$

Substitution of the above relation into (15) yields to:

$$I_{LV1} = I_o \left[\frac{1}{1-D} - \frac{D(1-D)R}{2Lf(2-D)} \right], \tag{22}$$

The critical inductance of L_1 can be extracted form (22) as follows:

$$L_{C1} = \frac{V_i^2 (V_o - 2V_i) R}{V_o (V_o - V_i)^2 f}, \tag{23}$$

Assuming $L_1 = L_2$, we have:

$$L_{C2} = L_{C1}, \tag{24}$$

4. Design Considerations

The peak current flow switch (PCFS) plays a vital role in designing and selecting the type of switch, and finally, the converter price, and it can be minimized by proper selection of the inductor values. Next, the peak current of switches are extracted in CCM and DCM.

4.1. Switches Current in CCM

According to Figure 2a,b, the peak current passing through the switches are equal to:

$$i_{SP1} = I_{LP1} + i_{C1}, \tag{25}$$

$$i_{SP2} = I_{LP2} + i_{C2}, \tag{26}$$

By considering (21) and assuming $L_1 = L_2$, it has resulted:

$$i_{SP1} = i_{SP2} = I_o \left[\frac{1}{1-D} + \frac{D(1-D)R}{2Lf(2-D)} \right] + i_{C1}, \tag{27}$$

By considering $L_1 = L_{C1}$ and $L_2 = L_{C2}$ into (27), the maximum peak current of the switches are determined as follows:

$$i_{SP1,\max}^{CCM} = i_{SP2,\max}^{CCM} = \frac{V_o(V_o - V_i)}{2RV_i} + \frac{V_i(V_o - 2V_i)}{2Lf(V_o - V_i)} + i_{C1}, \tag{28}$$

From the above equation, it can be concluded that the peak current passing through the switches depends on the values of D, L and R. Additionally, the maximum peak current of switches can be selected for $L_1 = L_{C1}$ and $L_2 = L_{C2}$.

4.2. Switches Current in DCM

According to Figure 5, PCFSs are obtained as follows:

$$i_{SP1}^{DCM} = i_{SP2}^{DCM} = \frac{V_i D}{2L_1 f}, \tag{29}$$

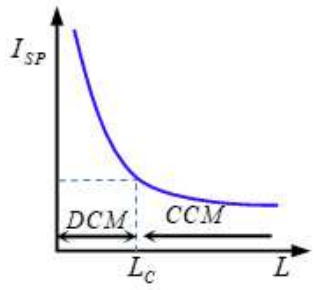

Figure 5. The relation between the value of the inductances and PCFS.

By replacing (22) into the above relation, PCFSs are rewritten as follows:

$$i_{SP1,\min}^{DCM} = i_{SP2,\min}^{DCM} = \sqrt{\frac{V_o(2V_i - V_o)}{L_1 Rf}}, \tag{30}$$

From the above relation, it can be seen that the minimum PCFSs in DCM also have an inverse relation with D, R and inductors values and they are obtained by considering $L_1 = L_{C1}$ and $L_2 = L_{C2}$. The maximum PCFSs are obtained for $L_1 < L_{C1}$ and $L_2 < L_{C2}$. Figure 5 shows the relative between the peak current of switches and inductors values. It is obvious that the peak current of switches in DCM is higher than CCM ones.

Comparing (28) and (30), it has resulted:

$$i_{SP1,\min}^{DCM} = i_{SP2,\max}^{CCM} = i_{SP2,\min}^{DCM} = i_{SP2,\max}^{CCM}, \tag{31}$$

4.3. Switches Voltage Stress

From Figures 2 and 4, the voltage stress of switched-off can be calculated as follows:

$$V_{S1} = V_i - V_{C1}, \tag{32}$$

$$V_{S2} = V_i + V_{C2} \tag{33}$$

5. Efficiency Analysis

Neglecting of the inductors current ripple and the capacitors voltage ripple, the root-mean-square (RMS) current relations of inductors is given as follows:

$$I_{L1} = I_{L2} = \frac{1-D}{2-D} I_i, \tag{34}$$

Thus, the inductors losses are obtained as follows:

$$P_{L1} = r_{L1} I_{L1}^2 + (K f^{\alpha} B_{ac}^{\beta} W_{tfe})(10^{-3}), \tag{35}$$

$$P_{L2} = r_{L2} I_{L2}^2 + (K f^{\alpha} B_{ac}^{\beta} W_{tfe})(10^{-3}), \tag{36}$$

The diodes RMS current relations are calculated as follows:

$$I_{D1} = \sqrt{\frac{1}{T} \int_0^{DT} \left(\frac{3-D}{2(2-D)} I_i \right)^2 dt} = \frac{3-D}{2(2-D)} I_i \sqrt{D}, \tag{37}$$

$$I_{D2} = \sqrt{\frac{1}{T} \int_0^{(1-D)T} \left(\frac{3-D}{2(2-D)} I_i \right)^2 dt} = \frac{3-D}{2(2-D)} I_i \sqrt{1-D}, \tag{38}$$

$$I_{Do} = I_{Co} + I_o \approx \frac{1-D}{2-D} \frac{I_i}{3}, \tag{39}$$

After neglecting turn off state losses in the diodes and defining Q_{rr} as reverse recovery energy of diode, the diode losses are as follows:

$$P_{D1} = V_F I_{D1,ave} + r_D I_{D1}^2 + 0.25 Q_{rr} V_D f, \tag{40}$$

$$P_{D2} = V_F I_{D2,ave} + r_D I_{D2}^2 + 0.25 Q_{rr} V_D f, \tag{41}$$

$$P_{Do} = V_F I_{Do,ave} + r_D I_{Do}^2 + 0.25 Q_{rr} V_D f, \tag{42}$$

The RMS current values of C_1 and C_2 are obtained as follows:

$$\begin{aligned} I_{C1} &= \sqrt{\frac{1}{T} \left[\int_0^{DT} \left(\frac{3-D}{2(2-D)} I_i \right)^2 dt + \int_0^{(1-D)T} \left(\frac{1-D}{2(2-D)} I_i \right)^2 dt \right]} \\ &= I_i \left[\frac{3-D}{2(2-D)} \sqrt{D} + \frac{1-D}{2(2-D)} \sqrt{1-D} \right] \end{aligned} \tag{43}$$

$$\begin{aligned} I_{C2} &= \sqrt{\frac{1}{T} \left[\int_0^{DT} \left(\frac{1-D}{2(2-D)} I_i \right)^2 dt + \int_0^{(1-D)T} \left(\frac{3-D}{2(2-D)} I_i \right)^2 dt \right]} \\ &= I_i \left[\frac{1-D}{2(2-D)} \sqrt{D} + \frac{3-D}{2(2-D)} \sqrt{1-D} \right] \end{aligned} \tag{44}$$

Considering $Q_{Co}^{+} = Q_{Co}^{-}$, the RMS value of capacitor C_o current is as follows:

$$I_{Co} = \sqrt{\frac{1}{T} \left[\int_0^{DT} \left(\frac{1-D}{2-D} \frac{I_i}{6} \right)^2 dt + \int_0^{(1-D)T} \left(-\frac{1-D}{2-D} \frac{I_i}{6} \right)^2 dt \right]} = \frac{1-D}{2-D} \frac{I_i}{6}, \tag{45}$$

The capacitors losses are obtained as follows:

$$P_{C1} = r_{C1} I_{C1}^2, \tag{46}$$

$$P_{C2} = r_{C2} I_{C2}^2, \tag{47}$$

$$P_{Co} = r_{Co} I_{Co}^2 \tag{48}$$

The switches RMS current and their losses are equal to:

$$I_{S1} = \sqrt{\frac{1}{T}\int_0^{DT} \left(\frac{5-2D}{3(2-D)} I_i\right)^2 dt} = \frac{5-2D}{3(2-D)} I_i \sqrt{D}, \tag{49}$$

$$I_{S2} = \sqrt{\frac{1}{T}\int_0^{(1-D)T} \left(\frac{5-2D}{3(2-D)} I_i\right)^2 dt} = \frac{5-2D}{3(2-D)} I_i \sqrt{1-D}, \tag{50}$$

$$P_{S1} = r_{DS-on} I_{S1}^2 + 0.5(t_r + t_f) I_{S1,ave} V_{S1} f + 0.5 C_{OSS} V_{S1}^2 f + 0.25 f Q_{rr,BD} V_{S1} + r_{BD1,} I_{BD1}^2 + V_{BF1} I_{BD1,ave}, \tag{51}$$

$$P_{S2} = r_{DS-on} I_{S2}^2 + 0.5(t_r + t_f) I_{S2,ave} V_{S2} f + 0.5 C_{OSS} V_{S2}^2 f + 0.25 f Q_{rr,BD} V_{S2} + r_{BD2,} I_{BD2}^2 + V_{BF2} I_{BD2,ave}, \tag{52}$$

Thus, the total loss and efficiency are equal to:

$$P_{Loss} = P_{L1} + P_{L2} + P_{S1} + P_{S2} + P_{C1} + P_{C2} + P_{Co} + P_{D1} + P_{D2} + P_{Do}, \tag{53}$$

$$\eta\% = \frac{P_{out}}{P_{out} + P_{Loss}} \times 100, \tag{54}$$

6. Comparison

The comparison results of different converters avilable in the literature and the proposed converter are presented in Table 2. As shown in Table 2, the comparison is made in terms of the number of active and passive elements and the voltage gain in CCM. In terms of the number of active elements, the proposed converter topology has more switches than the ones proposed in [16] and [17]. Moreover, the proposed converter has fewer diodes than the topology in [18–20], and has the same number of diodes as the ones in [9,10,16,17]. Although the number of inductors of the proposed converter is less than [9,17], its number is equal to [10,16,18–20]. As a result, the size of the proposed converter may be smaller than the others. In terms of the number of capacitors, the proposed converter has the same number of capacitors compared to [9,16], and has less than [17,19], and more than [10,18].

Table 2. Comparison between proposed converter and the existing topologies.

Elements/Ref.	[9]	[10]	[16]	[18]	[19]	[20]	[17]	Proposed
Switch	2	2	1	2	2	2	1	2
Inductor	3	2	2	2	2	2	4	2
Capacitor	3	2	3	2	4	4	6	3
Diode	2	3	3	4	4	5	3	3
Voltage gain in CCM	$\frac{1+3D}{1-D}$	$\frac{1}{D(1-D)}$	$\frac{1+D}{1-D}$	$\frac{1+D}{D(1-D)}$	$\frac{4}{1-D}$	$\frac{4}{1-D}$	$\frac{3D}{1-D}$	$\frac{2-D}{1-D}$
Max. Nor. voltage of switch	$\frac{M+3}{2M}$	1	$\frac{M+1}{2}$	$\frac{2M+2}{3M}$	$\frac{M}{4}$	$\frac{M}{4}$	$\frac{M+3}{3M}$	$\frac{3M-4}{2M-3}$
Max. Nor. voltage of diode	$\frac{M+3}{2M}$	$\frac{\frac{3}{2}+}{\sqrt{\frac{1}{4}-\frac{1}{M}}}$	$\frac{M+1}{2}$	$\frac{1+}{\sqrt{M+2}}$	$\frac{M}{2}$	$\frac{M}{2}$	$\frac{M+3}{3M}$	$\frac{M-1}{3}$

Figure 6a,b show the changes in the maximum normalized voltage stress of the switch and the maximum normalized voltage stress of the diode, respectively. Except for [10], which has a fixed graph in both analyzes, the values of the maximum normalized voltage stress of the switch and the maximum normalized voltage stress of the diode change varied for different amounts of voltage gain (M). From Figure 6a, the maximum normalized

voltage stress of the switch in the proposed converter is almost equal to [9], while compared to [10,16,18–20], the value of the maximum normalized voltage stress of the switch is lower. It is worth noting that the maximum normalized voltage stress of the switch in the proposed converter is more than [17]. The maximum normalized voltage stress of the diode at lower yields is better than the converters studied (see Figure 6b). The maximum normalized voltage stress of the diode in the proposed converter is better than [16,18–20], while the value of this parameter is higher compared to [9,10,17].

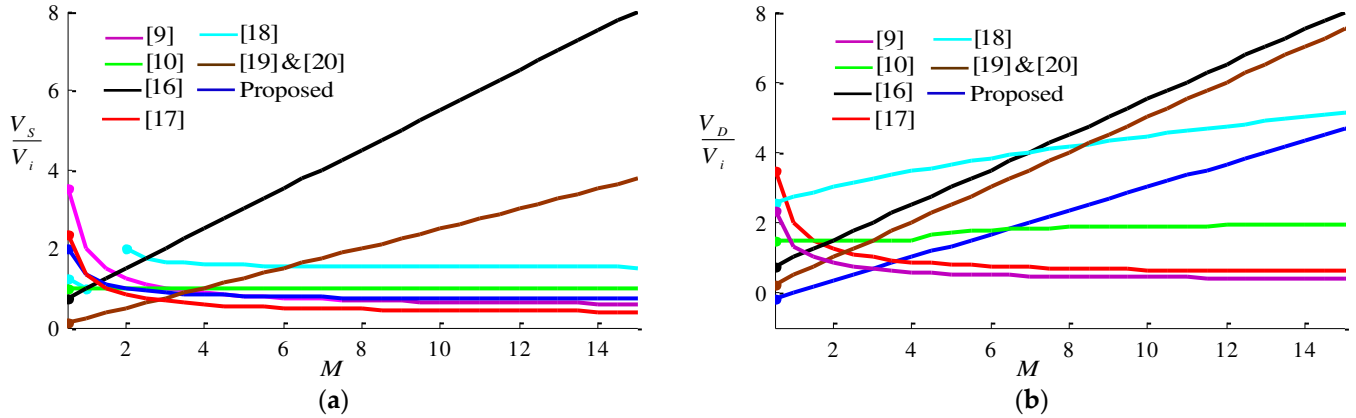

Figure 6. The maximum normalized voltage stress for (**a**) switch and (**b**) diode.

7. Experimental Results

Assuming that the switches and diodes are ideal and considering the parameters presented in Table 3, the correctness of the stated theoretical concepts and relations are examined. Based on the suggested converter topology described in Section 2, a hardware-in-loop (HiL) simulating setup is configured based on the OPAL-RT real-time simulator as depicted in Figure 7. Since the HiL is developed in a real-time platform, this simulation is a more practical validation setup than an off-line MATLAB simulation for the verification of system responses to unusual events. First, the operating of the proposed converter in critical condition is carried out. Then, CCM and DCM results are recorded for the proposed converter. It should be noted that the recorded time period of the results shown is selected to show the performance of the converter in steady-state.

Table 3. Parameters for the proposed converter topology.

Parameters	CCM	DCM
Duty cycle	$D = 50\%$	$D' = 50\%$
R	100 Ω	100 Ω
$L_1 = L_2$	1 mH	70 μH
$C_1 = C_2$	47 μF	47 μF
C_o	100 μF	100 μF
V_i,	70 V, 33.5 kHz	70 V, 33.5 kHz

Figure 7. Photograph of the OPAL-RT setup adopted for the HiL verification.

To analyze the performance of the proposed dc-dc boost converter, the operating mode of the converter must first be determined. According to (23) and Table 3, the value of critical inductances for L_1 and L_2 are equal to 256 µH. If $L_1 = L_2 > L_{C1} = L_{C2}$, the converter will be in CCM; otherwise, it will be in DCM. The operation of the proposed converter will be in critical mode for $L_1 = L_2 = L_{C1} = L_{C2}$. The experimental results are recorded by choosing $L_1 = L_2 = L_{C1} = L_{C2} = 256$ µH. The switch's current waveforms are illustrated in Figure 8a,b. As one can observe from these figures, the maximum peak current of switches is 15 A. Additionally, the output voltage in this mode is equal to 209 V.

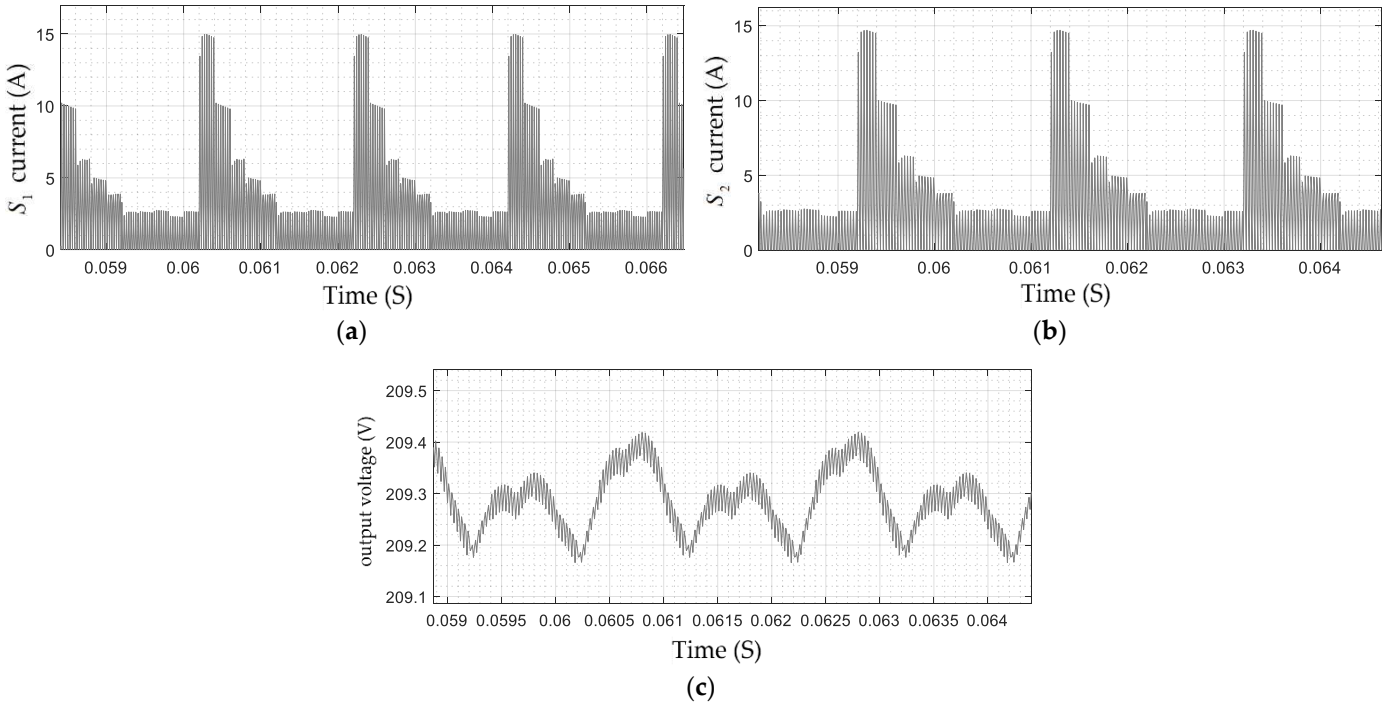

Figure 8. The results in critical mode, (**a**) S_1 current, (**b**) S_2 current, and (**c**) output voltage.

Figure 9 shows the experimental results in CCM. As shown in Figure 9a,b, the maximum peak current of the inductors is 2.7 A; hence, the inductor size can be reduced. It can be noted that $\Delta i_{L1} = \Delta i_{L2} = 1$ A. The switches' current waveforms are shown in

Figure 9c,d, while their maximum values are 13 A according to (25) to (28). The output voltage is almost equal to 209 V, reconfirming the theoretical calculation (see Figure 9e).

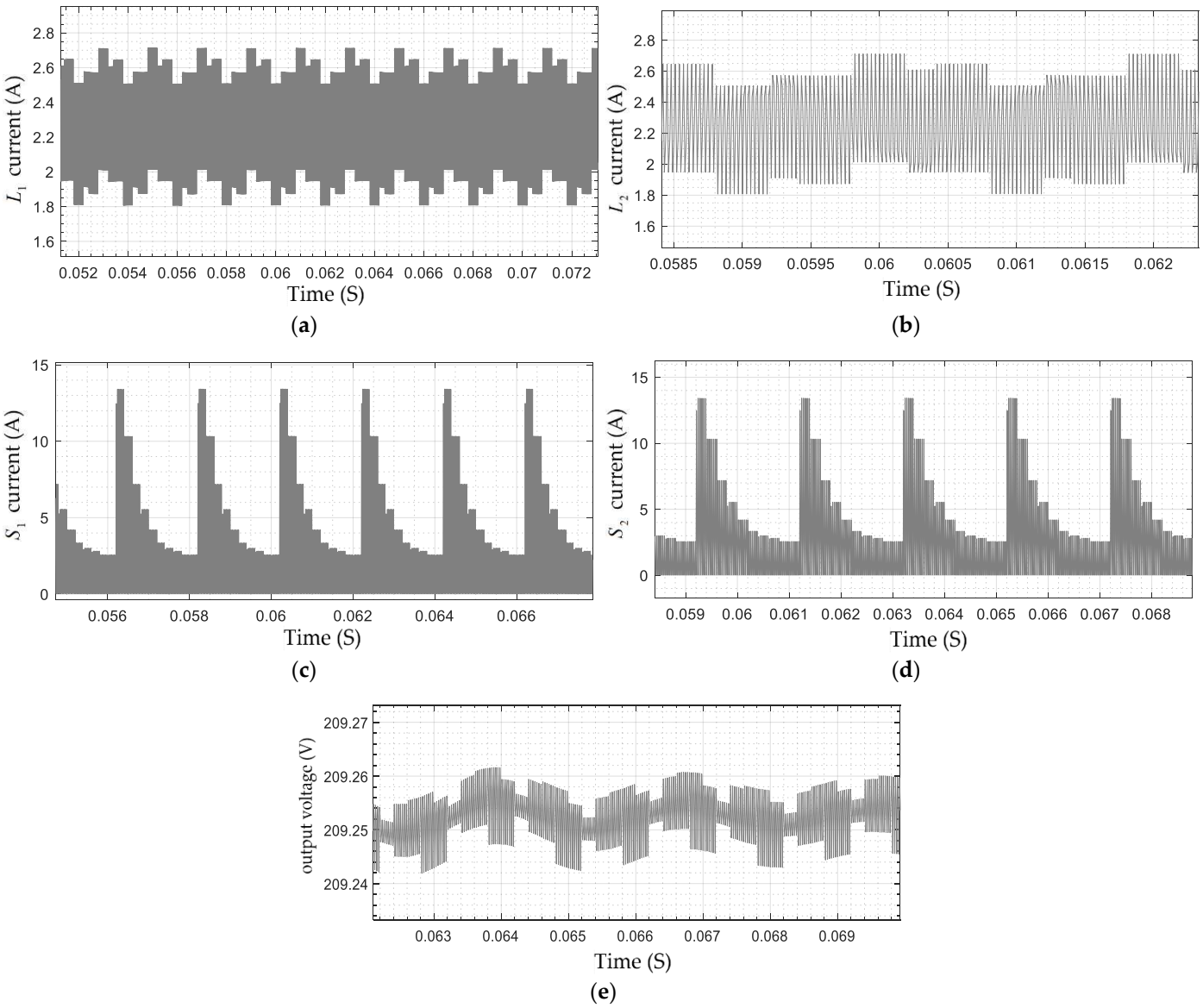

Figure 9. The results in CCM, (**a**) L_1 current, (**b**) L_2 current, (**c**) S_1 current, (**d**) S_2 current, and (**e**) output voltage.

Considering the presented parameters in Table 3 into (34) and (52), powder core inductor ($r_{L1} = r_{L2} = 0.08\ \Omega; K = 0.00551; \alpha = 1.23; \beta = 2.12; W_{tfe} = 34.6; B_{ac} = 0.0527$), electrolytic capacitor ($r_{C1} = r_{C2} = 0.015\ \Omega; r_{Co} = 0.02\ \Omega$), N-channel MOSFET (Type :STW45NM50F; $r_{DS-on} = 0.07\ \Omega; t_r = 28$ nS; $t_f = 25$ nS; $C_{OSS} = 1260$ pF; $Q_{rr} = 1600$ nC; $di/dt = 100$ A/μS), diodes (Type :MUR1560; $V_{F,D} = 0.8$ V; $r_D = 0.01\ \Omega$) and neglecting from the third term of the diodes losses relations and fifth and sixth term of switch losses relations yields $P_{L1} = P_{L2} = 0.72$ W, $P_{D1} = P_{D2} = 6.3$ W, $P_{Do} = 0.816$ W, $P_{C1} = P_{C2} = 1.6$ W, $P_{Co} = 0.01$ W and $P_{S1} = P_{S2} = 6.0543$ W. Thus, the calculated efficiency is 93.1%.

The results in DCM are depicted in Figure 10. The inductors' currents are illustrated in Figure 10a,b. As shown in these figures, their variation proves the theorical relations and their maximum values are 14 A. The switch current also reached 17 A (see Figure 10c–e shows the output voltage value, which is equal to 295 V.

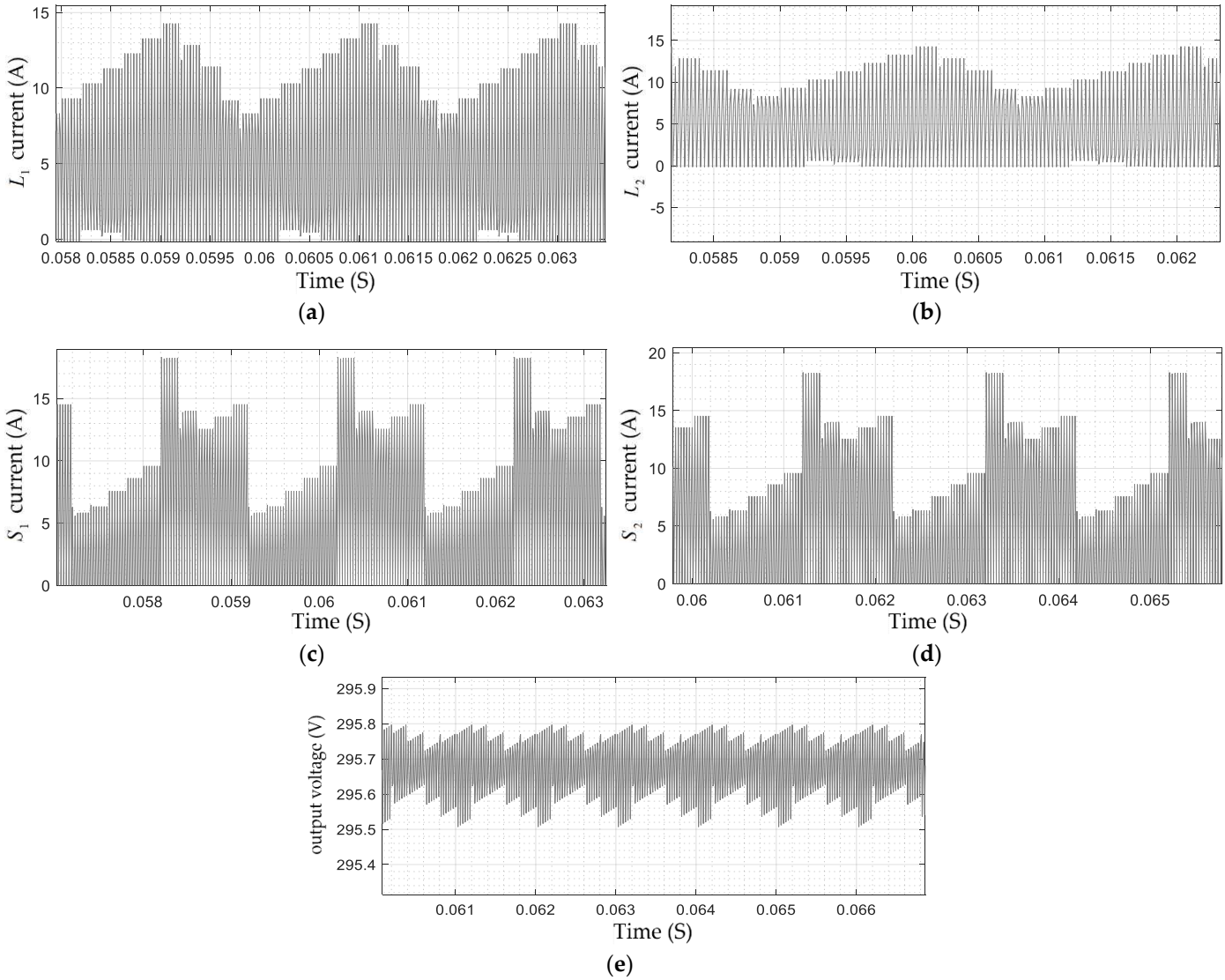

Figure 10. The results in DCM, (**a**) L_1 current, (**b**) L_2 current, (**c**) S_1 current, (**d**) S_2 current, and (**e**) output voltage.

8. Conclusions

In this paper, a new topology of a non-isolated boost dc-dc converter is proposed for the off-board EV charger. High voltage gain and high-frequency transformer-less are the main advantages of the proposed topology. Throughout this paper, the operation of the proposed converter was analyzed at CCM and DCM in detail. Additionally, the critical inductance calculations were carried out, and the designing considerations were extracted for choosing proper switches. Then, the proposed converter was compared with the existing topologies in the literature. The validity of the correctness of the theoretical concepts was verified through HiL setup based on the OPAL-RT simulator. As discussed in Section 2, the output voltage increased to 210 V and 295 V at CCM and DCM, respectively, by $D = 50\%$, $V_i = 70$ V and $f = 30.5$kHz with the calculated efficiency equal to 93.1%. Additionally, the maximum peak current of switches reached 15 A, 13 A and 17 A at critical mode, CCM and DCM, respectively. Therefore, the proposed topology can be a suitable appliance as an EV charger.

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