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Single-active switch high-voltage gain DC–DC converter using a non-coupled inductor

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Abstract

A single-active switch high-voltage gain non-coupled inductor DC–DC converter is presented. The introduced converter achieves high step-up gain without using any coupled inductors or transformers, provides high efficiency, and has a simple control system. The converter also achieves low voltage stress on the switch and diodes without clamping circuits, reducing cost, conduction losses, and complexity. The input current of the introduced converter is continuous with low ripple, and is therefore suitable for renewable energy applications in which the fast dynamic response of the converter is necessary. The principle of operation and design considerations of the introduced converter are investigated. A 200 W prototype circuit with 40 kHz switching frequency, 40 V input voltage, and 250 V output voltage is implemented. The prototype operates at 93.2% efficiency, with voltage and current error of less than 4% compared to theoretical values.

1 | INTRODUCTION

Recently, due to political focus on environmental issues, global warming and rising global energy demand, renewable energy sources such as photovoltaic systems (PV), wind power, and fuel cells have received more attention. However, some renewable energy sources such as PV and energy storage systems have low output voltage, particularly for small systems or where active cell balancing is required. Hence, research in high-voltage gain DC–DC converters has been increasing in recent years. In addition to their use in renewable energy systems, high gain DC–DC converters are also used in other applications, e.g. DC distribution networks, uninterruptible power supplies (UPS), and energy storage systems [1].

For conventional DC–DC converters to operate with high gain, they require a very high duty cycle resulting in reverse recovery problems with diodes and high conduction losses in the semiconductor devices. In addition, conventional DC–DC converters suffer from high-voltage stress on diodes and switches. As an example, the switch voltage stress in the boost converter is equal to the output voltage. It is hence necessary to use a high-voltage rating switch which typically has higher

on-state resistance $R_{ds(on)}$, causing increased conduction losses. Numerous high gain DC–DC converters have been introduced to tackle these issues in conventional DC–DC converters [2, 3].

Isolated and non-isolated converters are two main groups of the hard-switched high gain step-up DC–DC converters. Isolated converters such as flyback converter and forward converter use a high-frequency transformer. Thus, higher gain can be achieved by increasing the transformer turns ratio. Nevertheless, the coupled magnetic component increases the volume and weight of the converter. Furthermore, the leakage inductance of the transformer causes voltage spikes to occur on the switches [4]. Hence, active or passive clamp circuits are frequently used to decrease the amplitude of the spike and recycle the energy stored in the leakage inductance. These mitigations rise the cost and complexity [5, 6].

Non-isolated DC–DC converters are divided into coupled inductor converters and non-coupled inductor converters. Since the coupled inductor converters suffer from leakage inductance, a clamp circuit is frequently needed to recycle the stored energy and limit ringing [7, 8]. For this reason, coupled inductor converters suffer from the similar drawbacks to those mentioned for isolated converters [9–11]. In grid-connected applications, a

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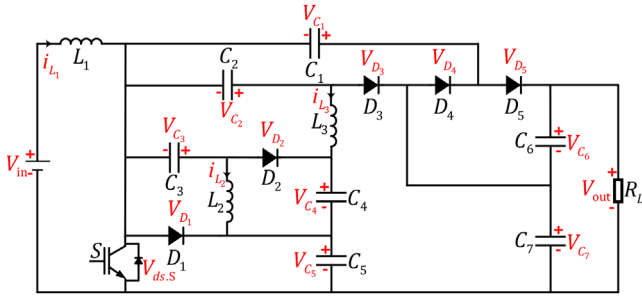


FIGURE 1 The schematic of the introduced DC–DC converter

big transformer is already required at the AC side, which makes high frequency transformers in each converter less attractive. Accordingly, attention in non-coupled inductor converters has increased [12].

Nevertheless, non-coupled inductor converters have some disadvantages, e.g. lower gain, high-voltage stress on switches, and high ripple of input current [13]. Many techniques have been introduced for non-coupled inductor DC–DC converters to overcome their demerits. For instance, the cascade technique [14, 15], interleaved technique [16,17], voltage lift technique [18], quadratic technique [19,20], voltage multiplier technique [21, 22] are introduced to enhance the performance of the DC–DC converters in terms of efficiency, gain, input current ripple, and voltage stress on semiconductors. However, these converters suffer from high component count, low efficiency, and complicated control. In [23–28], recent non-coupled inductor high gain DC–DC converters have been introduced. Even though these converters can benefit from far higher gain in comparison with the conventional DC–DC converters, their voltage gains are not sufficient in some applications. Therefore, recently, a high-voltage gain step-up non-coupled inductor DC–DC converter has been introduced in [29] which provides a very high-voltage gain $(1 + 3D)/(1 - D)$. However, this converter has two switches with two isolated gate drives, which rises the complexity, cost, and size. Moreover, the converter has high ripple of input current. Hence, it needs a large input filter which slows the dynamic response of the control system and power density. It is worth noting that changing voltage level is not the only application for DC–DC converters: frequently they are used for maximum power point tracking (MPPT) in photovoltaic systems. In PV systems, a large input filter slows down the dynamic response of the system.

In order to enhance the performance of power conversion for PV, a high-voltage gain step-up non-coupled inductor DC–DC converter is introduced and shown in Figure 1. The voltage gain of the presented DC–DC converter is higher than the voltage gain of the state-of-the-art converters proposed in [24–29] for a given duty cycle. Thus, it can provide high gain with lower duty ratio, which increases the efficiency. Moreover, the voltage stress across the switch and diodes in the introduced converter is lower than the converters presented in [24–29]. This allows lower voltage rating semiconductors and hence lower conduction losses and cost to be used. In addition, the

absence of coupled magnetics in the proposed converter means it shares the merits of the non-coupled inductor converters, e.g. high power density, low electromagnetic interference (EMI), reduced cost and the lack of voltage spike across the semiconductors. Furthermore, since the output voltage of the presented topology divides between two capacitors (C_6 and C_7), low voltage capacitors which are cheaper and more commercially available can be used. Finally, the presented converter uses only one switch and has a continuous input current with low ripple. Hence, the introduced converter is suitable for many PV applications.

This paper is arranged as follows: the principle of operation of the introduced converter is presented in Section 2. Then, the design consideration and performance comparison of the introduced converter with some recent DC–DC converters are investigated in Sections 3 and 4, respectively. In Section 5, the experimental results of the introduced converter are provided. Finally, the conclusion is presented in Section 6.

2 | OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

The introduced high gain DC–DC converter is illustrated in Figure 1. The introduced converter consists of a switch S_1 , three non-coupled inductors L_{1-7} , five diodes D_{1-5} , and seven capacitors C_{1-7} . The following assumptions are made in order to simplify the theoretical analysis:

1. All components are considered ideal.
2. All the capacitors are considered large enough in order that their voltages remain constant in each switching cycle.
3. All diodes possess zero forward voltage drop

The principle of operation and steady-state analysis of the converter in continuous conduction mode (CCM), discontinuous conduction mode (DCM), and boundary conduction mode (BCM) is discussed below.

In the following analyses, T_s is the switching period which begins with the switch S_1 just turning on, D is duty ratio of the switch and δ is the proportion between switch turn off and all diode currents falling to zero.

2.1 | CCM operation

The introduced converter operates in two modes per switching period in CCM. The key waveforms of the introduced converter over a single switching cycle are shown in Figure 2(a). The converter is considered to be operating in state such that $x(t = 0) = x(t = T_s)$ where x is a capacitor voltage or inductor current. Also, at $t = 0$, the inductor currents and capacitor voltages are positive.

Mode I [$0 \leq t < DT_s$]: The equivalent circuit of the introduced converter during this mode is shown in Figure 3(a). Switch S_1 is turned on. The diodes D_1 , D_2 , D_3 , and D_5 are

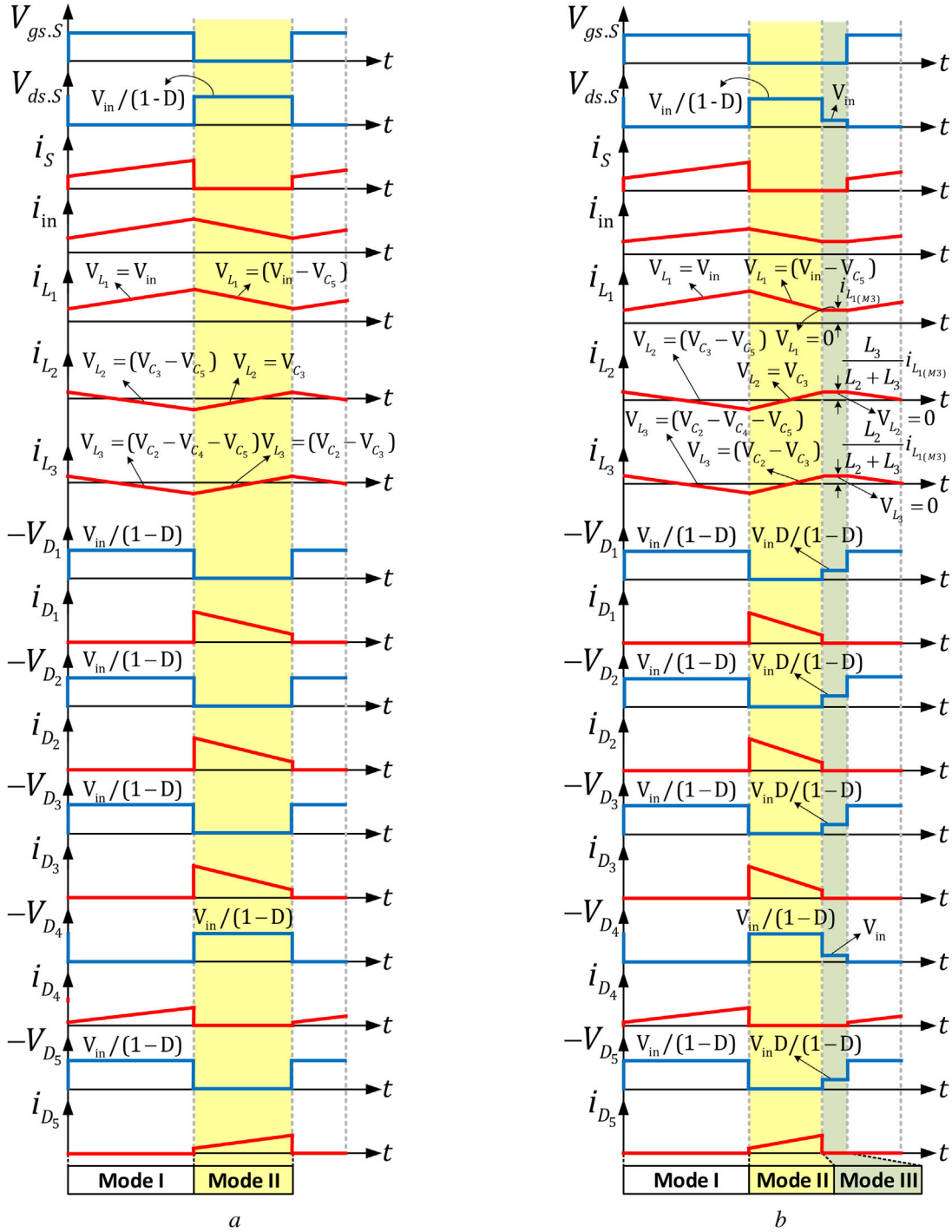


FIGURE 2 The key waveforms of the introduced topology. (a) Continuous conduction mode (CCM) operation and (b) discontinuous conduction mode (DCM) operation

reverse biased and diode D_4 is forward biased. The inductor L_1 has the full supply voltage across it, and its current increases linearly. Meanwhile, the energy stored in the inductors L_2 and L_3 decreases. Capacitor C_1 is charging and capacitors C_6 and C_7 are discharging. In addition, the capacitors C_2 , C_3 , C_4 , and C_5 charge and discharge according to the current direction in L_2 and L_3 , which is not constant during the mode. The voltages across the inductors may be obtained as follows, noting that the

charge on each capacitor is constant over a switching cycle:

$$V_{L_1} = V_{in}, \tag{1}$$

$$V_{L_2} = V_{C_3} - V_{C_5}, \tag{2}$$

$$V_{L_3} = V_{C_2} - V_{C_4} - V_{C_5}. \tag{3}$$

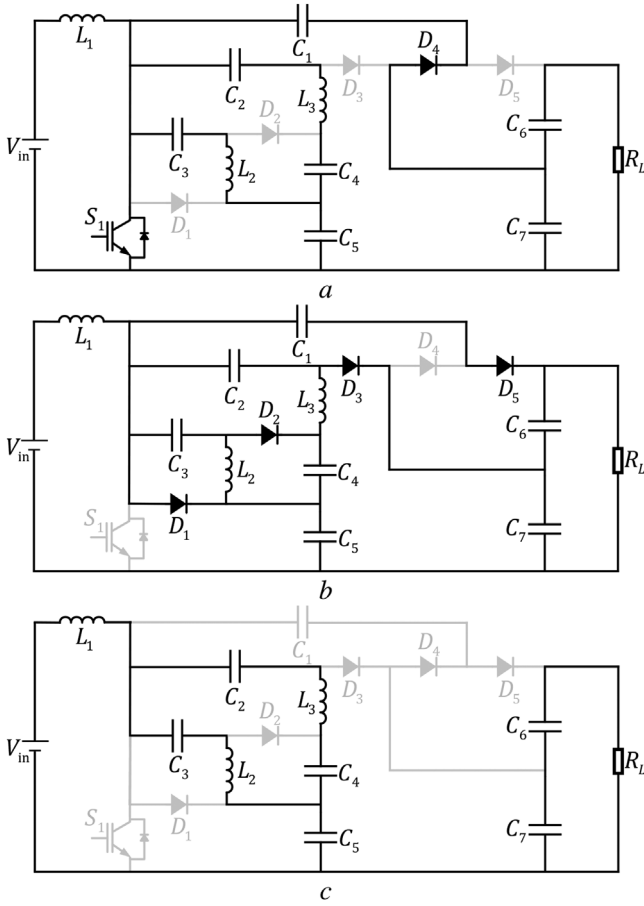


FIGURE 3 Equivalent circuit of the introduced circuit in one switching period in different modes. (a) Mode I, (b) mode II, and (c) mode III for discontinuous conduction mode (DCM) operation

Mode II [$DT_s \leq t < T_s$]: The equivalent circuit in this mode is presented in Figure 3(b). S_1 is turned off. $D_1, D_2, D_3,$ and D_5 are forward biased and diode D_4 is blocking. L_1 is discharging, and the inductors L_2 and L_3 are charging. C_1 is discharging and capacitors C_6 and C_7 are charging. As in Mode I, $C_2, C_3, C_4,$ and C_5 charge and discharge according to the current direction in L_2 and L_3 , which again is not constant during this mode. The voltage across inductors may be obtained as follows:

$$V_{L_1} = V_{in} - V_{C_3}, \tag{4}$$

$$V_{L_2} = V_{C_3}, \tag{5}$$

$$V_{L_3} = V_{C_2} - V_{C_3}. \tag{6}$$

According to Figure 3(a) and (b) and noting that the charge on each capacitor is constant over a switching period, the voltage of the capacitor C_1 is equal to the voltage of the capacitor C_7 , and the voltage of the capacitor C_3 is equal to the voltage of the capacitor C_4 :

$$V_{C_1} = V_{C_7}, \tag{7}$$

$$V_{C_3} = V_{C_4}. \tag{8}$$

In addition, Equations (9) and (10) can be obtained according to Figure 3(b):

$$V_{C_1} = V_{C_6} + V_{C_2}, \tag{9}$$

$$V_{C_2} = V_{C_7} - V_{C_5}. \tag{10}$$

From the Equations (7–10), the Equation (11) is obtained:

$$V_{C_5} = V_{C_6}. \tag{11}$$

From the volt-second balance principle on the inductors and using Equations (1–11) and (13–16) are derived:

$$\int_0^{DT_s} V_{L_{1,2,3}} dt + \int_{DT_s}^{T_s} V_{L_{1,2,3}} dt = 0, \tag{12}$$

$$V_{C_5} = V_{C_6} = \frac{V_{in}}{1-D}, \tag{13}$$

$$V_{C_3} = V_{C_4} = \frac{DV_{in}}{1-D}, \tag{14}$$

$$V_{C_2} = \frac{2DV_{in}}{1-D}, \tag{15}$$

$$V_{C_1} = V_{C_7} = \frac{(2D+1)V_{in}}{1-D}. \tag{16}$$

According to Figure 1, the output voltage V_{out} is equal to the sum of output capacitors (C_6, C_7). So,

$$V_{out} = V_{C_6} + V_{C_7}. \tag{17}$$

Then, according to the Equation (17) and substituting Equations (13) and (16) into Equation (17), the voltage gain of the introduced DC–DC converter in CCM operation M_{CCM} may be obtained as Equation (18):

$$M_{CCM} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{2D+2}{1-D}. \tag{18}$$

2.2 | DCM operation

The introduced converter operates in DCM under light loads (the boundary condition is given in Equation (34) later). There are three modes in each switching period.

The key waveforms of the introduced topology under DCM operation in one switching cycle are illustrated in Figure 2(b). Modes I and II in DCM are the same as the modes I and II in CCM. However, in mode III, all the semiconductor devices are off.

The equivalent circuit of the introduced topology during mode III $[(D + \delta)T_s \leq t < T_s]$ is presented in Figure 3(c). The voltage across each inductor is zero; therefore, the currents through the inductors remain constant during this interval:

$$V_{L_1} = V_{L_2} = V_{L_3} = 0. \quad (19)$$

By considering the voltage-second balance principle for the inductors, Equations (20–22) can be derived:

$$\int_0^{DT_s} V_{in} dt + \int_{DT_s}^{(\delta+D)T_s} (V_{in} - V_{C_5}) dt + \int_{(\delta+D)T_s}^{T_s} 0 dt = 0, \quad (20)$$

$$\int_0^{DT_s} (V_{C_3} - V_{C_5}) dt + \int_{DT_s}^{(\delta+D)T_s} V_{C_3} dt + \int_{(\delta+D)T_s}^{T_s} 0 dt = 0, \quad (21)$$

$$\int_0^{DT_s} (V_{C_2} - V_{C_4} - V_{C_5}) dt + \int_{DT_s}^{(\delta+D)T_s} (V_{C_2} - V_{C_3}) dt + \int_{(\delta+D)T_s}^{T_s} 0 dt = 0. \quad (22)$$

From Equations (7–11) and (20–22), with some manipulation the following can be obtained:

$$V_{C_5} = V_{C_6} = \frac{(D + \delta)}{\delta} V_{in}, \quad (23)$$

$$V_{C_3} = V_{C_4} = \frac{D}{\delta} V_{in}, \quad (24)$$

$$V_{C_2} = \frac{2D}{\delta} V_{in}, \quad (25)$$

$$V_{C_1} = V_{C_7} = \frac{(3D + \delta)}{\delta} V_{in}. \quad (26)$$

By substituting Equations (23) and (26) into Equation (17), the voltage gain of the introduced topology in DCM operation is obtained:

$$M_{DCM} = \frac{V_{out}}{V_{in}} = \frac{4D + 2\delta}{\delta}. \quad (27)$$

The average of the input current and the output current can hence be found:

$$I_{in} = \frac{1}{T_s} \left(\frac{\Delta i_{L_1}}{2} (D + \delta) T_s + I_{L_1(M_3)} T_s \right), \quad (28)$$

$$I_{out} = \frac{1}{T_s} \left(\frac{\Delta i_{L_3}}{2} (D + \delta) T_s - \frac{L_2}{L_2 + L_3} I_{L_1(M_3)} T_s \right), \quad (29)$$

where Δi_{L_i} ($i = 1, 2, 3$) is peak-to-peak ripple current of L_i and $I_{L_1(M_3)}$ is the constant current through L_1 in mode III. The current through all inductors is constant during mode III, since the voltage across them is 0. Assuming efficient operation, input and output powers are considered equal. Thus,

$$V_{in} I_{in} = V_{out} I_{out}. \quad (30)$$

From Equation (28–30), Equation (31) is obtained:

$$I_{L_1(M_3)} = \frac{D\delta V_{in} (D + \delta)}{2f_s \left((4D + 2\delta) \frac{L_2}{L_2 + L_3} + \delta \right)} \left(\frac{M_{DCM}}{L_3} - \frac{1}{L_1} \right). \quad (31)$$

Substituting Equation (31) into Equation (29) and assuming L_2 and L_3 are equal, we can derive an expression for δ and the converter gain:

$$\delta = \frac{1 + \sqrt{1 + 4D^2 Z}}{DZ}, \quad (32)$$

$$M_{DCM} = \frac{V_{out}}{V_{in}} = \frac{4D^2 Z + 2 + 2\sqrt{1 + 4D^2 Z}}{1 + \sqrt{1 + 4D^2 Z}}, \quad (33)$$

where Z is

$$Z = R \frac{1/L_3 + 1/(2L_1)}{4f_s}. \quad (34)$$

2.3 | Boundary operation

The introduced DC–DC converter operates under BCM operation when the voltage gain of the converter in CCM is equal to the voltage gain of the converter in DCM. Therefore, in BCM operation, Z may be obtained as follows:

$$Z_B = \frac{2D + 2}{D(1 - D)^2}. \quad (35)$$

If $Z < Z_B$, the introduced converter operates in CCM and if $Z > Z_B$, it operates in DCM. The voltage transfer gain versus Z is illustrated in Figure 4.

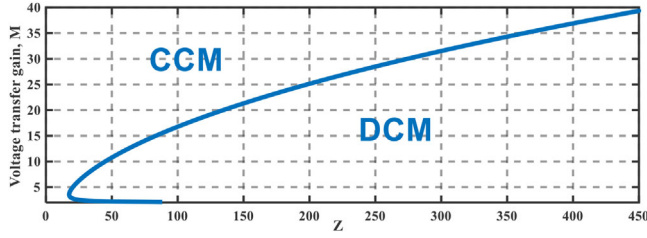


FIGURE 4 Voltage transfer gains versus Z in discontinuous conduction mode (DCM) and continuous conduction mode (CCM) operation

3 | DESIGN CONSIDERATIONS

The proposed converter may operate under DCM; however, operation in DCM can result in high input current ripple, requiring a large input filter which slows the dynamic response time. DCM operation also causes high voltage and current stress to the semiconductor devices, requiring high-performance devices and hence causing high conduction and switching losses. The introduced DC–DC converter should therefore be designed properly to operate in CCM [29]. Hence, the components are selected according to the provided equations in this section. The validation of these equations is discussed in Section 5.

3.1 | Voltage stress across the semiconductor devices

From Figures 2 and 3, the voltage stress across the semiconductor devices may be obtained as follows:

$$V_{ds(\max)} = \frac{V_{in}}{1-D}, \quad (36)$$

$$V_{D_{1-5}(\max)} = \frac{V_{in}}{1-D}. \quad (37)$$

3.2 | Inductor design

The voltages across inductors L_1 , L_2 , and L_3 in mode I are obtained from Equations (1–3). According to Equations (1–3) and (13–15), in mode I, voltages across inductors are equal to V_{in} . The inductance required is found by considering the increase in current during mode I alone. Thus, for a given current ripple specification, identical inductors may be used. This value may be found in Equation (38):

$$L_i = \frac{V_{in}D}{\Delta I_{L_i} f_s} \quad i = 1, 2, 3. \quad (38)$$

It is possible to use different inductors should the application require it, e.g. for low input ripple applications.

3.3 | Capacitor selection

The capacitor values, which depend on the output current (I_{out}), duty cycle (D), voltage ripple (ΔV_C), and switching frequency (f_s), may be found using Equations (39–42):

$$C_1 = \frac{I_{out}}{\Delta V_{C_1} f_s}, \quad (39)$$

$$C_i = \frac{DI_{out}}{\Delta V_{C_i} f_s} \quad i = 2, 3, 4, 6, \quad (40)$$

$$C_5 = \frac{2DI_{out}}{\Delta V_{C_5} f_s}, \quad (41)$$

$$C_7 = \frac{(1-D)I_{out}}{\Delta V_{C_7} f_s}. \quad (42)$$

In practice, the ripple requirements for most capacitor are likely to be the same in order to equalise capacitor ageing. C_6

TABLE 1 The performance comparison of the introduced converter with other topologies

Parameter	Boost converter	[24]	[25]	[26]	[27]	[28]	[29]	Proposed converter
Number of switches	1	1	1	1	1	1	2	1
Number of diodes	1	2	3	3	5	3	2	5
Number of inductors	1	2	3	4	3	1	3	3
Number of capacitors	1	3	5	6	7	3	3	7
Total device count	4	8	12	14	16	8	10	16
Continuous input current	Yes	Yes	No	Yes	No	No	Yes	Yes
Current ripple	Low	Low	High	Low	High	High	High	Low
Voltage gain	$\frac{1}{1-D}$	$\frac{1+D}{1-D}$	$\frac{3D}{1-D}$	$\frac{3D}{1-D}$	$\frac{4-3D}{1-D}$	$\frac{2D}{1-D}$	$\frac{3D+1}{1-D}$	$\frac{2D+2}{1-D}$
Voltage stress on switch	V_{out}	$\frac{V_{out}}{1+D}$	$\frac{V_{out}}{3D}$	$\frac{V_{out}}{3D}$	$\frac{V_{out}}{4-3D}$	$\frac{V_{out}}{2}$	$\frac{V_{out}}{1+3D}$	$\frac{V_{out}}{2+2D}$
Voltage stress on diodes	V_{out}	$\frac{V_{out}}{1+D}$	$\frac{V_{out}}{3D}$	$\frac{V_{out}}{3D}$	$\frac{V_{out}}{4-3D}$	$\frac{V_{out}}{2}$	$\frac{2V_{out}}{1+3D}$	$\frac{V_{out}}{2+2D}$

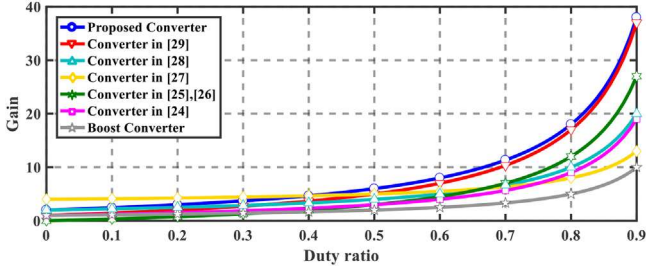


FIGURE 5 The comparison of the voltage gain

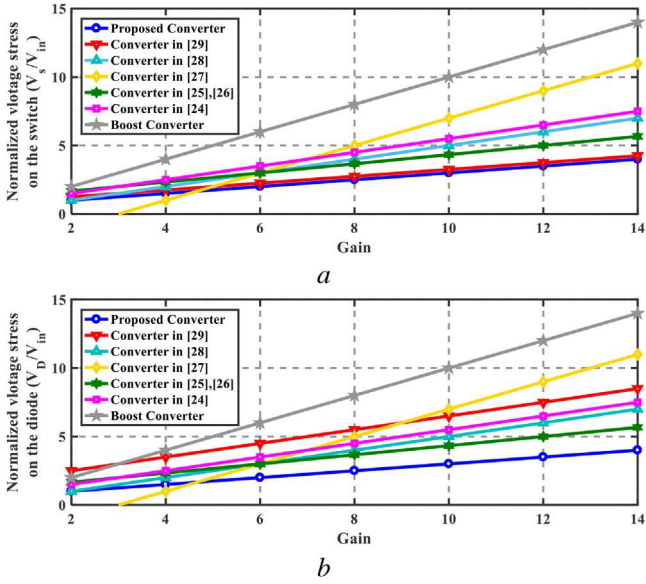


FIGURE 6 The comparison of voltage stress across (a) Switches and (b) diodes

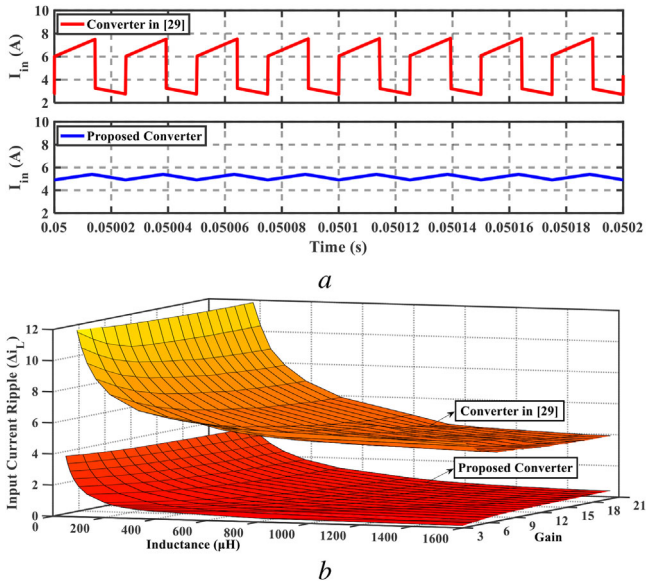
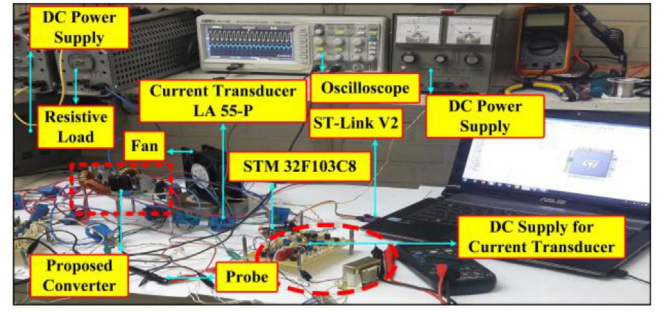
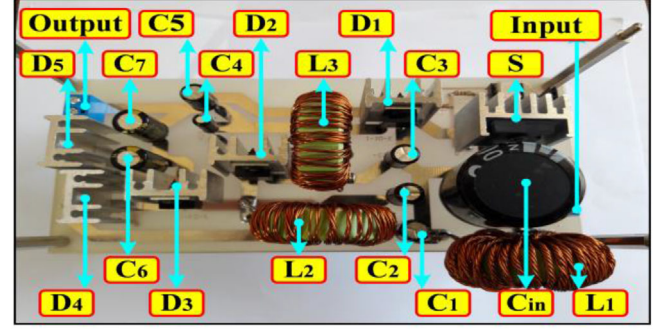


FIGURE 7 The comparison of the input current. (a) The input current waveforms in nominal conditions with $\Delta i_L = 0.5$ A and $M_{CCM} = 6.25$ and (b) input current ripple versus inductance and gain values. $P_o = 200$ W, $V_{in} = 40$ V, and $f_s = 40$ kHz



a



b

FIGURE 8 Proposed converter. (a) Experimental prototype and (b) laboratory set-up

TABLE 2 The components of the proposed converter

Parameter	Parameter	Value
P_o	Output power	200 W
V_{in}	Input voltage	40 V
V_{out}	Output voltage	250 V
f_s	Switching frequency	40 kHz
L_1, L_2, L_3	Inductors	177, 172, 172 μH
$C_1, C_2, C_3, C_4, C_5, C_6, C_7$	Capacitors	4.7, 3.3, 3.3, 3.3, 4.7, 15, 15 μF
S	Switch	IRFP150
D_{1-5}	Diodes	UG8GT

and C_7 , the output capacitors, may have more stringent requirements according to the application (e.g. hold-up time).

3.4 | Design procedure

Finally, the components of the proposed converter can be selected using the following procedure:

1. Calculation of the duty cycle according to given input and output voltages by (18).
2. Calculation of the inductance values from Equation (38). It should be mentioned that the low peak-to-peak current ripple of the inductors reduces the hysteresis losses; however, it also increases the volume, cost, and conduction losses of the

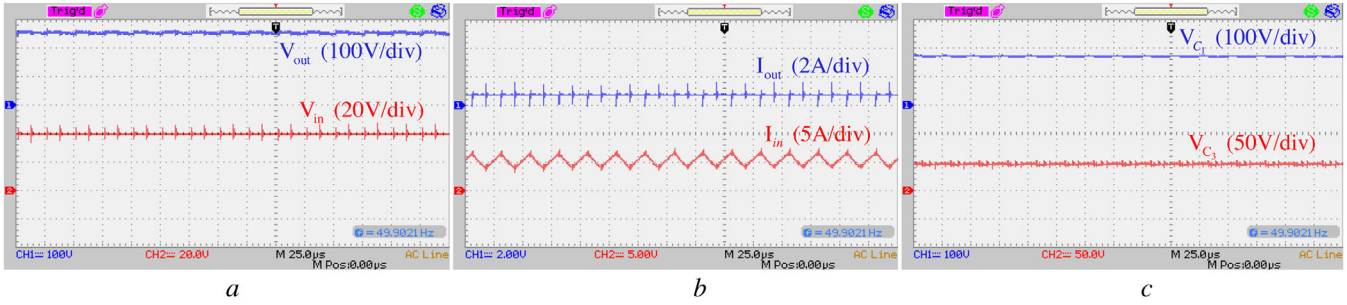


FIGURE 9 The experimental results for (a) output and input voltage, (b) output and input current, and (c) voltage of the capacitors C_1 and C_2

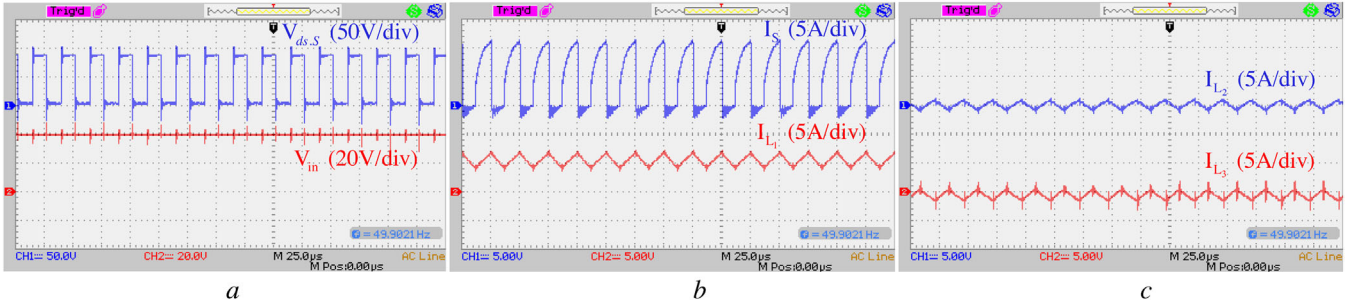


FIGURE 10 The experimental results for (a) the switch voltage and input voltage, (b) switch current and inductor L_1 , and (c) current of inductors L_2 and L_3

inductors. Therefore, a compromise must be found according to the requirements of the application. In addition, in order that the converter operates in CCM, the inductances should ensure that $Z < Z_B$ using Equations (34) and (35).

- The capacitor values may be calculated by Equations (39–42). The more the capacitance, the lower the voltage ripple. However, high capacitance leads to increased volume and high cost. Again, a compromise is required.
- The switch and diodes are then selected, taking account of their voltage and current stress, given by Equations (36) and (37).

4 | PERFORMANCE COMPARISON

In this section, the features of the introduced topology are compared with other topologies. A comparison between the introduced topology, the converters in [24–29], and the boost converter is presented in Table 1 with voltage gain comparison shown in Figure 5. From Table 1 and Figure 5, it can be seen that the voltage gain of the introduced topology is higher than the voltage gain of the topologies in [24–29] and boost converter for a given duty ratio.

The voltage stresses on the switches and diodes in the introduced topology are lower than the topologies in [24–29] and boost converter, as shown in Figure 6(a) and (b), respectively. The lower voltage stress permits the use of semiconductors with lower conduction losses and cost can be used. In addition, the introduced converter compared to the converter in [29] has one switch fewer. In addition, the introduced converter benefits

from continuous input current with low ripple, while the converter in [29] suffers from the high current ripple. The introduced topology and converter in [29] were designed for similar input and output voltage specification, power, inductor, and capacitor current ripple and their input currents are shown in Figure 7(a). The input current ripple of the introduced topology is about 82.76% lower compared to the converter in [29]. Therefore, the introduced converter is more suitable to be used in many renewable energy applications (e.g. PV) since it needs a smaller input filter. Moreover, the input current ripple of both converters for different inductance and gain values are shown in Figure 7(b). Not only does the proposed converter provide a lower current ripple in all conditions, but it is also less sensitive to inductance and gain.

5 | EXPERIMENTAL RESULTS

In order to verify the theoretical analysis of the introduced converter, a 200 W prototype was constructed and the experimental prototype and set-up are shown in Figure 8(a) and (b), respectively. The control of the introduced converter is simpler than resonant converters since its output voltage is neither load- nor frequency dependent. In addition, the proposed converter only has one switch while, for example the converter in [29] requires two switches with different isolated gate drives. In order that the output voltage in the introduced converter can be controlled, only the duty cycle needs to be adjusted. Therefore, the presented converter can be implemented with a simple control system.

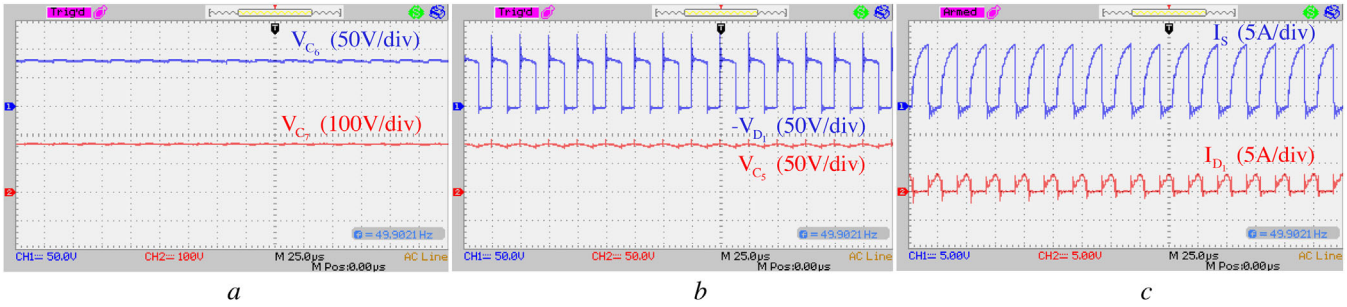


FIGURE 11 The experimental results for (a) voltage of the capacitors C_6 and C_7 , (b) voltage of the diode D_1 and capacitor C_5 , and (c) switch current and diode D_1

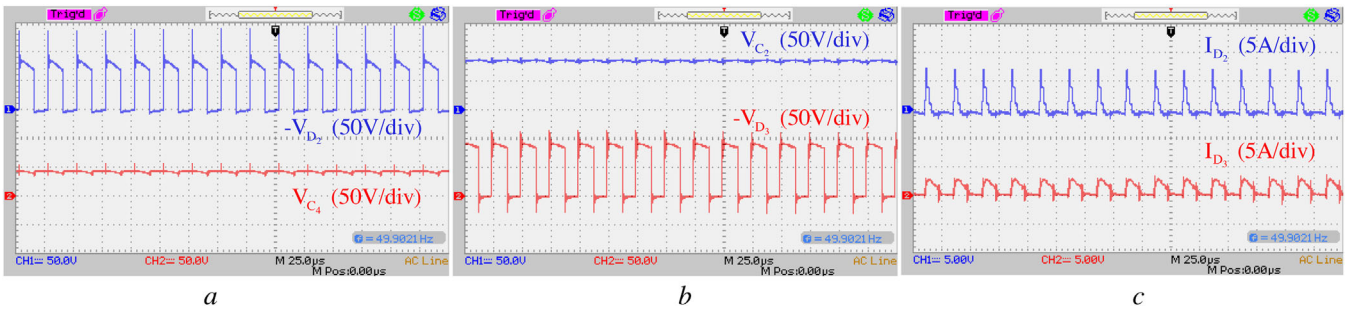


FIGURE 12 The experimental results for (a) voltage of the diode D_2 and capacitor C_4 , (b) voltage of the diode D_3 and capacitor C_2 , and (c) current of the diodes D_2 and D_3

The specification of the proposed converter and the component values selected by procedure in Section 3.4 are listed in Table 2. The switching frequency of the power converter is directly proportional to the switching losses and inversely proportional to the inductor and capacitor size. Therefore, there is a trade-off between the switching losses and volume of the converter. According to the experience of the authors, a switching frequency of 40 kHz is appropriate, but can be changed to suit the constraints of a particular application. According to Equation (18), the required duty cycle is 51.5%. The inductor values are calculated as 172 μ H using Equation (38), assuming the current ripple is 3 A. From Equations (34) and (35), Z and Z_B are 17 and 25, respectively. Hence, $Z < Z_B$ is satisfied and the converter operates under CCM. The capacitor values are calculated using Equations (37–40) and shown in Table 2. The design voltage ripple is 1 V for C_6 and C_7 , and 5 V for the other capacitors. The voltage stress on the diodes and switch are less than 100 V; hence, MOSFET IRFP150 and ultrafast rectifier diodes UG8GT are selected. In the prototype, the gating pulse for the switch is generated by an ARM-based STM32F103C8 microcontroller. To compensate for losses, duty cycle was increased to 53% at 40 kHz to produce 250V at the output.

The experimental results of the introduced converter, including voltage and current waveforms are presented in Figures 9–13. The output and input voltage are illustrated in Figure 9(a). It can be seen that the input and output voltages

are 40 and 250 V, respectively. The measured currents through inductors L_1 , L_2 , and L_3 are shown in Figure 10(b) and (c). According to the experimental results, the current ripple of the inductors is 3.1 A, in agreement with Equation (38). The input current of the introduced topology is continuous with a low ripple, which shows it is suitable for many renewable energy applications.

Relevant voltages, calculated by theoretical analysis and measured by experimental results, are listed in Table 3. In addition, the error between theoretical analysis and experimental results is presented as well. Results show good agreement with errors typically below 4%, indicating correct operation of the converter.

The efficiency versus output power curve for the introduced converter is illustrated in Figure 13(c). The efficiency at 200 W output power is 93.2%. To study the sources of loss, the presented converter was simulated in MATLAB and, with the help of the equations provided in [29], its loss distribution is calculated and illustrated in Figure 14. As shown, the conduction losses are dominant, which is typical of high gain step-up DC–DC converters. An important question is why efficiency of the converter in [29] at 200 W is about 93% even though it has two switches and fewer number of components compared to the proposed converter. It has to be mentioned that the converter in [29] is designed with a lower input voltage than the proposed converter, despite the same powers. Its input current is therefore higher; hence there is higher conduction losses per component.

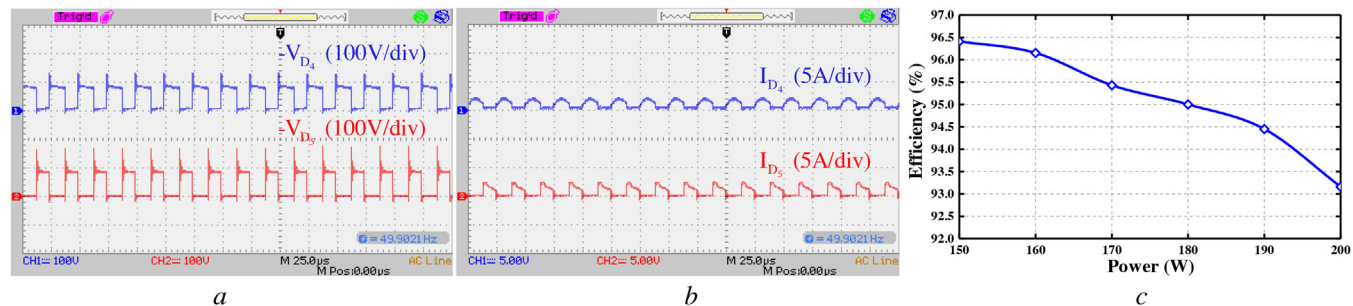


FIGURE 13 The experimental results for (a) voltage of the diodes D_4 and D_5 , (b) current of diodes D_4 and D_5 , and (c) the efficiency of the proposed converter in practical

TABLE 3 The average deviation between theoretical analysis and experimental results

Parameter	Equation	Calculated (V)	Measured (V)	Error (%)
Gain	(18)	260	250	<4
V_{ds}	(36)	85.1	87.6	<3
V_{D_1}	(37)	85.1	85.4	<2
V_{D_2}	(37)	85.1	85.6	<2
V_{D_3}	(37)	85.1	88.4	<4
V_{D_4}	(37)	85.1	87.2	<3
V_{D_5}	(37)	85.1	86.8	<2
V_{C_1}	(16)	175	178	<2
V_{C_2}	(15)	90	88.2	<2
V_{C_3}	(14)	45.1	46.4	<3
V_{C_4}	(14)	45.1	44.8	<2
V_{C_5}	(13)	85.1	84.4	<2
V_{C_6}	(13)	85.1	81.6	<4
V_{C_7}	(16)	175	168	<4

the switch and diodes and high efficiency. Moreover, since there is no transformer or coupled inductor in the introduced topology, there is no high-voltage spike across the main switch and a clamp circuit is therefore not needed. The introduced topology is compared to some recent non-coupled inductor DC–DC converters. It provides higher gain while achieving low voltage stress across its single switch and its diodes. The converter also provides continuous input current with low ripple. Hence, the proposed converter can benefit from fast dynamic response, which is necessary in many renewable energy applications. Finally, experimental results are provided which verify theoretical analysis. Typical errors are under 4%.

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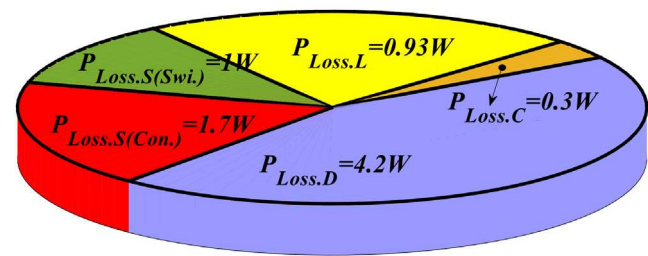


FIGURE 14 The power loss distributions of the proposed converter at 200 W output power

6 | CONCLUSION

A single-active switch high step-up non-coupled-inductor DC–DC converter is introduced. The introduced converter has a single switch and can be implemented with a simple control system. Additionally, the introduced converter has high-voltage gain, a non-inverted output voltage, low voltage stress across

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