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3-D Scaling Rules for High Voltage Planar Clustered IGBTs

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***Abstract*—In this paper, an approach for design optimization of high voltage (≥ 3300 V) planar Clustered IGBT (CIGBT) is proposed and investigated through TCAD simulations. New 3-D scaling rules are employed in this approach to improve the electrical characteristics and widen the safe operating area. As shown in the simulation results, a scaled 4.5 kV field-stop CIGBT can achieve an on-state voltage drop of 1.78 V at T_j = 300 K and J_c = 50 A/cm^2, mainly due to the enhancement of inherent thyristor action. High levels of turn-off robustness are maintained by the scaled CIGBTs. In addition, the scaling rules also result in improved short-circuit robustness due to control of current saturation levels. Furthermore, by integrating the 3-D scaling rules with the trench CIGBTs, the on-state performance shows significant improvement compared to the state-of-the-art IGBT technologies. Therefore, scaling rules on CIGBTs is a highly promising approach for enhancing the converter efficiency in medium and high voltage applications.**

***Index Terms*—IGBT, Clustered IGBT, scaling rule, safe operating area, short circuit capability, performance limit**

I. Introduction

NOWADAYS almost half of the worldwide electricity (~27600 TWh in 2019) is consumed by industrial motor drives in power electronics applications [1]. Assuming that the motor efficiency is 90 % and 30 % of the losses come from power switches, the total energy losses from power semiconductor devices are 414 TWh, which can fulfil the whole electricity usage in UK (294 TWh in 2019) [2]. As power semiconductor devices are widely used in energy transmissions, employing advanced power semiconductor technologies can save the energy waste by 25-40 % [3]. Therefore, continuous efforts are necessary to further improve the electrical characteristics of power semiconductor devices. Due to high current handling capability and high reliability, the Insulated Gate Bipolar Transistors (IGBTs) with blocking voltages from 3.3 kV up to 6.5 kV are widely used in high power applications such as industrial motor drives, transportations and smart power grids. Compared to the current-controlled thyristor devices such as Integrated Gate Commutated Thyristor (IGCT) and Gate Turn-Off thyristor (GTO), voltage controlled IGBTs can provide much higher switching frequency with smaller converter footprint and higher reliability [4]. Hence, the voltage-source converter technologies that using high voltage IGBTs are gradually replacing the line commutated converter options which are based on thyristor technologies in the HVDC transmissions [4]. However, the IGBTs exhibit higher on-state losses than thyristor devices due to lower on-state carrier densities as a result of lower current gains. Therefore, the MOS-Controlled Thyristor (MCT) devices are highly desirable to combine the advantages of both IGBTs and thyristors. Among the proposed MCT concepts, the Clustered IGBT (CIGBT) is the only MCT technology that has been experimentally demonstrated to show low on-state losses due to thyristor conduction, excellent current saturation behavior due to inherent self-clamping feature, and also fast switching speed due to PMOS actions [5-8]. Therefore, the CIGBT is a highly promising technology for high voltage power applications.

Recently, 3-D scaling concepts have been introduced to 1.2 kV trench IGBTs [9, 10]. Significant reduction in forward voltage drop ($V_{ce(sat)}$) can be achieved due to increased transconductance as well as Injection Enhancement (IE) effect. Nevertheless, the scaled narrow mesa IGBTs exhibit non-saturated I-V characteristics due to Collector Induced Barrier Lowering (CIBL) effect [11], which degrades the short-circuit robustness. This phenomenon can be attributed to the occurrence of conductivity modulation in the channel inversion layers of narrow mesa IGBTs [12]. As shown in Fig. 1(a), the n^+-cathode/P-base junction barrier of a scaled IGBT (*k3*-IGBT) decreases as collector voltage increases. The electron current is therefore continuously increasing with increased collector voltage. As the electron current serves as the base current of the PNP transistor, the total current increases as well and does not saturate. This phenomenon becomes more serious at high temperature due to decreased built-in potential at high temperature, as depicted in Fig. 1(b). In contrast, the 3-D scaling rules on 1.2 kV Trench Clustered IGBT [13] does not suffer from this drawback because the enhanced self-clamping feature can keep the MOS cells under the self-clamping voltage and therefore effectively control the current saturation levels. As the self-clamping voltage is independent of temperature, the CIBL effect can be effectively suppressed even under high temperature, as shown in Fig. 1(d).

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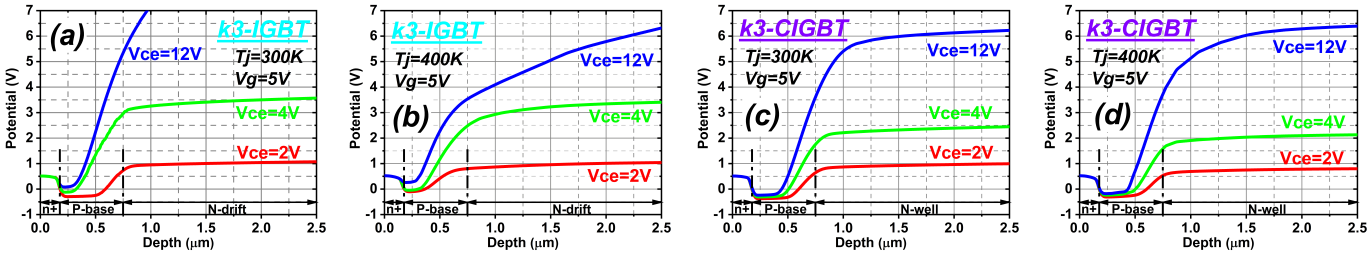

Fig. 1. Potential distributions within the middle mesa regions of scaled 1.2-kV *k3*-IGBT at (a) T_j = 300 K and (b) T_j = 400 K, and *k3*-CIGBT at (c) T_j = 300 K and (d) T_j = 400 K during forward conduction.

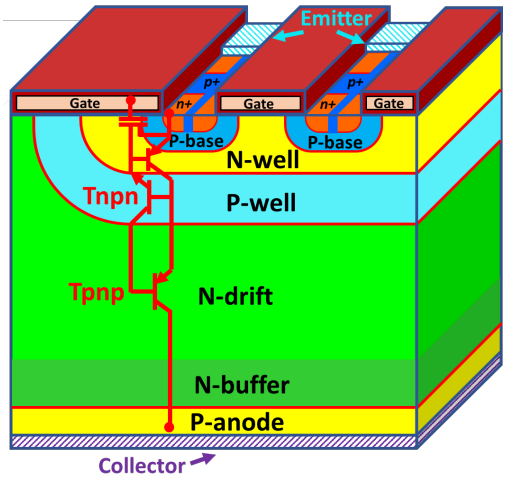

Fig. 2. 3-D cross section view of the planar CIGBT and its equivalent circuit.

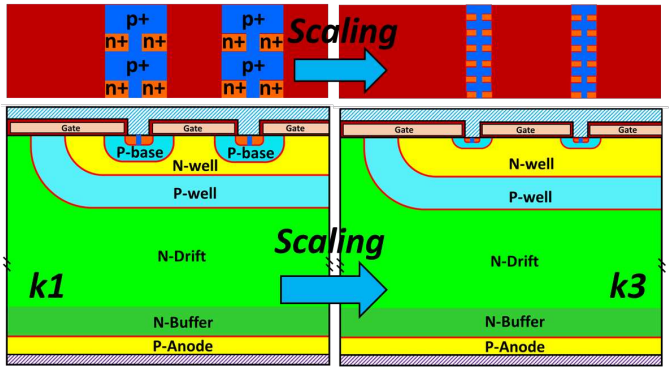

Fig. 3. 3-D scaling concept on the planar CIGBT.

In this paper, 3-D scaling rules for high voltage planar CIGBTs are proposed to improve the electrical characteristics and widen the safe operating area. A 4.5 kV field-stop planar CIGBT device is analyzed in detail to demonstrate the proposed 3-D scaling rules through 3-D TCAD tools [14]. Different from the previous scaling concept discussed in [13], the scaling rules proposed herein aim to achieve simultaneous reduction in on-state voltage drop and current saturation level. In addition, the on-state performances of the scaled CIGBTs are compared against the theoretical IGBT performance limit and state-of-the-art power semiconductor devices.

II. Device Structure and Scaling Concept

Fig. 2 shows the cross-section view of the 4.5 kV CIGBT device and its equivalent circuit. The CIGBT device employs a MOSFET to control a thyristor structure, which consists of N-well/P-well/N-drift transistor (T_{npn}) and P-well/N-drift/P-anode transistor (T_{pnp}). Its turn-on mechanism has been explained in previous papers [5, 8]. The cathode cells feature ladder design and the n^+ cathodes are penetrated by the p^+ cathodes. This unique design is used to suppress the turn-on of the parasitic n^+/P-base/N-well transistor at high current levels. The premature latch-up is therefore avoided during on-state.

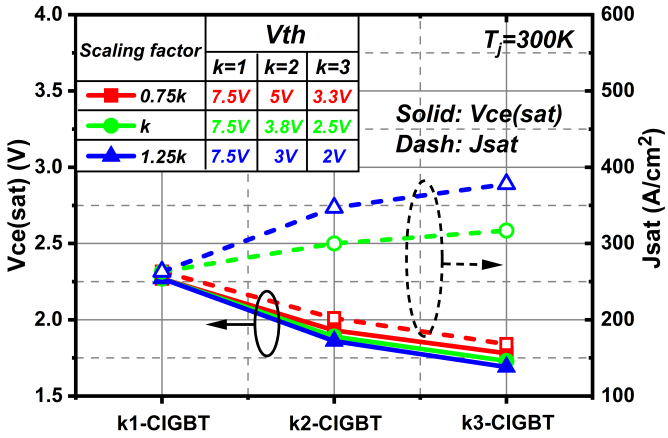

Fig. 4. Influence of scaling factors for V_{th} upon $V_{ce(sat)}$ and J_{sat}.

The proposed 3-D scaling rules and structural parameters are shown in Fig. 3 and Table I, respectively. As shown, the cell width and device thickness are kept identical for comparison whereas the main structure parameters of the MOS cells are shrunk as a factor of *k*. As the P-well thickness must be sufficient to support at least 5 kV blocking voltage for 4.5 kV device, and the N-well layer must provide a sufficient barrier to prevent holes from entering cathode cells prior to the turn-on of the thyristor, the N-well and P-well depths herein are not scaled and kept constant as conventional values. In addition, it should be noted that the gate voltage (V_g) is scaled down as *k* whilst the threshold voltage (V_{th}) is scaled as a factor of *0.75k*. Fig. 4 shows the influence of different scaling factors for V_{th} upon the $V_{ce(sat)}$ at J_c = 50 A/cm^2 and the saturation current density (J_{sat}). The J_{sat} is defined as the current density when dI/dV is zero in the I-V characteristics. A carrier lifetime of 50 μs is specified for holes and elections in the simulations. As shown, the variation of scaling factors for V_{th} has no significant influence upon the decrease of $V_{ce(sat)}$ whilst only the factor *0.75k* can achieve a decreasing trend of J_{sat}. This is because the P-base doping concentrations of the scaled devices are increased to achieve a factor *0.75k* for the V_{th}, and the increased P-base

TABLE I: PARAMETERS AND CHARACTERISTICS APPLIED FOR SCALING RULES.

Parameters & Characteristics	*Unit*	*k1*	*k2*	*k3*	*Scaling factor*
Cell Width	*μm*	32.7	32.7	32.7	*1*
n^+/p^+ Width	*μm*	1.8	0.9	0.6	*k*
P-base Width	*μm*	6.6	3.3	2.2	*k*
Channel Length	*μm*	2.4	1.2	0.8	*k*
p^+ Length	*μm*	4.5	2.25	1.5	*k*
n^+ Length	*μm*	1.5	0.75	0.5	*k*
Gate oxide thickness	*μm*	0.1	0.05	0.03	*k*
n^+/p^+ Depth	*μm*	0.5	0.25	0.17	*k*
P-base Depth	*μm*	2.5	2	1.5	-
N-well Depth	*μm*	4.5	4.5	4.5	*1*
P-well Depth	*μm*	15	15	15	*1*
P-base peak doping concentration	cm^{-3}	2×10^{17}	3.2×10^{17}	4.7×10^{17}	-
Gate Voltage (V_g)	*V*	15	7.5	5	*k*
Threshold Voltage (V_{th}) (T_j = *300 K*)	*V*	7.5	5	3.3	*0.75k*
Gate Resistance (R_g)	Ω	22	11	7.3	*k*
Electron Injection Efficiency γ_e	-	72%	72%	72%	1
Self-clamping Voltage (V_{scl})	*V*	21	18	15	-

Scaling rule: *Parameters of scaled devices (k = 2, 3) = Parameters of conventional device (k = 1) ÷ scaling factor*

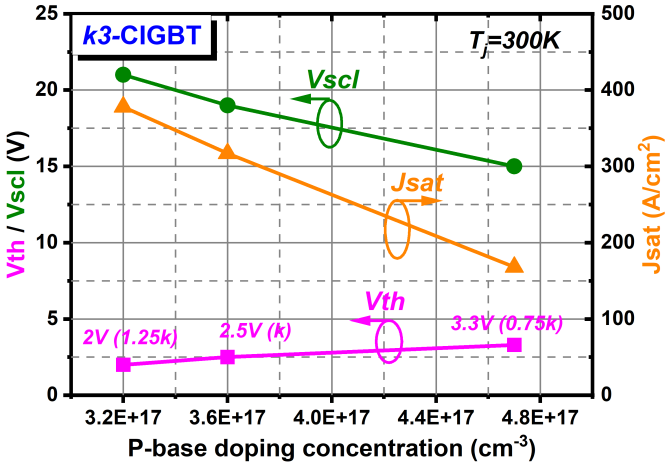

Fig. 5. Influence of P-base doping concentration upon V_{scl}, V_{th} and J_{sat} in k = 3. (V_g - V_{th} = 1.7 V)

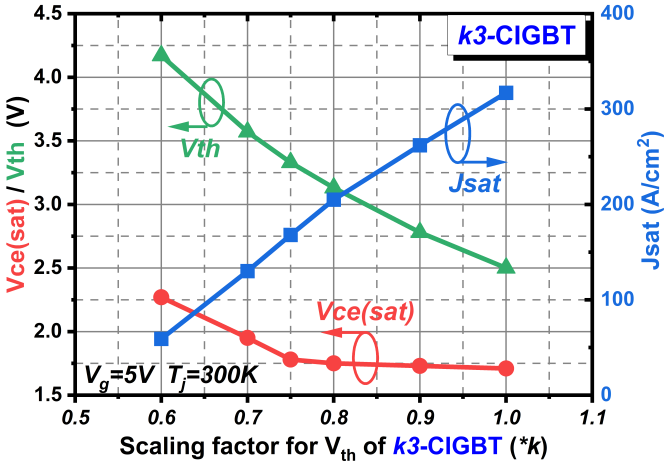

Fig. 6. Influence of various scaling factors for scaling V_{th} upon $V_{ce(sat)}$ and J_{sat} in *k*3-CIGBT. (V_g = 5 V)

doping concentration can reduce the self-clamping voltage (V_{scl}) in the scaled CIGBTs, as shown in Table I. In the CIGBT operation, lower V_{scl} can result in a lower J_{sat} [15]. To lower the V_{scl}, increasing P-base doping concentration is a direct solution. Fig. 5 shows the influence of P-base doping concentration on V_{th}, V_{scl} and J_{sat} in the case of *k3*-CIGBT. Note that the V_g - V_{th} and the P-base depth are kept identical so that the only variation is the P-base peak doping concentration. As shown, the V_{th} is increased with increasing P-base doping concentration whereas the V_{scl} is decreased with increased P-base doping concentration. As the V_g - V_{th} is kept identical, the reduction in J_{sat} is only because of the reduced V_{scl}. The detail reason can be explained as follows: The V_{scl} is essentially the punch-through voltage of the P-base/N-well/ P-well transistor. During forward conduction, the increasing collector voltage is first supported by the P-base/N-well junction. As the collector voltage increases, the depletion boundary within the P-base moves upwards whereas the depletion boundary within the N-well moves downwards. Higher P-base doping concentration can suppress the extension of depletion within the P-base layer. As a result, the N-well layer can be easily depleted with a lower V_{scl} and the J_{sat} is therefore reduced without affecting the $V_{ce(sat)}$. In addition, as shown in Fig. 6, other scaling factors (*0.6k, 0.7k, 0.8k, 0.9k*) for scaling the V_{th} of *k3*-CIGBT can also result in a reduced J_{sat} compared to the case at a scaling of *k*. However, the $V_{ce(sat)}$ increases dramatically when the scaling factor less than *0.75k*. Therefore, *0.75k* is finally selected for scaling the V_{th} to achieve simultaneous reduction in $V_{ce(sat)}$ and J_{sat}.

III. Electrical Characteristics and Discussion

A. Breakdown Characteristics

Fig. 7 shows the breakdown characteristics of the CIGBT devices. During blocking operation, the increasing collector

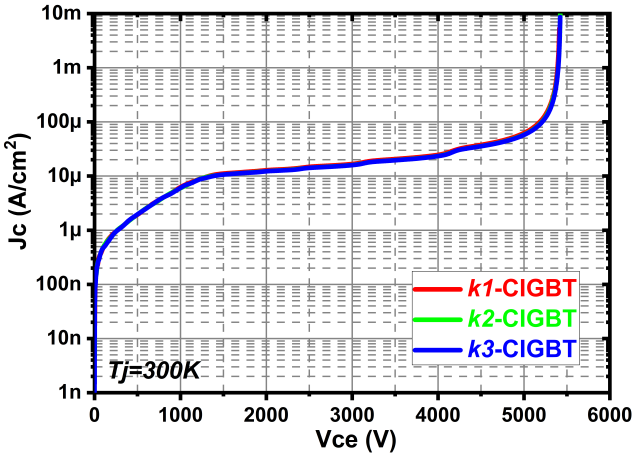

Fig. 7. Breakdown characteristics of the conventional and scaled CIGBTs.

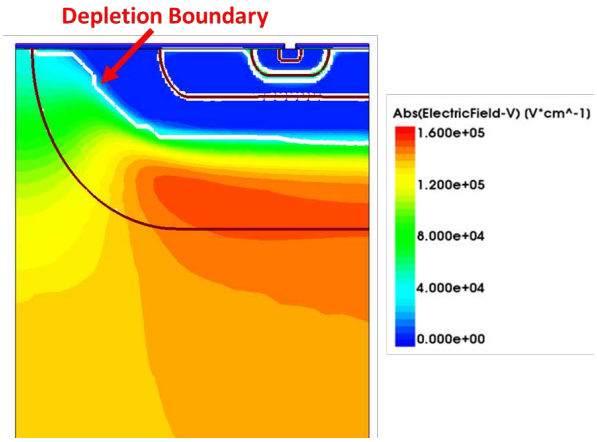

Fig. 8. Electric field distribution of the cathode side of *k1*-CIGBT at breakdown voltage (V_{ce} = 5400 V).

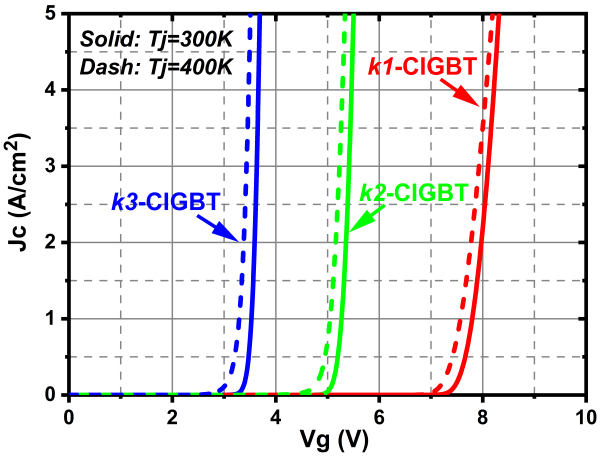

Fig. 9. Transfer characteristics of the conventional and scaled CIGBTs.

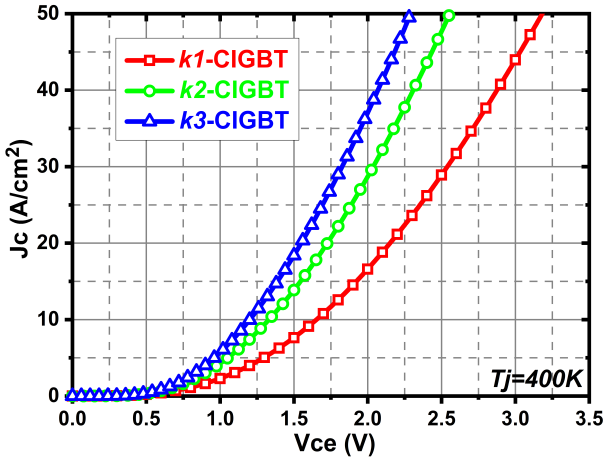

Fig. 10. I-V characteristics of the conventional and scaled CIGBTs.

potential is firstly supported by the P-base/N-well junction. After the N-well layer is punched through, the further increase in collector potential is supported by the P-well/N-drift junction. As a result, the MOS cells are protected from peak electric field, as shown in Fig. 8. As the collector voltage is mainly supported by the P-well/N-drift junction, scaling down cathode cells does not affect the breakdown characteristics.

B. Transfer Characteristics

Fig. 9 compares the transfer characteristics of the conventional and scaled devices. The threshold voltages measured at J_c = 100 mA/cm^2 and T_j = 300 K are shown in Table I. Due to the scaling rules on gate oxide thickness as well as channel length, the transconductance of the *k3*-CIGBT shows improvement compared to that of the *k1*-CIGBT.

C. I-V Characteristics

The comparison of I-V characteristics at T_j = 400 K is shown in Fig. 10. The *k3*-CIGBT can achieve low $V_{ce(sat)}$ (J_{rated} = 50 A/cm^2) of 1.78 V and 2.28 V at T_j = 300 K and T_j = 400 K, respectively, which are 22 % and 28 % lower than that of the conventional CIGBT. Furthermore, the individual components contributing to the on-state voltage drops are specified in Table II. The MOSFET voltage drop is considered to be the potential drop up to 15 μm from the surface. As shown, the MOSFET resistance is reduced in the scaled devices due to reduced channel resistance and JFET resistance as a result of scaling rules on MOS structure. Moreover, the reduction of voltage drop across N-drift region plays a significant role in improving the on-state behavior. This can be attributed to the increased current gain of the N-well/P-well/N-drift transistor (T_{npn}), which enhances the conductivity modulation within the N-drift layer. As the P-base depth is scaled down whereas the N-well depth is constant in the scaled CIGBTs, the N-well layer effective charge is dramatically increased, resulting in a greater emitter injection efficiency of the T_{npn}. Therefore, the thyristor

TABLE II: COMPONENTS OF ON-STATE VOLTAGE DROPS

T_j = 300 K	V_{MOSFET}	V_{drift}	V_{jun}	$V_{ce(sat)}$
k1-CIGBT (V_g = 15 V)	0.36	1.21	0.7	2.27
k2-CIGBT (V_g = 7.5 V)	0.27	0.96	0.7	1.93
k3-CIGBT (V_g = 5 V)	0.24	0.84	0.7	1.78

V_{MOSFET}: Voltage drop across MOSFET structure (consisting of channel layer, accumulation layer and JFET region).
V_{drift}: Voltage drop across N-drift region.
V_{jun}: Built in potential of P-anode/N-buffer junction.

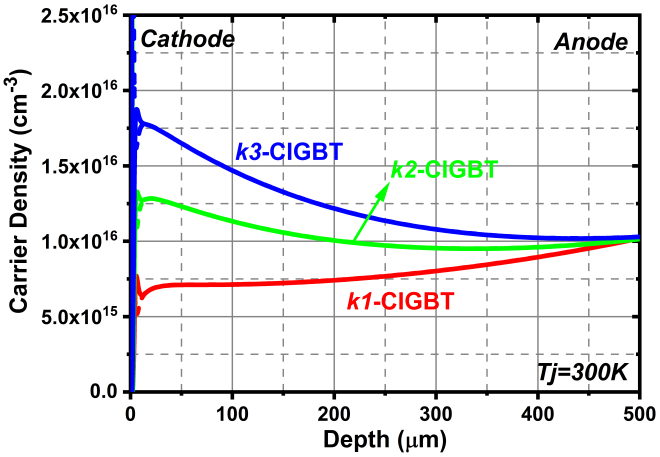

Fig. 11. Carrier distributions within the drift regions during on-state.

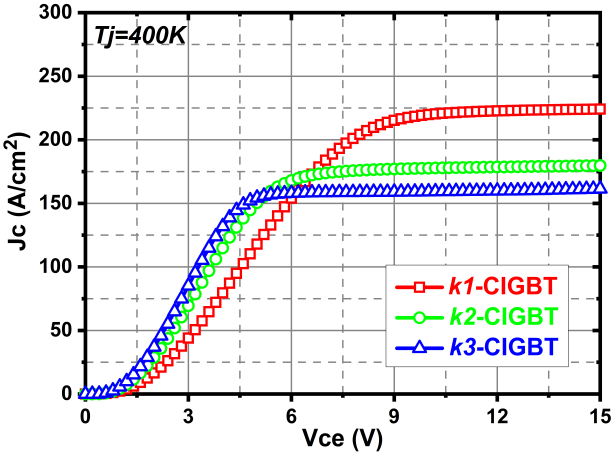

Fig. 12. Current saturation behavior of the conventional and scaled CIGBTs.

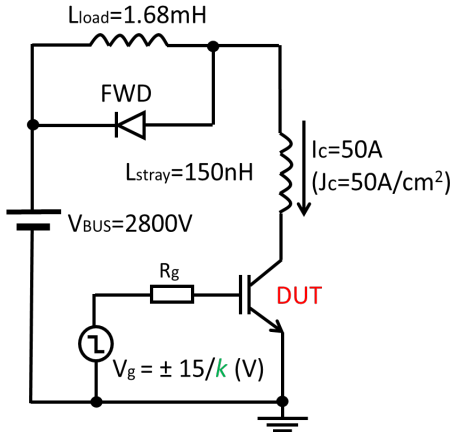

Fig. 13. Circuit configuration for inductive switching test.

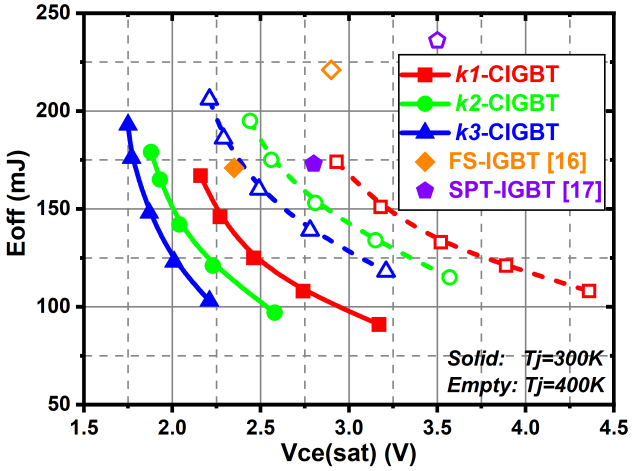

Fig. 14. $V_{ce(sat)}$-E_{off} trade-offs of the CIGBT devices and commercial IGBTs.

effect is significantly enhanced during on-state, leading to a much higher carrier distribution within the scaled devices, as shown in Fig. 11. It is worth mentioning that as specified in Table I, the electron injection efficiency (γ_e) does not change in the conventional and scaled devices. Therefore, IE effect is not involved in the improvement of on-state behavior. In addition, as depicted in Fig. 12, due to the optimization of the scaling factor for V_{th}, the J_{sat} of the *k3*-CIGBT is reduced to ~3 times of the rated current density at T_j = 400 K. Therefore, compared to the conventional CIGBT, a simultaneous reduction in $V_{ce(sat)}$ and J_{sat} can be achieved by the scaling rules.

D. Switching Characteristics

The switching characteristics are investigated with the mix-mode simulations and the circuit configuration is shown in Fig. 13. The $V_{ce(sat)}$ versus E_{off} trade-offs of the scaled CIGBTs with state-of-the-art commercial 4.5 kV IGBTs [16, 17] are depicted in Fig. 14. The $V_{ce(sat)}$ of the commercial devices are from the datasheets and the E_{off} is calculated at a current of 50 A. For identical E_{off}, the *k3*-CIGBT can achieve 20 % and 25 % reductions in on-state voltage drop compared to that of the conventional *k1*-CIGBT device at T_j =300 K and T_j = 400 K, respectively. In addition, the scaled CIGBTs show significant improvement of $V_{ce(sat)}$-E_{off} trade-offs even compared to the commercial IGBTs in trench and field-stop technologies. Therefore, the scaling work of the 4.5 kV CIGBT provides a more energy-efficient solution for high power electronics applications. In addition, the Reverse Bias Safe Operating Area (RBSOA) characteristics are shown in Fig. 15. The devices are turned off at T_j = 400 K and a current level of 150 A (~3 times of rated current). As shown, the scaled devices turn-off successfully without occurrence of Switching Self-Clamping Mode (SSCM). In the conventional high-voltage field-stop IGBTs, dynamic avalanche can be triggered during high currents turn-off [18]. The collector voltage is clamped after it raises to the peak value. This is due to the occurrence of dynamic avalanche at emitter side. The device will enter into SSCM after dynamic avalanche occurs, which is considered as a dangerous operation [19]. Increasing P-anode injection efficiency can compensate the excessive electrons caused by dynamic avalanche and suppress the turn-on of SSCM. However, this will increase the E_{off} and affect the short-circuit capability due to higher J_{sat} as a result of greater current gain of the internal PNP transistor. In contrast, CIGBTs can suppress the dynamic avalanche phenomenon during turn-off. This is because the increasing collector voltage is supported by the P-well/N-drift junction so that the MOS cells are isolated to the high electric field. The high ruggedness of the scaled CIGBTs

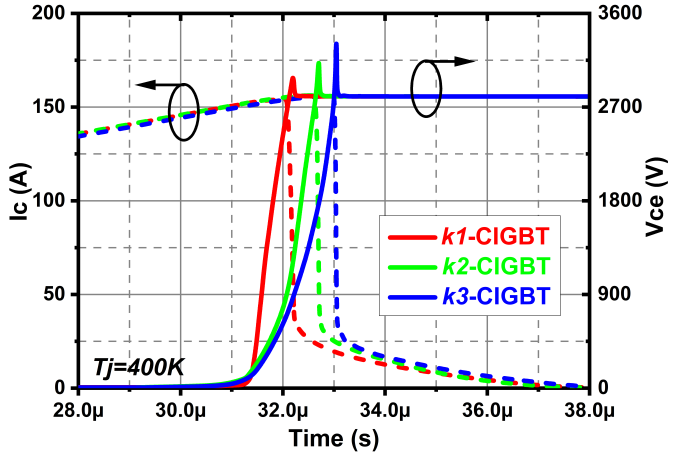

Fig. 15. RBSOA characteristics of the conventional and scaled devices.

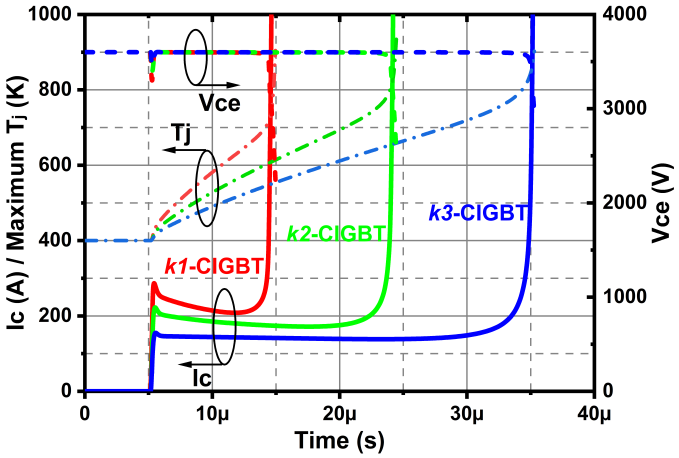

Fig. 16. Short-circuit performance of the conventional and scaled devices.

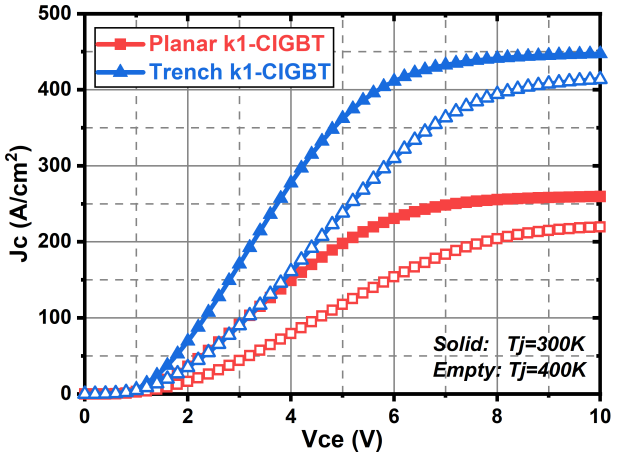

Fig. 17. Comparison of I-V characteristics between 4.5 kV planar CIGBT and 4.5 kV trench CIGBT. (V_g = 15V, τ = 50 μs)

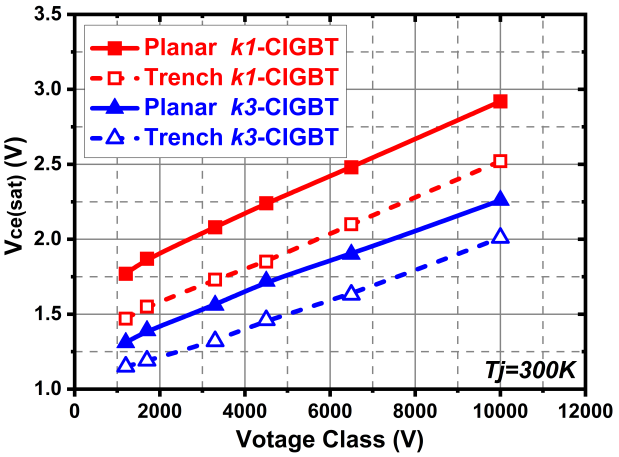

Fig. 18. On-state voltage drops of the conventional and *k3*-CIGBTs in both planar and trench technologies (τ = 100 μs).

enables the possibility to operate the devices under lower R_g, resulting in shorter switch-off delay time and lower E_{off}.

E. Short-circuit Characteristics

Fig. 16 shows the comparison of the short-circuit performance under high temperature. The DC bus voltage is raised to 3600 V and self-heating effect is considered in the simulations. During short circuit condition, the device has to support simultaneously high supply voltage and its saturation current for a defined period. As a result, the junction temperature increases dramatically with time due to excessive power dissipation. To improve the short-circuit withstand duration and reduce the power dissipation, one effective solution is reducing the saturation current level. As shown in Fig. 16, the *k3*-CIGBT significantly improves the short-circuit withstand duration due to the reduced J_{sat}. Therefore, a wider Short-Circuit Safe Operating Area (SCSOA) is achieved by the proposed 3-D scaling rules without penalizing $V_{ce(sat)}$.

IV. Comparison with IGBT Performance Limit

Fig. 17 compares the I-V characteristics of the 4.5 kV planar CIGBT and the 4.5 kV trench-gate CIGBT (TCIGBT). Compared to the trench CIGBTs, planar CIGBTs can provide higher switching frequencies due to lower E_{off} as well as wider Forward Bias SOA (FBSOA) and SCSOA due to lower J_{sat}. However, in terms of on-state behavior, trench CIGBTs are superior to planar CIGBTs due to elimination of JFET resistance and IE effect. Therefore, the on-state voltage drops are expected to be further reduced by applying the 3-D scaling rules to high voltage (≥ 3300 V) trench CIGBTs. Fig. 18 summarizes the $V_{ce(sat)}$ of the conventional and scaled CIGBTs in both planar and trench technologies. The $V_{ce(sat)}$ for medium voltage (≤ 1700 V) CIGBTs are the voltage drops at J_c = 200 A/cm² whilst the $V_{ce(sat)}$ for high voltage (≥ 3300 V) CIGBTs are the voltage drops at J_c = 50 A/cm². The planar CIGBTs employ the scaling rules proposed in this work while the trench CIGBTs use the scaling rules proposed in [13]. To support the rated breakdown voltage, the N-well and P-well depths of high voltage (≥ 3300 V) trench CIGBTs are kept constant. As shown in Fig. 18, a 20 % reduction of $V_{ce(sat)}$ can be achieved by the scaling rules for both planar and trench CIGBTs. In addition, the trench *k3*-CIGBTs display a 10 % improvement in forward voltage drop compared to the planar *k3*-CIGBTs.

Fig. 19 compares the specific on-resistances ($R_{sp,on}$) of the *k3*-TCIGBTs with the state-of-the-art IGBT technologies [20-24], scaled trench IGBTs [9, 10] and the IGBT theoretical limit [25]. The carrier lifetime for the simulations is set as 100

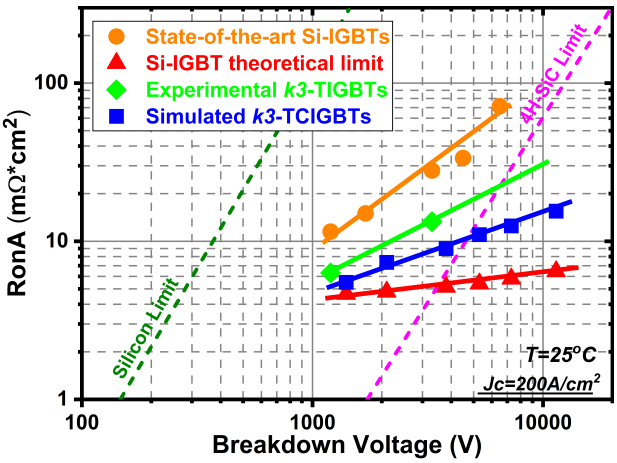

Fig. 19. Comparison of k3-TCIGBTs with novel IGBT technologies, SiC MOSFETs and IGBT performance limit.

μs. As shown, the *k3*-TCIGBTs show significant improvement in $R_{sp,on}$ compared to the latest IGBT technologies. The $R_{sp,on}$ of the *k3*-TCIGBTs are close to the theoretical limit in the cases of medium voltages (< 3300 V) while the difference at high voltages (> 3300 V) is mainly due to recombination of carriers within thick N-drift layers. Furthermore, Fig. 19 shows that the $R_{sp,on}$ of the *k3*-TCIGBTs can outperform the 1-D 4H-SiC unipolar limit when breakdown voltage is higher than 5 kV.

V. CONCLUSION

The 3-D scaling rules for high voltage planar CIGBTs are investigated through TCAD simulations. Detailed simulation results of a 4.5 kV CIGBT show that the scaling rules result in significant improvement in on-state behavior and $V_{ce(sat)}$-E_{off} trade-off. Moreover, the short-circuit withstand capability is increased by more than three times to achieve a much wider SOA. More importantly, compared to the state-of-the-art IGBT technologies, the scaled TCIGBTs exhibit significant improvement of on-state performance. Therefore, the 3-D scaling rules provide an excellent approach of design optimization for improving the overall performance of high voltage CIGBTs.

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