



Research article

Carrier-based sinusoidal pulse-width modulation techniques for flying capacitor modular multi-level cascaded converter

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ABSTRACT

Carrier-based sinusoidal pulse-width modulation (PWM) techniques, such as phase disposed PWM (PD-PWM) and phase shifted PWM (PS-PWM), are widely applied to control the modular multilevel cascaded converters (MMCC) having full H-bridge as sub-modules. This paper evaluates these PWM techniques when controlling a variant of the H-bridge MMCC, i.e. the MMCC five-level flying capacitor converter as sub-modules. This MMCC poses an extra challenge to PWM schemes; namely maintaining two inner floating capacitor voltage balancing. Two novel PWM techniques known as the swapped carrier PWM techniques are introduced for the control of this converter. The paper compares them with the two conventional ones using a performance metrics composed of voltage waveform performance, capability in natural flying capacitor voltage balancing, converter power loss, and switch utilisation. The results show that the proposed new PWM schemes outperform both conventional methods in both switching and conduction power losses and achieve similar performance like the PS-PWM under the three other metrics.

1. Introduction

Recent trend in the widespread integrations of renewable energy sourced generators in existing power grid and interconnection of power networks has resulted an increasing demand for medium and high-power converters. Multilevel converters, particularly modular multi-level cascaded converters (MMCC) offer great advantages to high voltage transmission and distribution networks, hence have received a widespread interest [1, 2, 3]. Classical multiple level converters such as neutral point clamped (NPC), or flying capacitor (FC) converters present different challenges when more levels are added to meet the high voltage requirement. For example a 5-level NPC poses challenges of balancing the neutral point voltage and device power losses resulting from its neutral point clamping diodes [4, 5]. For an FC converter, there is difficulty in balancing capacitor voltages when the number of clamping capacitors increased for higher voltage output. The cascaded H-bridge converter (CHB) using the three-level full bridge (3L-FB) as the basic module overcomes the limitations of the above two converters. This has led to the MMCC [5, 6], which provides superior features of modularity, scalability, low harmonic contents in voltage waveforms at low switching frequencies. The MMCC has gained huge attention because of its vast

industrial application in grid-connected converters [7], static synchronous compensators [8, 9, 10], unified power flow controllers [11, 12, 13] and HVDC transmission system [14, 15, 16].

The choice of basic module type for an MMCC depends on the operation requirement. For example, the two-level half bridge (2L-HB) module are popular for HVDC application [15, 16] while the 3L-FB are for flexible AC transmission applications because they allow four quadrant power flow operation. Other module types currently investigated for MMCC topologies are the 5-level NPC, 5-level FC and their hybrid combinations. The 5L-FC module offers benefits of more switching states and voltage level per module, thus with the same number of modules as 3L-FB, the converter output voltage is higher and harmonic content better.

A fundamental challenge for MMCC control is the increased complexity of modulation schemes required for cascaded modules to generate discrete output voltage levels. Selective harmonic elimination techniques (SHE) [17, 18] applied to MMCCs, with the number of modules in the range of many tens, provide output voltage waveforms with very low harmonic contents and at very low switching frequencies. However, because of its computational complexity, SHE is not applicable for MMCC-based STATCOM and machine drives, having less numbers of

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voltage levels, but requiring fast dynamic control. Another widely used modulation technique is the multilevel space vector modulation, this provides extra utilization of the module DC capacitor voltages but poses a complicated modulation algorithm when applied to MMCC [19, 20, 21].

Currently, MMCCs are mainly controlled by sine-triangle PWM [22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32] schemes because of their simplicity in implementation and good waveform quality. Typical ones include the phase shifted PWM (PS-PWM), the phase disposition PWM (PD-PWM) and their variants such as phase opposition disposition (POD), alternative phase opposition disposition (APOD) PWMs [33]. Extensive work has been done in applying the basic two methods for MMCCs having either 2L-HB or 3L-FB as the basic sub-modules, and it has been established that PD-PWM is the most preferred technique due to its resultant low power losses and good waveform quality [31].

This is to ascertain which of the large number of possible implementations of multilevel sine-triangle PWM is the optimum for a flying-capacitor inverter. However, very few investigations have been done on the optimum type of PWM schemes for an MMCC using 5L-FC as the basic sub-module [34]. The main requirement for a suitable PWM method is that it can maintain voltages of the sub-module clamping capacitors balanced under all operating conditions [22, 35, 36, 37, 38]. Sadigh et al. [39, 40] presented a detailed power loss analysis for sub-modules formed by hybrid FC and NPC converters irrespective of the modulation method. Authors in [34] provided comparisons between three different sine-triangle PWM schemes for a FC-based MMCC in terms of waveform performance and power losses. The work established that the PD-PWM gives poorer waveform performance in terms of THD values and higher losses due to flying capacitor equivalent series resistance (ESR) losses resulting from high voltage fluctuation, while PS-PWM gives higher switching losses due to its high equivalent switching frequency.

This paper presents novel swapped carrier PWM techniques for an MMCC with 5L-FC as sub-modules. This is to address the limitations posed by the PD-PWM and PS-PWM techniques. In addition, the performance of PS-PWM, PD-PWM and the novel PWMs are compared comprehensively under metrics of natural flying capacitor voltage balancing, power losses consisting of switching loss, conduction loss, and flying capacitor loss, waveform quality (THD) and switch utilization. This study uses models of a practical implementation to ensure simulate as accurately as possible the complete system's performance.

The paper is organised as follows; section 2 presents the FC-MMCC and 5L-FC module. In section 3, the metrics for analysing the performance of the various PWM techniques are discussed, a review of carrier-based PWM (i.e. PD-PWM and PS-PWM) are presented in section 4. In section 5, the novel PWM techniques are presented. In section 6, the various PWM method are compared and contrasted under the same conditions.

2. Flying capacitor modular multilevel cascaded converter

The circuit diagram of a flying capacitor MMCC used for evaluating the PWM techniques is shown in Figure 1. It uses a five-level flying capacitor H-bridge as the basic sub-module, which is formed by connecting two three-level FC half bridges sharing one capacitor C_{SM} known as the sub-module capacitor. Further splitting this FC sub-module, there are 4 switch cells; cells 1A and 1B consist of complementary switch pairs $S_{a1}:S_{a4}$ and $S_{b1}:S_{b4}$ having C_{SM} connected across them, while 2A consists of switch pairs $S_{a2}:S_{a3}$ with inner capacitor C_A and 2B has switch pair $S_{b2}:S_{b3}$ and inner capacitor C_B connected across them. Six such FC sub-modules are used to form a three-phase bridge; two are cascaded per phase and the three-phase limbs are connected in a single star configuration. The sub-module capacitor and inner capacitors are rated at V_{DC} and $0.5V_{DC}$ respectively. Each five-level flying capacitor H-bridge generates five voltage levels of V_{DC} , $0.5V_{DC}$, 0 , $0.5V_{DC}$ and $-V_{DC}$. Each of the three-level FC half bridges has four operating states 1100, 0101, 1010 and 0011.

3. Performance metrics for analysing FC-MMCC modulation techniques

In analysing the performance of the carrier-based modulation techniques to be applied in controlling the FC-MMCC, the following metrics are considered;

3.1. Natural flying capacitor voltage balance

Ideally, under steady-state conditions, the inner capacitor voltages of the FC-MMCC should be self-balanced. This is achieved by having the converter cell capacitors exchanging zero net active power with the AC side over one or several fundamental cycles. However, the net charges of the inner flying capacitor voltages may not be zero, thus, causing voltage deviations or drift from their nominal value (see Figure 2). The capacitor voltage deviation depends on the capacitance value of the inner flying capacitor, the switching frequency and importantly the pulses synthesized by the modulation technique.

Natural voltage balancing of inner flying capacitors, i.e. C_A and C_B , is an important attribute for evaluating PWM schemes regulating FC-MMCC. Severe voltage deviation and drift from its required levels in the inner flying capacitor will increase the harmonic distortion of the converter output voltage.

3.2. Power loss

Power losses of an MMCC are mainly due to the conduction and switching losses of the switching devices (power IGBTs and diodes). Two

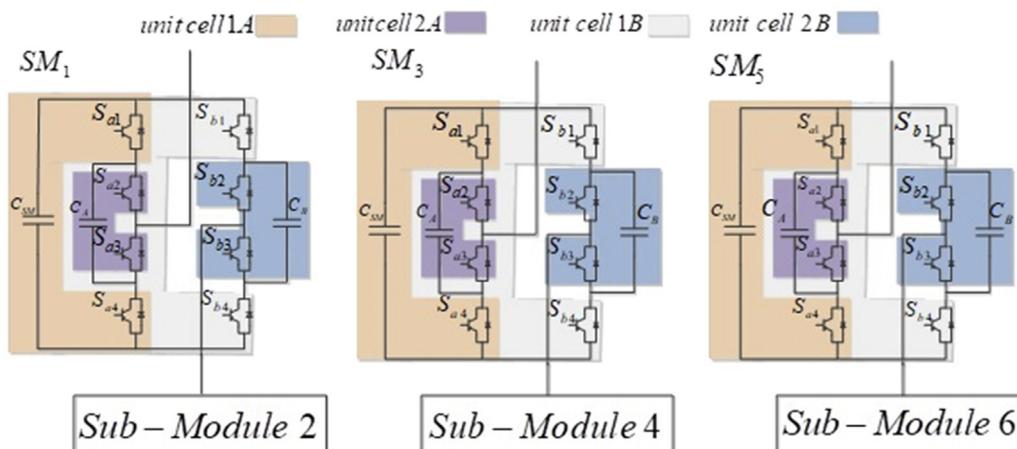


Figure 1. FC-MMCC circuit structure.

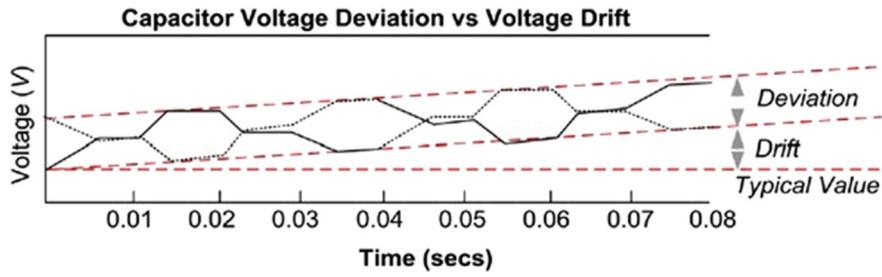


Figure 2. Graphical illustration of capacitor voltage drift and variation.

methods have been applied to calculating them. One uses a mathematical model of the current waveform in each switch [41] and the other an average model based on piecewise linear characteristics of semiconductor devices obtained from the manufacturer's datasheet [42, 43]. In this paper, a more accurate method of evaluating the power losses is applied. This incorporates the instantaneous current through the switches and their respective instantaneous junction temperature of each device in their evaluation. Losses due to flying capacitor equivalent series resistance (ESR) are also included in this analysis. This method has been extensively presented in [34, 38].

3.3. Total harmonic distortion (THD)

This metric is used to assess the output voltage waveform performance. The THD of a voltage waveform primarily depends on the PWM methods used and switching frequency. This is defined as:

$$THD = \sqrt{\sum_{n=2,3,\dots} (V_n/V_1)^2} \quad (1)$$

Where V_1 and V_n refer to the RMS values of the fundamental and n^{th} harmonic component present in the converter output voltage. For this analysis, the unipolar switching method is applied to all PWM methods presented.

In analysing the spectrum quality of the FC-MMCC output voltage, the Fourier series of the instantaneous voltage signal $v(t)$ generated by the carrier placement scheme is used [32]. This is expressed as:

$$v(t) = \underbrace{0.5a_{00}}_{1st \text{ Term (DC offset)}} + \underbrace{\sum_{n=1}^{\infty} [a_{0n} \cos(n(\omega_0 t + \phi_0)) + b_{0n} \sin(n(\omega_0 t + \phi_0))]}_{2nd \text{ Term (Fundamental+Baseband harmonics)}} + \underbrace{\sum_{m=1}^{\infty} [a_{m0} \cos(m(\omega_c t + \phi_c)) + b_{m0} \sin(m(\omega_c t + \phi_c))]}_{3rd \text{ Term (carrier harmonics)}} + \underbrace{\sum_m \sum_n [a_{mn} \cos(m(\omega_c t + \phi_c) + n(\omega_0 t + \phi_0)) + b_{mn} \sin(m(\omega_c t + \phi_c) + n(\omega_0 t + \phi_0))]}_{4th \text{ Term (sideband harmonics)}} \quad (2)$$

Where a_{00} represents the amplitude of the DC offset and is zero for all modulation strategies investigated in this paper.

a_{0n} and b_{0n} , are for reference fundamental component and its harmonics with index n , and often refer as the baseband harmonics. a_{m0} , b_{m0} and a_{mn} , b_{mn} represent the amplitudes of carrier and sideband harmonic components, where n and m represent the index variables for the baseband and carrier harmonics.

$\omega_0 = 2\pi/T$ and $\omega_c = 2\pi/T_c$ are the reference and carrier signal angular frequencies, ϕ_0 and ϕ_c phase shifts of the reference and carrier signals.

According to (2), the first term is zero, the second term represents the fundamental component surrounded by baseband harmonics. Ideally, for carrier placement methods, all baseband harmonics before the equivalent carrier switching frequency are totally suppressed except the

fundamental signal. The third term is the harmonic element at carrier signal frequency and its multiples. The fourth term is the sideband harmonics resulting from the difference between the carrier and baseband harmonic components.

3.4. Sub-module switch utilization

This metric is used to investigate whether the switches within a sub-module under a particular PWM scheme are evenly stressed/used over a fundamental period. If some switches are more stressed within a sub-module, these switches will be more prone to failure.

To analyse the performance of the two proposed methods and the PS-PWM, PD-PWM techniques under the above four metrics, each was tested in a digital simulation environment of PLCES and SIMULINK. The parameters for this investigation are given in Table 1.

4. Review of carrier placement pulse width modulation techniques

Detailed research has been carried out over the years on the carrier placement-based pulse width modulation techniques for multilevel converters [32, 44]. These are broadly grouped into vertical and horizontal placement schemes, called the phase disposition PWM and Phase shift PWM respectively.

4.1. Phase disposition PWM (PD-PWM)

This is also called the level shift PWM, which involves displacing the

triangular carriers vertically according to the voltage levels. The number of the triangular carriers used is determined by the number of distinct voltage levels m_L minus 1 i.e. (m_L-1) . For the five-level FC-MMCC, four triangular carrier signals are used. The four level-shifted carriers are all in phase and equally spaced from -1 to +1. They are compared with two

Table 1. MMCC five-level flying capacitor converter sub-module Parameters.

Components	Description
R-L Load	15 Ω - 20mH
Flying capacitance C_A , C_B and Voltage	C = 560 μ F, E.R.S. = 0.266 Ω , 50V
DC sub-module Voltage	100V
IGBT module	Infineon F4-50R06W1E3 $V_{CE,REF} = 600V$

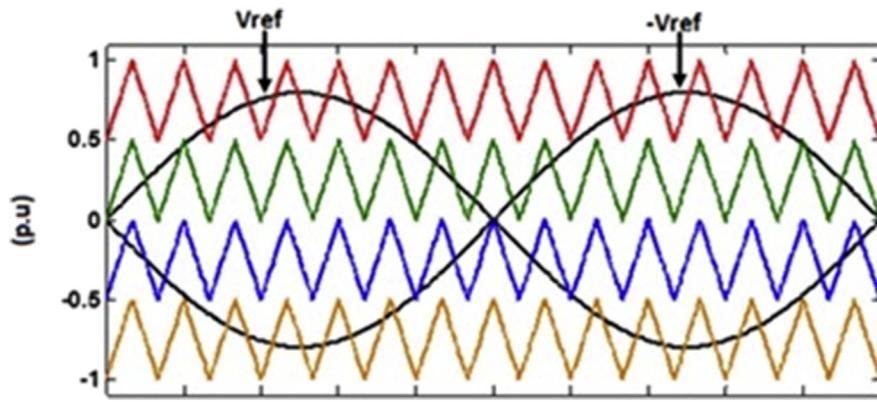


Figure 3. Phase disposition PWM for FC-MMCC at $m_f = 15$.

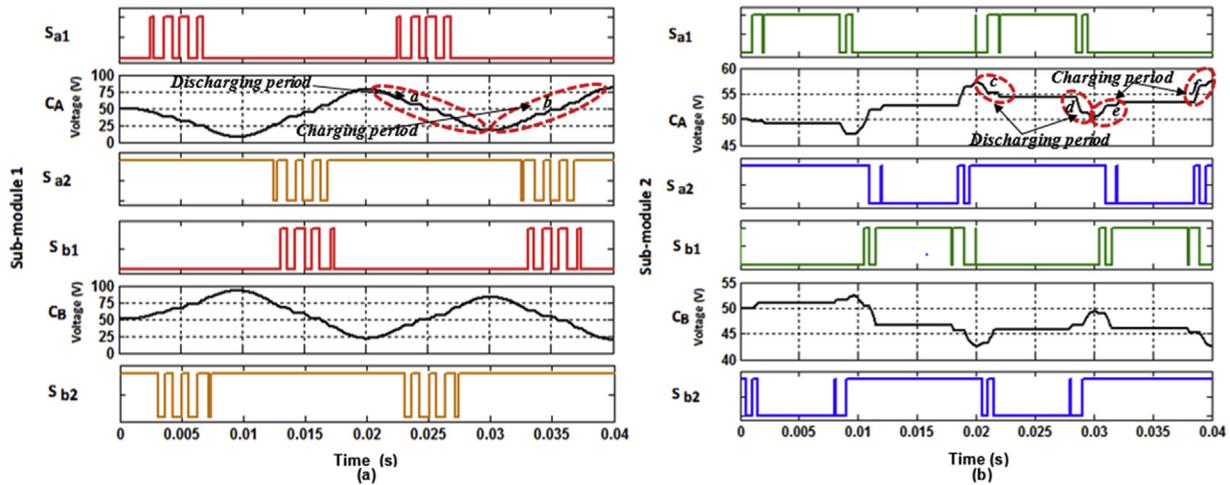


Figure 4. PD-PWM switching signals and sub-module inner flying capacitor voltage variations for (a) sub-module 1 and (b) sub-module 2.

reference signals which are phase shifted by 180° and with the same magnitudes and frequency. The PD-PWM scheme implemented for phase A of the FC-MMCC is illustrated in Figure 3. The four carrier signals are compared with two sinusoidal reference signals with their respective magnitudes $+V_{ref}$ and $-V_{ref}$. Frequency modulation index $m_f=15$, and amplitude modulation index $m_a=0.8$ are applied. The resultant pulse signals are applied to control eight complementary switch pairs in the two chained FC sub-modules.

4.1.1. Natural voltage balancing ability

The inner flying capacitor voltage natural balancing ability of the FC-MMCC under this scheme is analysed. The voltage waveforms of these capacitors in sub-module 1, 2 and their corresponding switching signals are as shown in Figure 4a and b respectively.

Clearly the inner flying capacitors in both sub-modules experience equal charging and discharging durations, thus resulting in zero voltage drift over every fundamental cycle. However, the voltage deviation

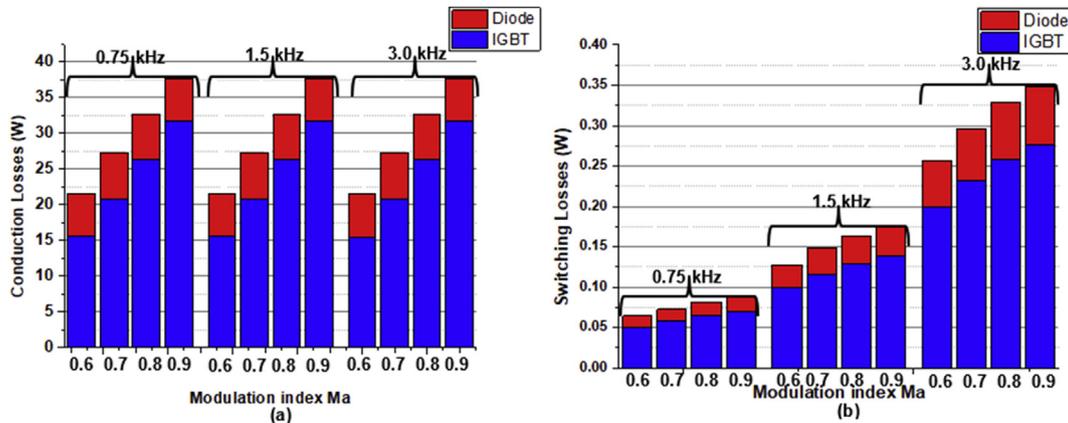


Figure 5. IGBT and Diode (a) conduction losses and (b) switching losses.

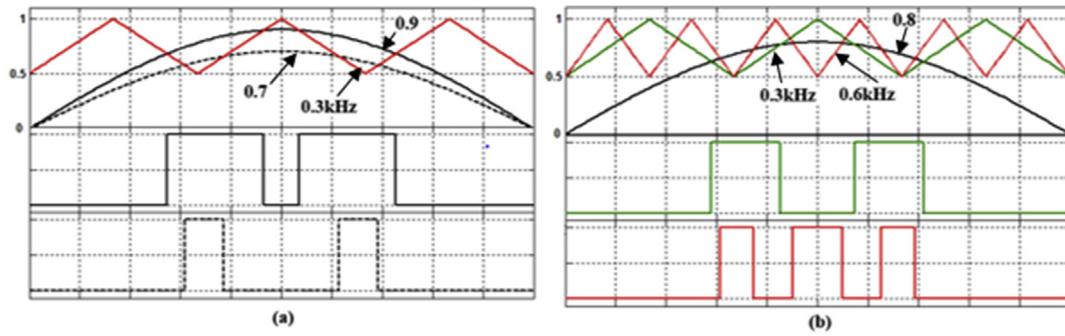


Figure 6. (a) Variation in reference signal m_a ; (b) variation in carrier signal frequency.

across each FC sub-module differs because of switching actions of switches, $S_{a1}:S_{a2}$ and $S_{b1}:S_{b2}$, in each sub-module. For sub-module 1, the mean voltage deviation is about $\pm 70\%$ because, over each half fundamental cycle, the pulses applied across S_{a1} ($=0$), S_{a2} ($=1$) have longer durations which discharges and charges C_A in each half of the fundamental cycle. Whilst for sub-module 2, both C_A and C_B experience mean voltage deviation of about $\pm 8\%$, which is attributed by switches, $S_{a1}:S_{a2}$ and $S_{b1}:S_{b2}$, having shorter duration of charging and discharging states compared to longer periods when both switches are turned high (i.e. C_A and C_B are bypassed) over each fundamental cycle.

As a result of the large Flying capacitor voltage variation in sub-module 1, the spectral quality of the output voltage waveform is adversely affected. The performance of the natural voltage balancing of the flying capacitors makes this method undesirable for FC-MMCC.

4.1.2. Power losses

4.1.2.1. Conduction loss. As seen in Figure 5a, modulation index affects both IGBT and diode conduction losses in different ways, i.e. when m_a increases, the conduction periods of the IGBTs increase, while those of the diodes reduce (see Figure 6a). Thus, the ratio of the diode to IGBT conduction losses decreases. It is also observed that, for the same reference magnitude, increasing the switching frequency has no impact on the conduction loss occurring in the IGBTs and diodes. As illustrated in Figure 6b, the conduction losses for the same m_a at carrier frequencies $f_s = 0.75$ KHz, 1.5 KHz and 3.0 KHz are the same.

4.1.2.2. Switching loss. As observed in Figure 5b, FC-MMCC switching loss increases as switching frequency increases. The number of switching transitions increases by a factor of 2 as the switching frequency increases from 0.75 KHz to 1.5 KHz (see Figure 6b). Also, as modulation index

increases for a fixed switching frequency, the number of switching transitions remains the same, see Figure 6a. The diode switching loss is nearly about 25% of the IGBT switching loss as seen in Figure 5b.

4.1.2.3. Flying capacitor losses. Due to the difference in voltage deviations between the inner flying capacitors of sub-modules 1 and 2, the power dissipations in both are unequal as seen in Figure 7a. It can be seen that the area of the charge/discharge region of each sub-module inner capacitor (see Figure 4) has a direct relationship with the power loss.

4.1.2.4. Total loss. As observed in Figure 7b, as m_a increases, the total power loss increases, which is mainly contributed by IGBT conduction losses. Likewise, the increase in total loss is only accounted for by the IGBT and diode switching losses as switching frequency increases. In addition, the power loss contribution of the IGBTs, diodes and inner floating capacitors with respect to the total loss are 60%, 15% and 25% respectively.

4.1.3. Total harmonic distortion (THD) analysis

For this method, it ideally gives a good harmonic performance when three-level H-bridge sub-modules are used. However, if using the five-level FC H-bridge sub-modules, the flying capacitor voltages deviate too far from their nominal values causing the poor spectral quality of the output voltage waveform. Figure 8a shows the ideal phase voltage waveform with $m_a=0.8$ and $m_f=15$. From the harmonic spectrum of the phase voltage shown in Figure 8b, it can be seen that all baseband harmonics and harmonics at twice the switching or carrier frequency and its multiples are suppressed except the fundamental and sideband harmonics due to the unipolar switching. These sideband harmonics frequencies are expressed as:

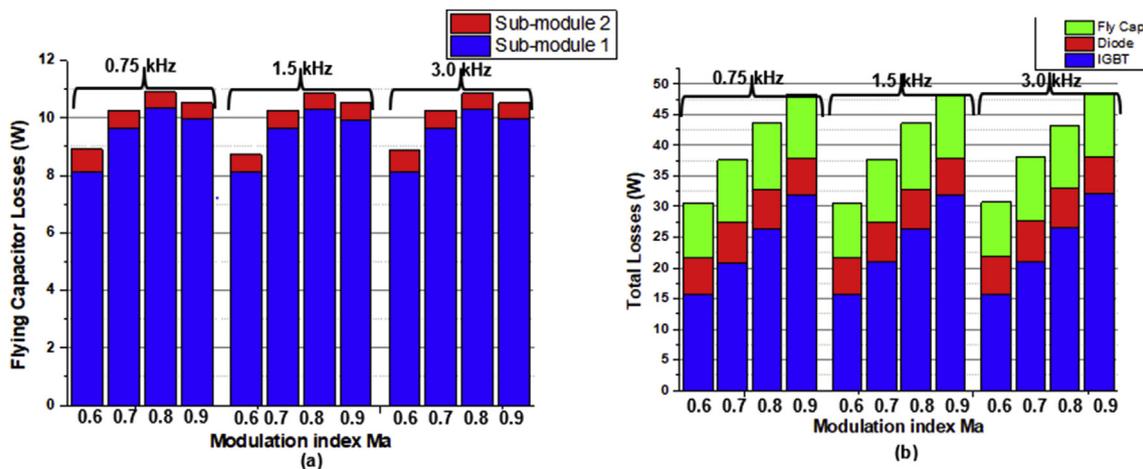


Figure 7. Power losses (a) Flying capacitor and (b) Total loss.

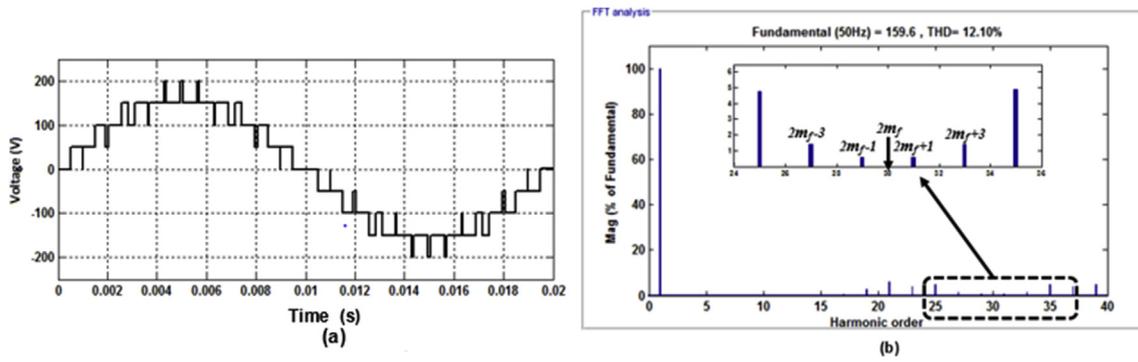


Figure 8. Ideal phase voltage (a) waveform and (b) spectrum of PD-PWM.

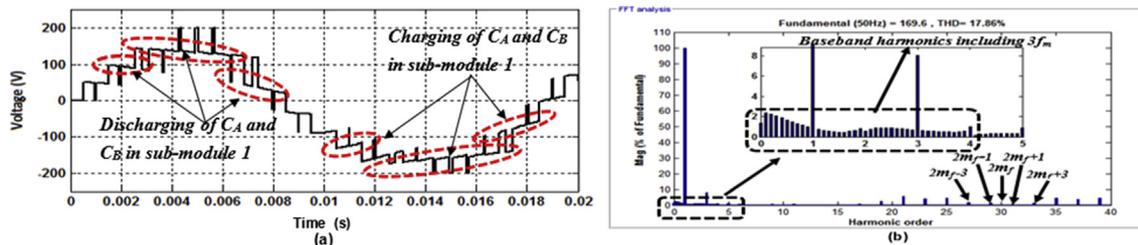


Figure 9. Phase voltage of the FC-MMCC (highlighting the intermediate voltage levels that are contributing to the distortion of voltage waveform) (a) waveform and (b) spectrum.

$$f_n = h \times f_0 = (j2m_f \pm k)f_0 \tag{3}$$

Where $j = 1, 2, 3 \dots k = 1, 3, 5 \dots$ odd number.

The total harmonic distortion of the phase voltage waveform is 12.10%. From Figure 8b, the first sidebands before and after the $2m_f$ are evaluated using (3) as:

$$f_{29} = ((2 \times 15) - 1) \times 50 = 1450\text{Hz} \text{ and } f_{31} = ((2 \times 15) + 1) \times 50 = 1550\text{Hz} \tag{4}$$

However using PD-PWM to control a nine-level FC-MMCC, the phase voltage waveform and spectrum are shown in Figure 9a and b respectively. The phase voltage spectrum has some baseband harmonics around the fundamental. These are introduced by the large voltage deviation of the flying capacitors C_A and C_B of sub-module 1, hence creating distortions on the output voltage waveform having a THD of 17.86%. The sideband harmonics (*i.e.* for phase voltage spectrum) appear around the carrier frequency as shown in Figure 9b.

4.1.4. Sub-module switch utilization

It is seen in Figure 4, that the conduction periods are different for each sub-module switch, and hence the conduction losses are different for different switches. From Figure 10, switches S_{a1}, S_{a3} show less conduction loss than S_{a2}, S_{a4} . This uneven switch utilization across the 5L-FC sub-module affects the charging and discharging of the sub-module capacitors, making this topology unattractive for active power filtering and FACTS application. The unequal utilization also results in uneven heat distribution across sub-module switches.

4.2. Phase shifted PWM (PS-PWM)

This is also known as horizontal displacement PWM. This involves the use of multiple triangular carriers which equally phase or time shifted from each other along the horizontal axis. The number of carriers N_T required by this technique is given by the number of voltage levels m_L , minus 1. For the two sub-module cascaded FC-MMCC, four triangular

carrier signals are required in total; two for each sub-module (*i.e.* for unipolar switching). The constant phase angle delay α_c between carriers is expressed as:

$$\alpha_c = 180^\circ / N_T \tag{5}$$

Where N_T is the total number of triangular carriers and in this case it is 4, so $\alpha_c = 45^\circ$.

The PS-PWM scheme implemented for the FC-MMCC in one phase limb is illustrated in Figure 11. The four phase-shifted carrier signals are compared with the two anti-phased reference signals V_{ref} and $-V_{ref}$ to synthesize switching signals.

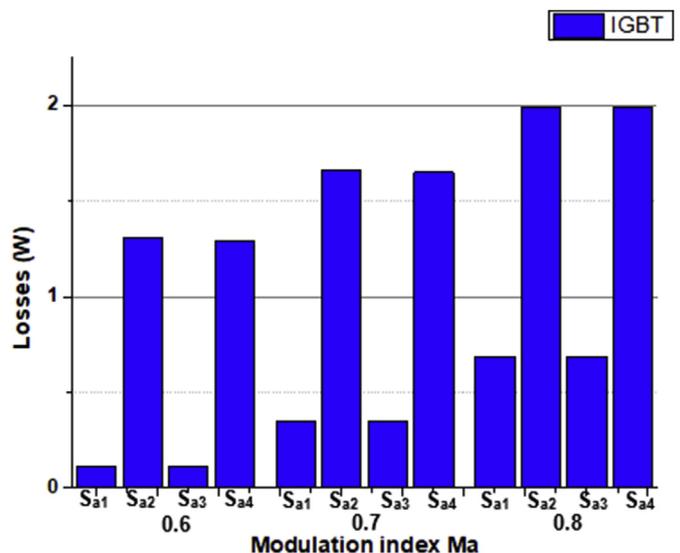


Figure 10. Sub-module Switch utilization conduction losses.

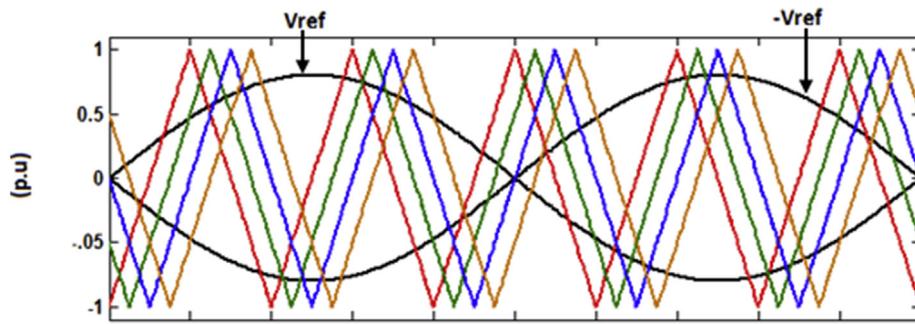


Figure 11. Phase shifted PWM for FC-MMCC at $m_f = 5$.

For sub-module 1, V_{ref} compared to triangular carriers 1 (Red) and 2 (Green) generates switching pulses to drive the complementary switches $S_{a1}:S_{a4}$ and $S_{a2}:S_{a3}$ and whilst $-V_{ref}$ compared with the same carriers leads to signals to drive switching pairs $S_{b1}:S_{b4}$ and $S_{b2}:S_{b3}$. In this case, the modulation frequency index $m_f=5$ is used and $m_a=0.8$.

4.2.1. Natural balancing ability

The balancing ability of the PS-PWM scheme for the inner flying capacitors is investigated using sub-module switching signals shown in Figure 12 for one reference cycle operation.

As observed in Figure 12, the switching patterns are symmetrical over a fundamental half cycle. This symmetry results from the repetitive nature of the switching signals over a fundamental cycle, thus resulting in the charging/discharging durations in each half modulating cycle to be equal having a zero-voltage drift (i.e. charge/discharge under area A = area B). Balance is assessed by considering whether the net charge transferred over one cycle is zero. In this example, the inner flying capacitor voltages deviate from their nominal values by $\pm 1.5\%$ per cycle. This small deviation is accounted by the bypass states of C_A and C_B far exceeding their charge/discharge operating switch states.

4.2.2. Power loss

4.2.2.1. Conduction loss. Similar relationships between conduction losses and m_a, m_f discussed for PD-PWM exist for the PS-PWM scheme, as seen in Figure 13a.

4.2.2.2. Switching loss. The switching loss of IGBT and diode increases by a factor of two as switching frequency increases by 2 as illustrated in Figure 13b.

4.2.2.3. Flying capacitor losses. The equal area of charge/discharge of each inner flying capacitor as shown in Figure 12 validates each sub-module flying capacitor experiencing equal power loss (see Figure 14a).

4.2.2.4. Total loss. The power loss contributions of IGBT, diode and the inner floating capacitor with respect to the total loss are 64%, 17.8% and 18.2% see Figure 14b.

4.2.3. Total harmonic distortion (THD) analysis

The FC-MMCC phase voltage waveform and frequency spectrum are shown in Figure 15a and b. For this analysis, $m_f = 15$. The harmonic orders in the spectrum of the phase output voltage are expressed below as:

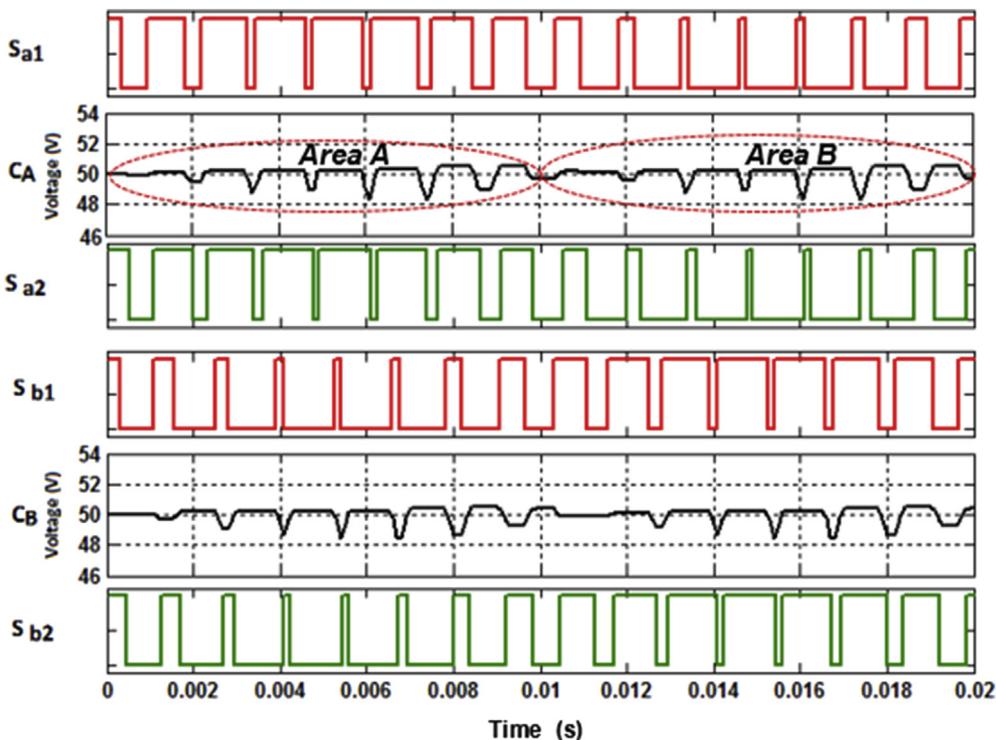


Figure 12. Phase shifted PWM switching actions for investigating sub-module flying capacitor variation.

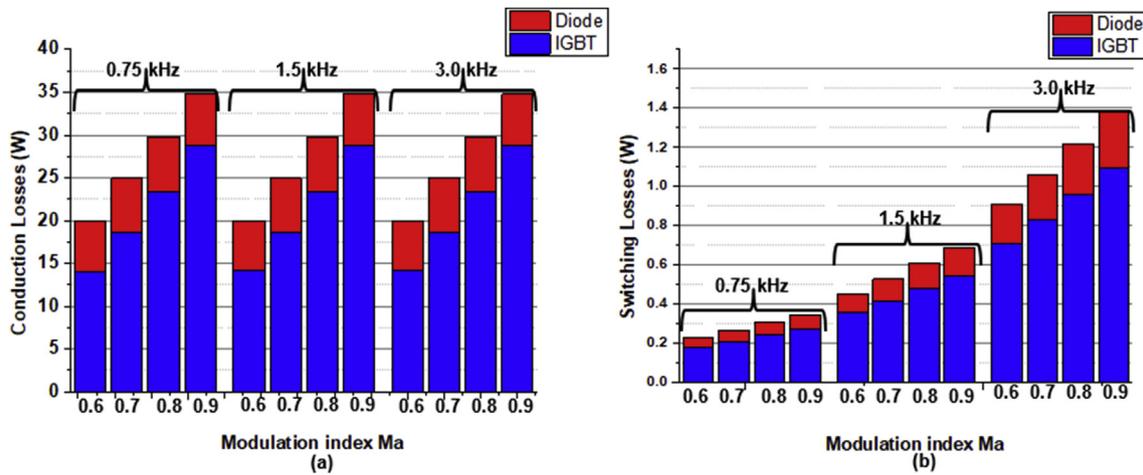


Figure 13. IGBT and Diode (a) conduction and (b) switching losses.

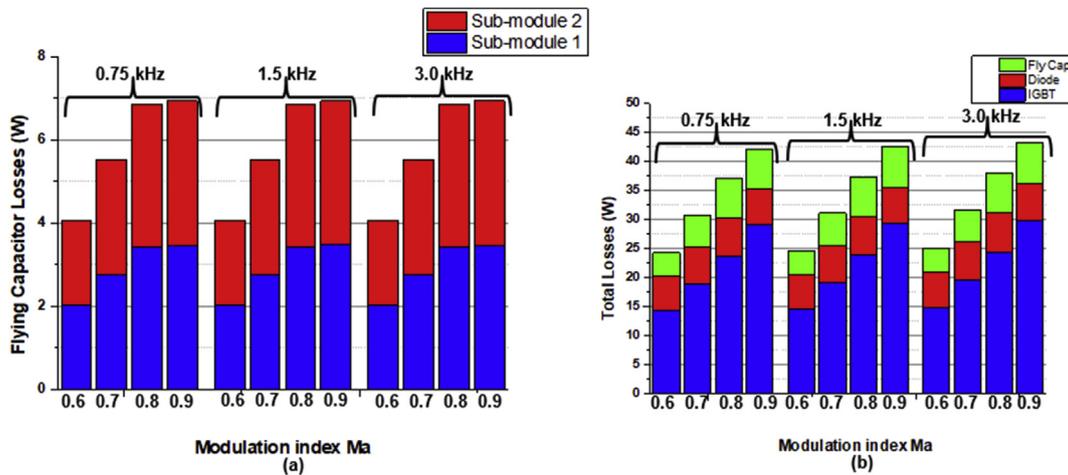


Figure 14. PD-PWM (a) Flying capacitor and (b) total losses.

$$\text{Phase voltage: } f_h = h \times f_0 = (j8m_f \pm k)f_0 \quad (6)$$

Where $j = 1, 2, 3 \dots k = 1, 3, 5 \dots$ odd number for phase voltage while for line voltage $j = 1, 2, 3 \dots k = 1, 5, 7 \dots$ odd number, excluding odd multiples of 3.

As seen from Figure 15b, all the baseband, and sideband around carrier harmonics are suppressed until the 8th multiple of the carrier frequency. This is because the four phase-shifted carriers and the two anti-phase reference signals make the equivalent switching frequency of the FC-MMCC to be eight times the cell switching frequency (i.e. $f_{sw} = 8 \times f_s$).

The THD for the phase voltage is 12.92%. For the phase voltage spectrum, all even harmonics are eliminated with sideband harmonics appearing around $8m_f$ and its multiples.

4.2.4. Sub-module switch utilization

From Figure 16, it is observed that the sub-module switches are equally utilized over every fundamental cycle. This is because the pulses applied in controlling the sub-module switches are identical, thus switches S_{a1}, S_{a2} and S_{b1}, S_{b2} across a sub-module experience equal conduction losses.

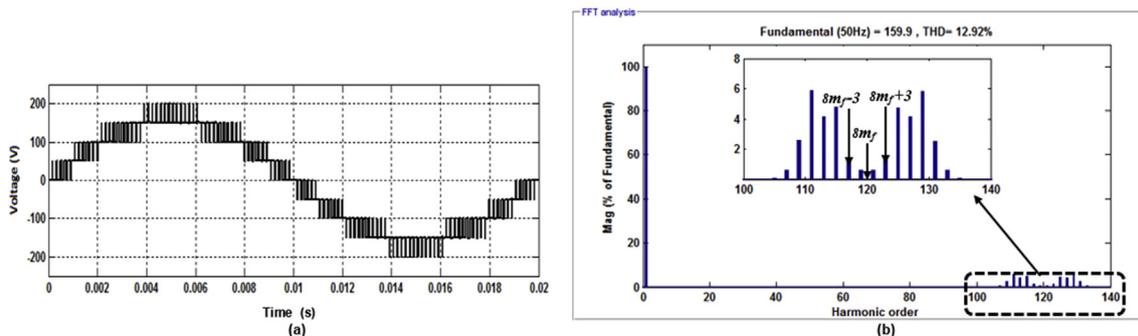


Figure 15. PS-PWM phase voltage (a) waveform and (b) spectrum.

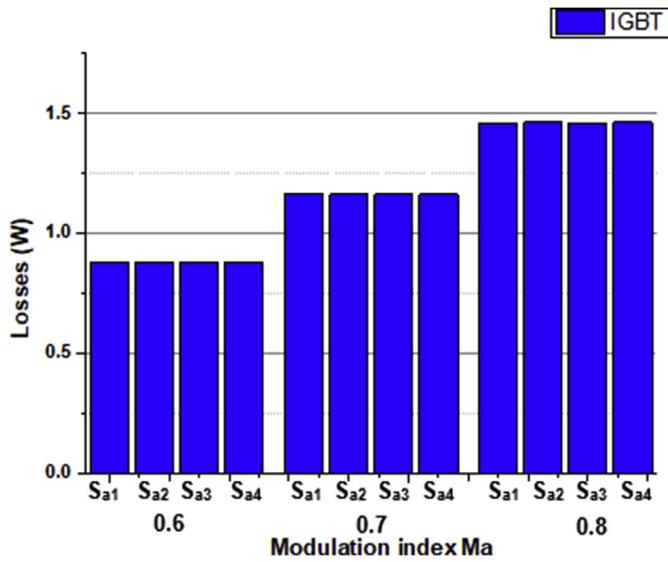


Figure 16. PS-PWM sub-module switch utilization conduction losses.

5. Swapped carrier PWM (SC-PWM)

In this method, the level of the carrier signals is rotated in an orderly manner either at the end of each quarter fundamental cycle named as method 1 or at the end of each carrier wave cycle as method 2.

The two anti-phase sinusoidal modulating signals are compared with four carrier signals. Carrier signals 1 and 2 control complementary switch pairs, $S_{a1}:S_{a4}$, $S_{b1}:S_{b4}$ and $S_{a2}:S_{a3}$, $S_{b2}:S_{b3}$ in sub-module 1, while carrier signals 3 and 4 are for switch pairs in sub-module 2. A modulation frequency index $m_f = 15$ is applied.

5.1. Method 1 - quarter fundamental cycle rotation

Figure 17 shows this method. The colour code in Figure 3 (PD-PWM) is maintained for uniformity. Here the two carriers, Red and Green, that lie above the x-axis and intersect with the positive reference $+V_{ref}$, are dedicated for sub-module 1 Left-Hand-Side (LHS) switches $S_{a1}:S_{a4}$ and $S_{a2}:S_{a3}$. They interchange their vertical positions after every quarter of the reference signal cycle ($T_m/4$). The other two carriers (Blue and Brown) lying below the x-axis, and also intersecting with $+V_{ref}$, are for sub-module 2 LHS switches S_{a1} and S_{a2} and changes positions at the same quarter cycle instants. This procedure is also applied to control sub-modules 1 and 2 RHS switches, $S_{b1}:S_{b4}$ and $S_{b2}:S_{b3}$.

This sequence of alternating positions is repeated for the other two carriers in the second (i.e. negative) half cycle. After the first fundamental cycle T_m , the two carrier signals, either above or below the x-axis are transposed, i.e. red (signal-1) shifts to level 2, green (signal-2) up to

level 1, blue (signal-3) down to level 4 and brown (signal-4) up to level 3. Then the quarter cycle swapping procedure applied during the first fundamental cycle is repeated. These two carrier rotational sequences (i.e. for signal-1, level 1 to level 2 first fundamental cycle and level 2 to level 1 s fundamental cycle) are repeated for every two fundamental cycles. The effect of this quarter cycle swapping is that it brings a phase shift equal to the duration $T_m/4$ between the two resultant adjacent pulse signals during each positive and negative half of the modulating signals.

5.2. Method 2- carrier cycle rotation method

The two carriers across the positive and negative of the reference signals swap their positions after each carrier cycle (T_c), namely the Red (carrier signal-1) and the green (carrier signal-2) swap their positions every carrier cycle (see Figure 18). The same applies to blue (carrier signal-3) and brown (carrier signal-4). This sequence of swapping positions is repeated for a fundamental cycle period T_m . At the beginning of the second fundamental cycle, the swapping sequence is transposed such that carrier signal-1 occupies the former position of carrier signal-2, carrier signal-2 occupies the former position of carrier signal-1. Likewise, carrier signal-3 and carrier signal-4 swap their previous positions at the first carrier cycle. These two carrier rotational sequences are repeated for every two modulating cycles. This method creates a phase shift equivalent to the duration T_c between the two adjacent carrier signals in controlling sub-module 1 and 2.

5.3. Natural flying capacitor voltage balancing

Using the switching signals generated by the above two carrier swapping PWM techniques, the natural voltage balancing ability of the FC-MMCC's inner flying capacitors is assessed over two modulation cycles. Figure 19a shows the switching signals for S_{a1} and S_{a2} , and those for S_{b1} and S_{b2} , together with the voltage waveforms of their corresponding inner capacitors, C_A and C_B when Method 1 is used. In Figure 19b the switching signals for the same pairs of devices and voltage waveforms of the same inner capacitors under Method 2 are displayed.

As observed from both sets of diagrams, the patterns of switching pulses for LHS S_{a1} and S_{a2} and those for RHS S_{b1} and S_{b2} are symmetrical except for the phase shifts over two fundamental cycles. Consequently if during the first fundamental cycle, the switching signals cause the inner flying capacitors to discharge, they would result in the same capacitors being charged during the second cycle, and vice versa. Also, the ampere-time products for charging and discharging intervals would be equal, making the voltage drift to be zero.

For the quarter cycle rotational method as shown in Figure 19b, it is observed that due to spreading the carrier swapping sequence over a half of the modulating signal cycle, the inner flying capacitors voltages rise by +35% during the first fundamental cycle and fall by the same percentage during the second. This same swapping sequence is implemented for the

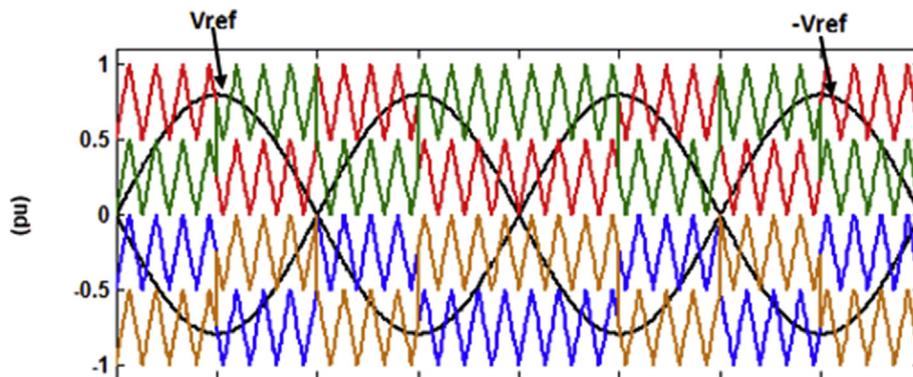


Figure 17. Quarter fundamental cycle rotation method for FC-MMCC.

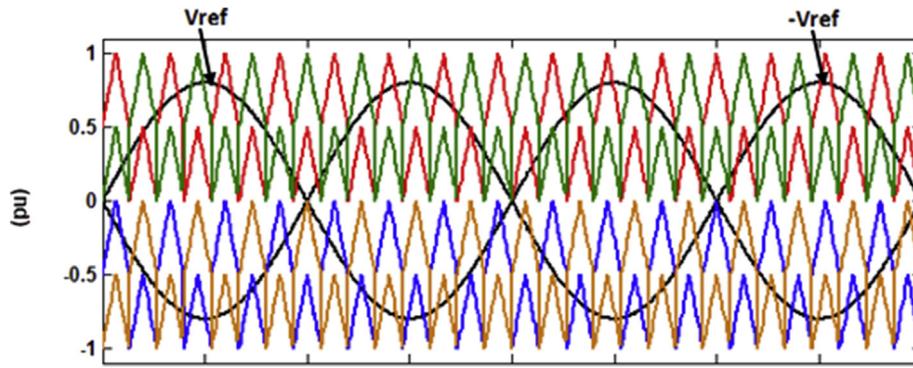


Figure 18. Carrier cycle rotation method for FC-MMCC.

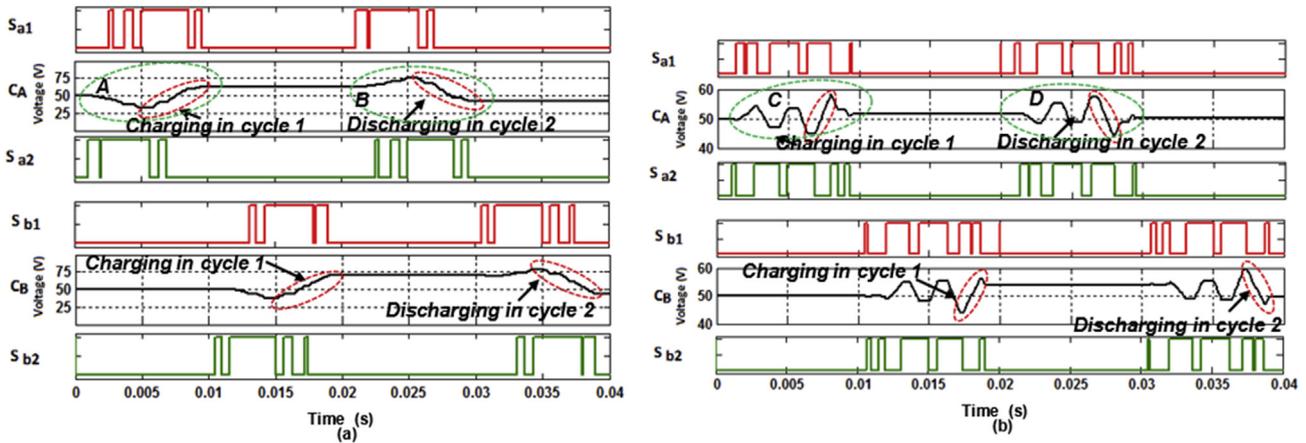


Figure 19. Sub-module flying capacitor voltage variation investigation (a) Quarter cycle rotation PWM and (b) Carrier cycle rotation PWM.

carrier cycle rotation method, causing the inner capacitors to deviate by $\pm 8\%$ under both fundamental cycles. The differences in capacitor voltage deviation between these two methods are due to the durations of the switches in states causing C_A and C_B bypassed. In contrast, the PD-PWM scheme experiences longer durations of charging and discharging switch states, hence giving significantly higher voltage fluctuations, as shown in Figure 4, compared to the Swapped Carrier-PWM methods.

5.4. Power loss

5.4.1. Conduction loss

As observed across Figure 20a and b, the carrier Method-2 experiences more conduction periods than the Method-1 quarter cycle PWM corresponding to conduction losses of 27.90W and 29.65W respectively at $f_s = 0.75\text{kHz}$ and $m_a = 0.8$.

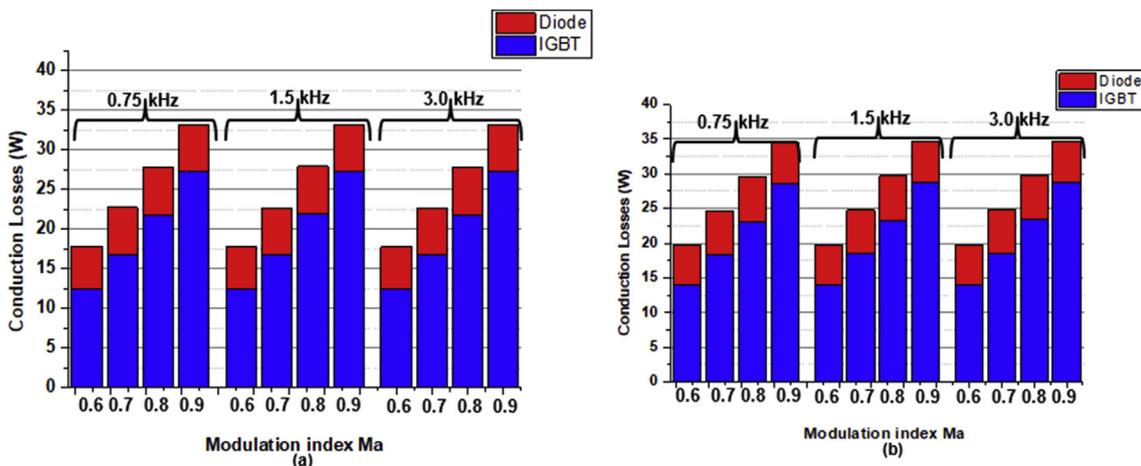


Figure 20. IGBT and Diode conduction loss; (a) Quarter cycle rotation PWM and (b) Carrier cycle rotation PWM.

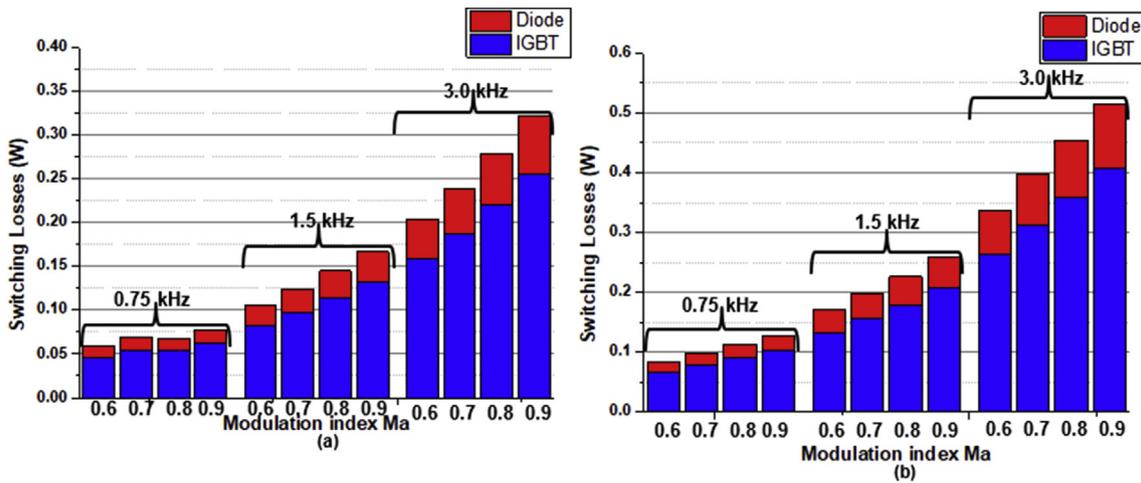


Figure 21. IGBT and Diode switching losses for (a) Quarter cycle rotation PWM and (b) Carrier cycle rotation PWM.

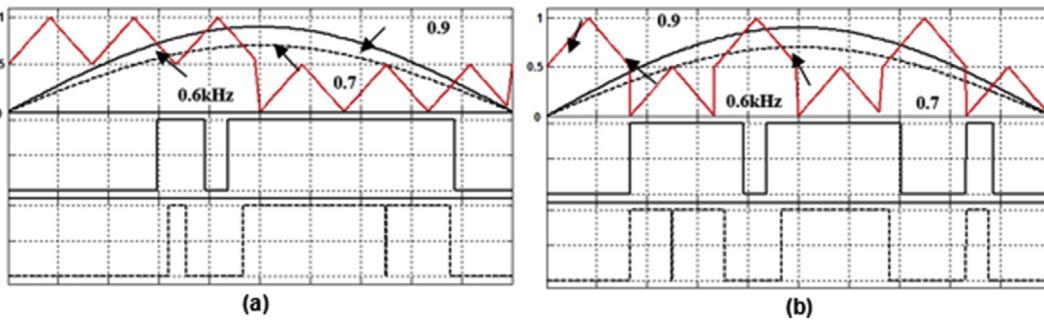


Figure 22. Variation in reference signal m_a (a) Quarter cycle rotation PWM; and (b) Carrier cycle rotation PWM.

5.4.2. Switching loss

Under both swapped carrier methods, the switching losses increase by a factor of two as switching frequency increases from 0.75kHz and 1.5kHz respectively as seen in Figure 21a and b. The difference in switching losses between both methods is solely accounted for by their number of switching transitions over half a fundamental cycle (see Figure 22). The diode switching loss is nearly about 25% of the IGBT switching loss as seen in Figure 21.

5.4.3. Flying capacitor losses

The power losses across both sub-module inner flying capacitors of both methods are equal (see Figure 23a and b). This is because the area of

the charge/discharge region of each flying capacitors (see Figure 19a and b) are equal.

5.4.4. Total loss

The relationship expressed under PD-PWM scheme between total losses with m_a and m_f is similar under these methods. In contrast, the Carrier cycle rotation PWM incurs higher total losses compared to the Quarter cycle rotation PWM as seen in Figure 24a and b respectively.

5.5. Total harmonic distortion (THD) analysis

The phase voltage waveform, and their frequency spectrum, the two swapped carrier PWM methods, are shown in Figures 25 and 26. The

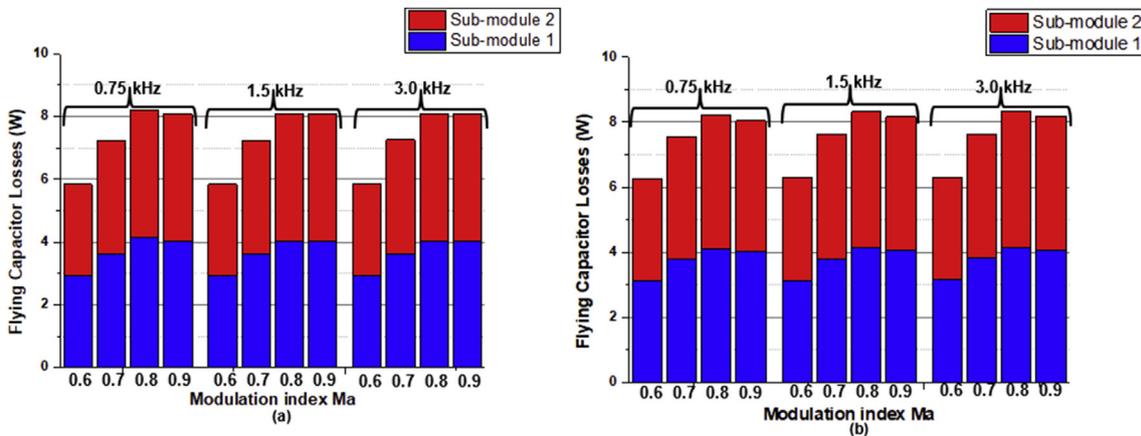


Figure 23. Flying capacitor losses for (a) Quarter cycle rotation PWM and (b) Carrier cycle rotation PWM.

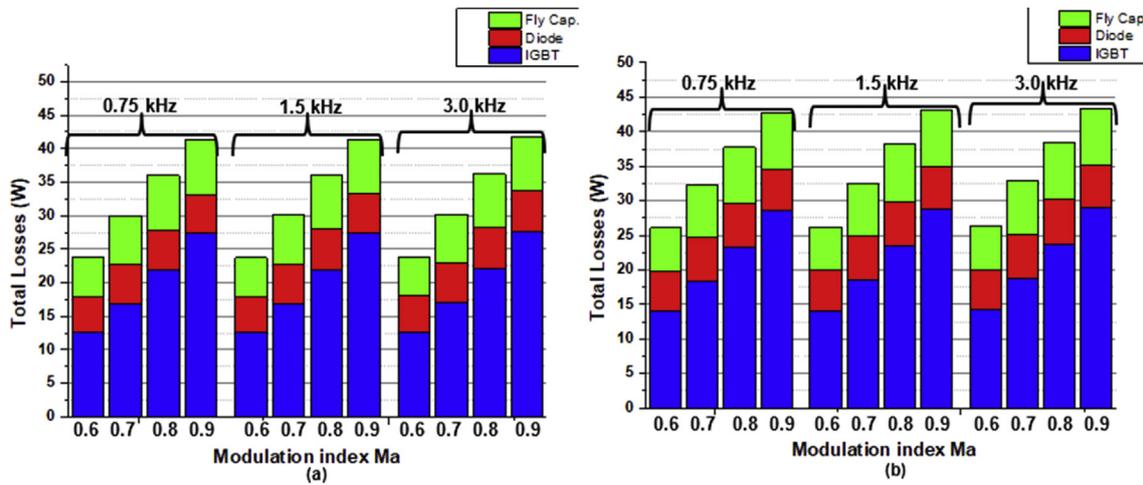


Figure 24. Total losses for (a) Quarter cycle rotation PWM and (b) Carrier cycle rotation PWM.

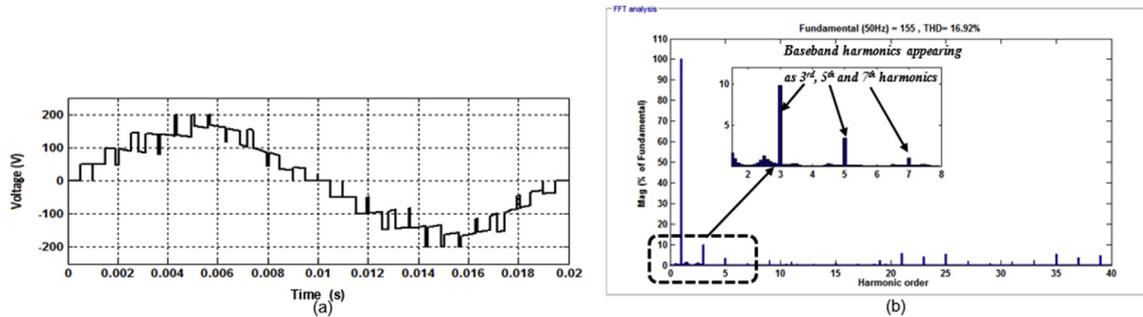


Figure 25. Quarter cycle method Phase voltage (a) waveform and (b) spectrum.

harmonic orders in the spectrum of the phase output voltage waveform is expressed below using unipolar switching:

$$\text{Phase voltage: } f_h = h \times f_0 = (j2m_f \pm k)f_0 \quad (7)$$

Where $j = 1, 2, 3 \dots k = 1, 3, 5 \dots$ odd number for phase voltage.

The THD for the phase output voltage waveforms are 16.92% for Method1 and 12.68% for Method 2. The difference in spectrum quality for both methods lies in the fact that for the quarter cycle method, some baseband harmonics are present around the fundamental frequency while for the carrier cycle method, the baseband harmonics are suppressed up to sidebands found around $2m_f$. These baseband harmonics are introduced by the large voltage deviations experienced by the inner flying capacitors for the quarter cycle method as seen in Figure 25b. These variations in the flying capacitor voltages create distortion in the output voltage waveforms as seen in Figure 25a.

5.6. Sub-module switch utilization

From Figure 27, switches S_{a1} , S_{a2} exhibit less conduction loss than S_{a3} , S_{a4} . But the variation in sub-module switch utilization is lower compared to the PD-PWM scheme.

6. Comparison of different carrier PWM techniques

6.1. Natural balancing ability

This is achievable under all the PWM schemes discussed but the amount of voltage deviation varies between them. This is as observed in Figure 28, which shows the relationship between m_f and inner capacitor voltage variations (i.e. actual voltage deviation/nominal capacitor voltage) for all PWM techniques. From Figure 28, the carrier and quarter cycle rotational swapped PWM techniques offer better voltage deviation

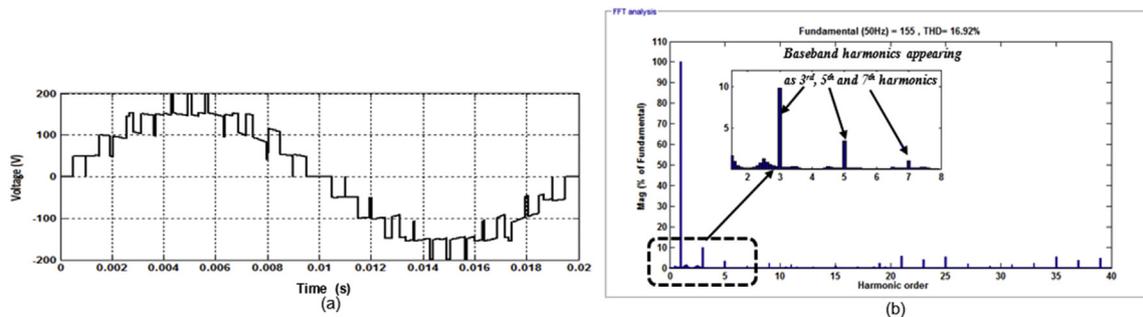


Figure 26. Carrier cycle method Phase voltage (a) waveform and (b) spectrum.

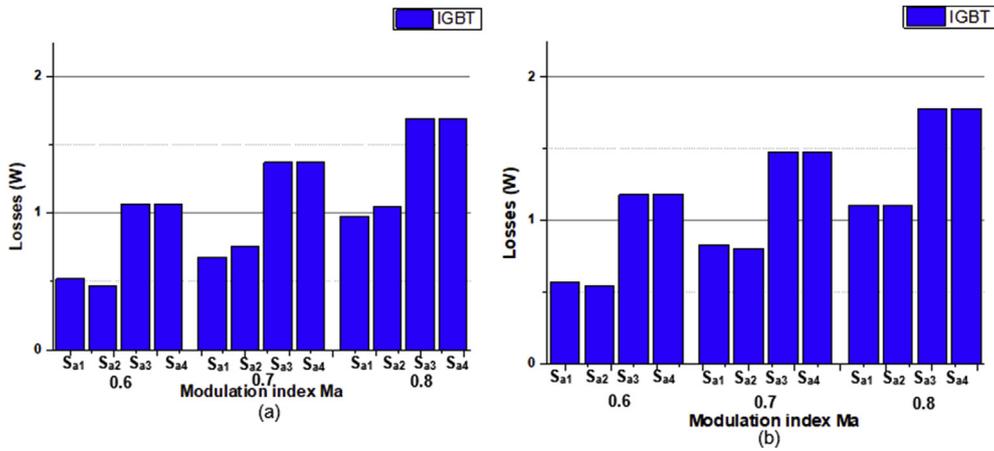


Figure 27. Sub-module switch utilization for (a) Quarter cycle PWM and (b) Carrier cycle PWM.

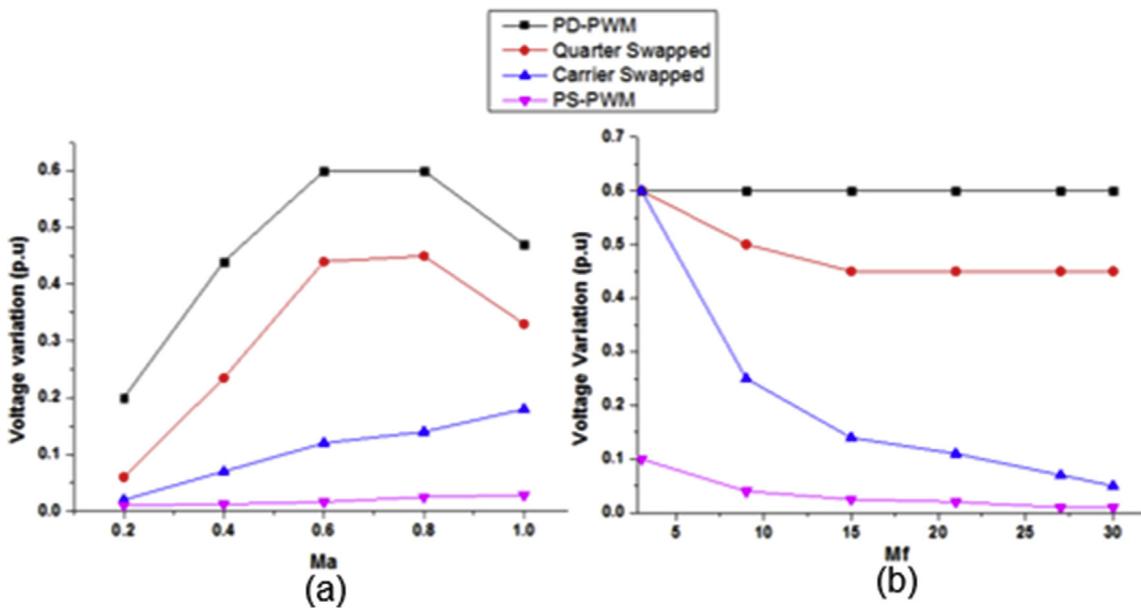


Figure 28. Inner flying capacitor voltage with respect to (a) modulation index and (b) modulation frequency.

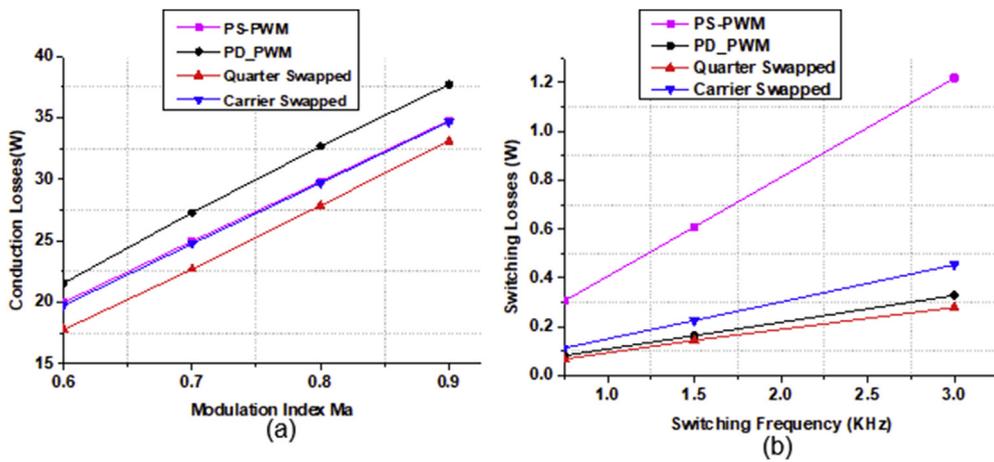


Figure 29. Power losses (a) conduction and (b) switching losses.

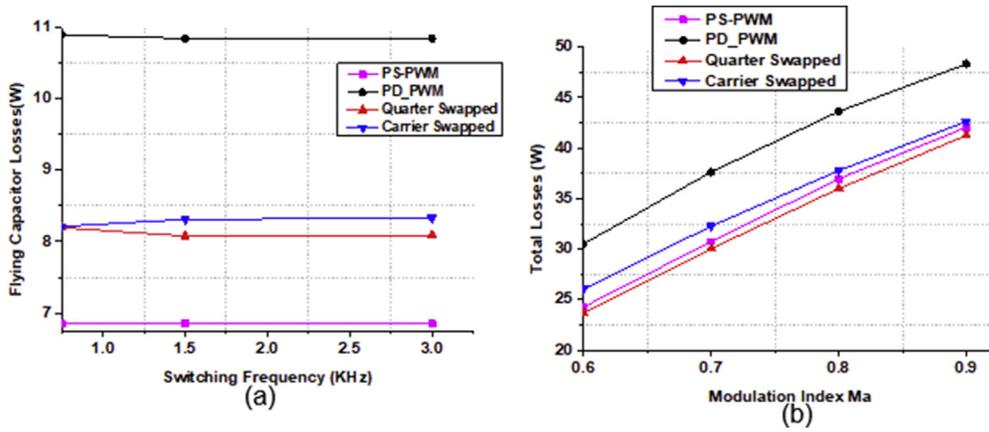


Figure 30. Power losses (a) Flying capacitor and (b) total losses.

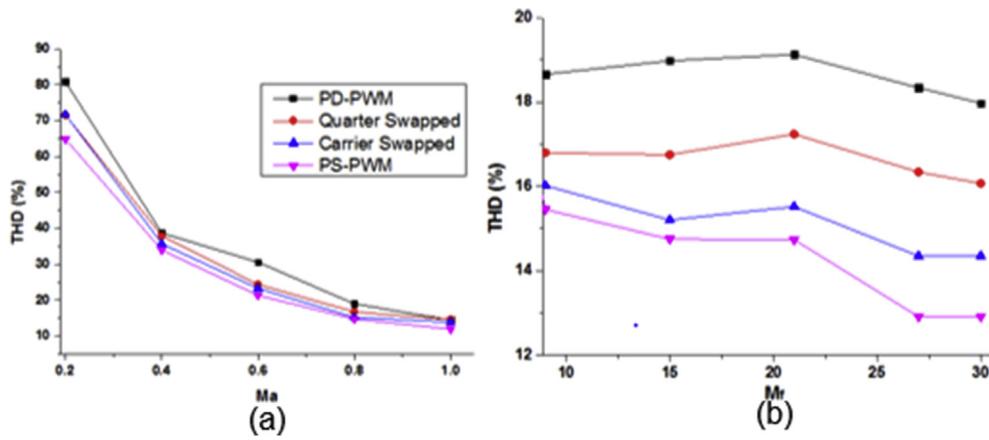


Figure 31. Total harmonic distortion with respect to (a) modulation index and (b) modulation frequency.

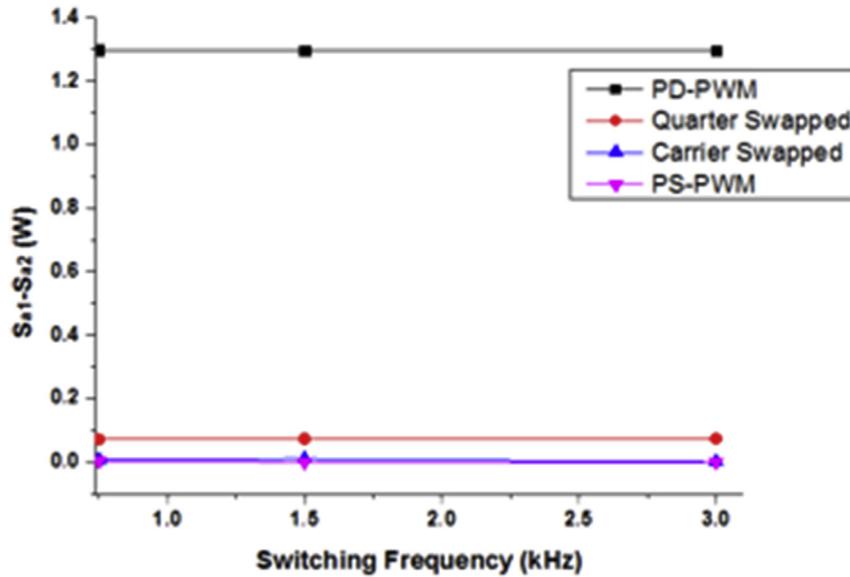


Figure 32. Sub-module switch utilization.

than the phased disposed PWM. This is due to the high number of switching transitions provided by these schemes.

6.2. Power loss

As seen in Figure 29a, the PD-PWM and quarter cycle PWM give the highest and lowest conduction losses compared to the other PWM schemes. This is accounted for by their conduction periods. Figure 29b shows that the PS-PWM incurs more switching losses compared to other PWM methods. This is due to the phase shifting effect of its carrier signals which result in an equivalent switching frequency of $8m_f$ compared to the $2m_f$ offered by the vertically displaced and swapped carrier methods.

The carrier and quarter cycle rotational swapped PWM techniques offer lower inner flying capacitor power losses compared to the PD-PWM as seen in Figure 30a. This is because the rate of charge and discharge has a direct relationship with power dissipated across the equivalent series resistance of each inner flying capacitor. In addition, the summation of each device power losses shows that the both proposed techniques offer lower losses than the PD-PWM as seen in Figure 30b.

6.3. Total harmonic distortion

The PS-PWM and PD-PWM gave the lowest and highest THDs while the two carrier swapped methods are in between as seen in Figure 31. The PS-PWM is thus superior as it causes least levels of its inner flying capacitor voltage deviation.

6.4. Sub-module switch utilization

From Figure 32, it is seen that in comparing between S_{a1} and S_{a2} switches, both proposed modulation techniques achieves an equal switch utilization similar to the PS-PWM whereas for the PD-PWM method, switches S_{a1} and S_{a2} are unequally utilized. And this uneven switch utilization is the sole factor that influences the large voltage deviation in inner flying capacitors when PD-PWM is applied.

7. Conclusion

A detailed investigation on the use of PS-PWM, PD-PWM and two proposed techniques on a modular multilevel cascaded converter using five-level flying capacitor converter (5L-FC) as sub-module has been discussed in this paper. This investigation is based on the performance metrics of natural balancing of floating capacitors, total harmonic distortion, sub-module switch utilization and power losses. These two proposed methods of carrier cycle rotation swapped PWM and quarter cycle rotation swapped PWM techniques has addressed the drawback of high switching power losses of PS-PWM by reducing the switching transition experienced by PS-PWM by a factor of 4. Also, these two proposed techniques addresses the limitations of high flying capacitor losses, high total harmonic distortion, high capacitor voltage deviation and uneven switch utilization when PD-PWM is applied to MMCC using 5L-FC as sub-modules. In conclusion, these two proposed methods can achieve good waveform quality, equal switch utilization and good capacitor voltage deviation like the PS-PWM with an extra benefit of reduced switching and conduction losses.

Declarations

Author contribution statement

Conceived and designed the experiments; Performed the experiments; Analyzed and interpreted the data; Contributed reagents, materials, analysis tools or data; Wrote the paper.

O. J. K. Oghorada: Conceived and designed the experiments; Performed the experiments; Wrote the paper.

Li Zhang: Analyzed and interpreted the data; Wrote the paper.

Egbune Dickson: Contributed reagents, materials, analysis tools or data.

B.A. Esan: Contributed reagents, materials, analysis tools or data; Wrote the paper.

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Competing interest statement

The authors declare no conflict of interest.

Additional information

No additional information is available for this paper.

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