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Paradigm of magnetic domain wall based In-memory computing

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ABSTRACT:

While the conventional microelectronic integrated circuits based on the electron charge are approaching to the theoretical limitation in foreseeable future, next generation nonvolatile logic units based on electron spin have potential to build logic networks of low-power consumption. Central to this spin based architecture is to develop a paradigm for in-memory computing with magnetic logic units. Here we demonstrate the basic function of a transistor logic unit with patterned Y-shaped NiFe nanowires by gate-controlling domain wall pinning and depinning. This spin based architecture possesses the critical functionalities of transistors and can achieve a programmable logic gate by using only one Y-shaped nanostructure, which represents a universal design currently lacking for in-memory computing.

KEYWORDS: *In-memory computing, spin-based transistor, programmable nano-logic unit, domain-wall logic, permalloy.*

1. INTRODUCTION

Conventional microelectronic integrated circuits (ICs) based on complementary metal-oxide-semiconductor (CMOS) are experiencing its bottleneck. On contrast, Spintronics, which could replace CMOS or work alongside it in heterogeneous system, is rapidly evolving due to various breakthroughs in the study of spin quantum phenomena as well as huge industry demand in the last a few decades[1]. Motivated by this, a variety of concepts and spintronic devices have been proposed to overcome the limitation, knows as the memory wall, in which computation and storage are physically separated[2]. Instead of re-optimizing conventional integrated circuits, in-memory computing, which is a new revolutionary concept, aims to subvert the von Neumann architecture by *in-situ* calculations, where the data are located[3]. This new architecture, which has become the most attractive hot topic in the last decade, provides a straightforward advantage by totally eliminating the latency and energy burdens of memory wall[2]. Without any separation between the memory and computation, in-memory computing approach is very similar to the operation method of the human neurons networks[4].

Various in-memory computing schemes have been proposed in both analogue and digital spaces[2] and these new architectures require capability that can compute and store data at the same time. The emerging nonvolatile computational memory techniques, such as resistance switching RAM (RRAM)[5], phase change memory (PCM)[6], magnetoresistive RAM (MRAM)[7], and ferroelectric RAM (FeRAM)[8], which have unique storage strategic rather than based on electronic charge, push the in-memory computing one step forward by reducing the 'distance' between computing and the data[9]. Digital computing by bipolar resistive switching[10] based on spintronic memory device offers several advantages over the nanomagnets[11] and quantum cellular automata [12-14] for in-memory digital computing. Analogue computing with crosspoint arrays is also applying computational memory technique such as RRAM[15] or PCM[16] to implement the in-memory computing. Another branch of in-memory computing is

investigating a magnetic logic architecture, referred to as "domain-wall logic" (DWL), where data are encoded along the magnetic nanowires. The DWL based on soft magnetic material such as Permalloy (NiFe) has been investigated for decades which has a strong potential to replace present logic gate [17-20]. In conventional DWL, however, a continuous rotation magnetic field is applied on logic units [17, 21] and output detection method based on MOKE signal is hard to integrate for in-memory computing. The chirality-encoded architecture has been proposed most recently[20] which has big advance on spin logic where data is encoded within the structures and carried by continuous stream. The limitation of this chirality-encoded architectures, however, is that the output chirality was not totally correlated to the input switching order[20]. Previous researches on DWL just focus on the function of the logic gate, and there is rare investigation of the combination of magnetic logic unit and memory. Here, we demonstrate the development of a new paradigm of in-memory computing by using the ability of DWL to calculate in memory.

Central to this work is representing a phenomenon in specific design of DWL based on Y-shaped magnetic nanostructure which shows the similar function of a transistor in the circuit. The transistor inside the CMOS ALU (arithmetic logic unit) has a 'Gate' terminal which determines the conductivity of this device (as shown in Figure 1a and b). Inspired by this, we have designed a Y-shaped nanowire (as shown in Figure 1d) to implement the similar function of a conventional semiconductor transistor. The 'Gate' arm has the same effect as the 'insulated gate' in the transistor. The magnetization direction of this 'Gate' arm (restricted arm) controls the domain propagation process of the 'Drain' and 'Source' arm (switching arms)[22]. The domain wall pinning and depinning state in Y junction corresponds to 'gate on' and 'gate off', respectively, at the same input condition (as shown in Figure 1e). By controlling different magnetization states of three arms, several basic Boolean logic functions can feasibly perform under two input signals. Based on this phenomenon, a programmable logic gate with functions

including OR/NAND/XOR is achieved within only one nanostructure. Furthermore, comparing with the conventional CMOS-Based computer architecture (as shown in Figure 1a), this DWL can either process input signals or store output results that breaks the physical separation between the memory and computing. Instead of reading data and writing back process, spin-based logic is stored and operated in memory with a single writing instruction (as shown in Figure 1c). After receiving the instruction, a series of input signals will change the spin state of three arms, which is called the calculation stage. Subsequently, at the memory stage, the spin state is stored in two switching arms. There are two different spin states, namely "head to head" (domain wall exists) and "head to tail" to yield different outputs [23-25] (operations are illustrated in Figure 1e). This ingenious architecture, which combines ease of fabrication and integration for in-memory computing, fills the gap in the simplification of complex logic gates either in a conventional integrated circuit or the previously proposed DWL[17, 19-20, 26].

2. EXPERIMENTAL SECTION

The Y-shaped nanowires were made from the magnetically soft Permalloy ($Ni_{80}Fe_{20}$) by e-beam lithography. Magnetization analysis was performed with a magneto-optical Kerr effect (MOKE) image system[27]. The successive images were taken at each applied in-plane sweep magnetic field in 1.44mT steps. The MOKE result was extracted from the average of 5 times full loop sweep signal. Same experiment was repeated for three times. Figure. 1d shows a SEM image of Y-shaped nanostructure with one nucleation pad (maximum width 6μm, maximum length 10μm). The angle between the three arms of Y-shaped nanowire are equal to 120°. 'Drain' arm and 'Gate' arm are 1μm width, 27μm length (from joint to the tail), and 'Source' arm is 1μm width, 32μm length. For the nanowire design, the large ratio of length to width can yield strong shape anisotropy enough to overcome the driven magnetic field to ensure the functionality of nanowire device. H_{sat} ($\pm$ 350mT) indicates initial applied saturated field along 'Gate' arm ($x - \theta'$ ($\theta' = 60°$)) and an orthogonal external field H_a (the range of

change is -350mT to 350mT) is then exerted along the $x + \theta$ where θ is $30°$(Detailed of other experimental results about the 'Gate' arm controlled are analyzed and presented in the Supporting Information, Section S4).

3. RESULTS AND DISCUSSION

Figure. 2 represent the Kerr contrast images and continuous magnetization progress within the structure. Before the Kerr imaging, the sample was first saturated at magnetic field H_{sat} as an initial state. And subsequently a continuous sweeping magnetic field H_a is applied to the sample along $(x + \theta)$. Under the sweeping magnetic field which started from negative to positive and sweeping back, the magnetization state of entire device is changing via applied external field. Eight images (Figure. 2a to d and f to i) experiencing different applied field were picked up from the whole process. The magnetization reversal first occurs at nucleation pad and then the domain wall formed between the arm and the nucleation pad is pushed along the 'Source' arm (Figure. 2a). The domain wall passes the joint after depinning and subsequently moves to the terminal of 'Drain' arm (Figure. 2b), leading to a magnetization direction reversal of the 'Drain' arm. Due to the strong magnetic shape anisotropy in narrow FM (ferromagnetic) wire, the magnetization direction (magenta arrow shown in Figure 2a to d) of the 'Gate' arm is restricted to be directed parallel to the wire axis under orthogonal magnetic field H_a. Two switching arms experience different magnetization process under magnetic field sweep back from positive to negative (as shown in Figure. 2c and b). After the domain wall leaves the nucleation pad, it propagates from 'Source' arm to 'Drain' arm without pinning, meanwhile 'Gate' arm remains its magnetization direction pointing from the terminal to joint. In the opposite spin state (blue arrow shown in Figure 2f to i) of the 'Gate' arm, the 'Drain' arm and 'Source' arm exhibit opposite magnetization process at the same experimental method. The domain propagates from 'Source' arm to 'Drain' arm without pinning appeared during negative

to positive field (Figure. 2f and g). And domain wall pinning occurred during positive to negative field (Figure. 2h and i).

For easy observation, we combine the hysteresis loops taken from 'Source' arm and 'Drain' arm under sweeping magnetic field showing in Figure. 2e. A significant different coercivity (approximately 15mT) of the 'Source' and 'Drain' arm can be clearly observed from Figure. 2e under a positive magnetic field. This coercivity bias indicates asymmetric magnetization of the 'Drain' and 'Source' arm. Comparing with Figure. 2e, an opposite offset coercivity around 19mT can be observed under a negative external field at the opposite spin state of 'Gate' arm as shown in Figure. 2j. This asymmetric magnetization process shows that the spin state of the 'Gate' arm determined by the external magnetic field can control the magnetization of the 'Drain' arm, which has the similar function of a transistor in the conventional circuit.

To gain understanding of the domain-wall motion within the nanowire in detail, we performed quasi-static micromagnetic simulations of the Y-shaped nanostructure with one nucleation pad showing in Figure. 3 (Detailed of other simulation results are analyzed and presented in the Supporting Information, Section S3). The micromagnetic simulations are performed by ***Mumax3*** simulation package (reference). The parameters of the device material in the micromagnetic simulation are given as blow, the exchange stiffness $A_{ex} = 13 \times 10^{-12}$ j/m, the crystalline anisotropy constant $\mathrm{K} = 0 j/m^3$, saturation magnetization $M_s = 8.6 \times 10^5$ A/m and for the quasi-static simulations the Gilbert damping constant $\alpha = 0.5$. The cell size for the 2D micromagnetic simulation is $5\mathrm{nm} \times 5\mathrm{nm} \times 20\mathrm{nm}$.

The simulation results showed that the domain switching process is similar to the function of the transistor. For the domain-wall pinning situation (Figure. 3a), there is a transverse domain-wall generated at the junctions showing in the enlarge image. Meanwhile,

the magnetizations along the 'Gate' to 'Drain' arm and 'Gate' to 'Source' arm are the head-to-tail. Thus, the domain depinning needs to overcome an energy barrier. Further increasing the applied field, the transverse domain-wall overcomes the barrier and propagate to 'Drain' arm (Figure. 3b). Under opposite magnetic field, three arms appeared to have head-to-head domain configurations with the domain-wall approaching to the junction. This led the domain wall to propagate directly along an easy magnetization direction to 'Source' arm, where 'Gate' arm is a hard magnetization axis along the external field due to strong shape anisotropy (Figure. 3c and d). Since the device was applied sweeping magnetic field, the initial and final magnetization state are totally same (as shown in Figure. 3d and i). The hysteresis loops which extracted X-axis magnetization from one pixel state at two arms (Figure. 3e) show a red square loop ('Source' arm, parallel to the X-axis) and a gray oblique loop ('Drain' arm, an 60° angle with X-axis). This result indicates that an asymmetric magnetization process takes place on the 'Drain' arm, which is exactly the same as the experimental observation.

Instead of applying H_{sat} as an initialization in the simulation, opposite magnetic field $-H_{sat}$ was also applied to set up the initial state. As external field $-H_{sat}$ applied along the 'Gate' arm, the magnetization direction along this arm is from joint to the terminal which shows the blue background in Figure. 3f. The same sweeping magnetic field was applied to this simulation, however, the directly propagation process appeared first (Figure. 3f and g) and subsequently domain-wall pinning state (Figure. 3h and i) occurred under reversed field condition. Comparing with pervious simulation hysteresis loop (Figure. 3e), Figure. 3j represents the opposite asymmetric magnetization process due to a reversed initial spin state of 'Gate' arm. Detailed simulation results are analyzed and presented in the Supporting Information, Movies S1 and S2.

According to these simulation and experiment result, the magnetization direction of 'Gate' arm and the 'Source' arm, which is directly connected with nucleation pad, plays a

decisive role in this transistor-like magnetic nanostructure. Our simulation results (figure.3a to d and f to i) indicate that the gate arm magnetization impacted by the external magnetic field and it's not exactly along the arm axis. This switching behavior of 'Gate' arm is attributed to the result of both external magnetic field and shape anisotropy. Since the asymmetric results mainly come from the along or opposite magnetization directions of the 'Source' and 'Gate' arm (such as head-to-tail or head-to-head), therefore, a slightly changes in the direction of the 'Gate' arm magnetization will not significantly affect the functions. The simulation results represent agreements to the experimental phenomenon under large amount of repeated experiment summarized. This Y-shaped nanostructure with the required functionality observed reliably shows the feasibility to develop logic unit or integrated logic networks. Here we propose several significant logic units which has strong potential to enhance the value of in-memory computing.

Based on the observed transistor-like phenomenon, we propose a feasible programmable logic gate, where a universal design based on just one nanostructure is still lacking. The operating principles of magnetic programmable logic gate are illustrated in Figure. 4. The key characteristic is that the output exhibits two different conductivity states for high ('1') or low ('-1') under two input external fields, where the two arms have different spin states due to the asymmetric magnetization process within the nanowire. The input signal Y_{input} (same with H_{sat}), along the $\mathrm{x}-\theta'$ ($\theta'=60°$) which should be the first input (Detailed of inputs order are analyzed and presented in the Supporting Information, Section S4), saturates the 'Gate' arm and controls its magnetization direction (H_{sat} refer to '1' and $-H_{sat}$ refer to '-1'). Subsequently, a set saturated field X_{set} that set to '1' $(\mathrm{x}+\theta)$ or '-1' $(-(\mathrm{x}+\theta))$, which initializes the magnetization of arm 'Source' and 'Drain' to same direction (head to tail magnetization state), can be used to control the logic gate selection. Finally, a X_{input} along the $(\mathrm{x}+\theta)$ or $(-(\mathrm{x}+\theta))$ with '1/2' magnitude (the specific value depends on the specific

structure) apply to this DWL. Here we illustrate three different logic gates function within one nanostructure.

OR GATE. We select the saturated field X_{set} to '+1' to implement the OR logic gate (Figure. 4a to d). Noticeably, Y_{input} should first input to this nanostructure, otherwise it will impact the magnetization of other two arms. Each time after the Y_{input} applied, the saturated field X_{set} set the 'Drain' arm and 'Source' arm to the same state. And subsequently X_{input} is applied to complete a cycle of logic calculation. Detecting the conductivity between the 'Drain' arm and 'Source' arm, we get the same function of OR gate representing in the Table. 1. Due to the asymmetric magnetization process, the domain wall is pinned at the junction (Figure. 4a) where represents low conductivity because of domain wall (Tail-to-Tail) existed at joint under both 'high' input of X and Y. Same direction of X_{input} and X_{set} cause no changing of two arms' magnetization (Head-to-Tail) (Figure. 4b and d) which exhibit high conductivity. Figure. 4c indicates the fast propagation process when 'low' Y_{input} and 'high' X_{input} are applied, and same magnetization direction along the 'Drain' arm and 'Source' arm. As summary, only 'high' input of both X, Y can yield 'low' output under the 'low' X_{set} setting saturated field.

NAND GATE. When '-1' of X_{set} setting saturated field was selected, this programmable magnetic logic gate switches to the NAND function (Figure. 4e to h). With the same input signal applied to this nanostructure, we can only get the 'low' output under both 'low' input of X, Y. This function represents the same logic of NAND gate and true table shows in Table.2.

XOR GATE. Different from pervious logic gate, the XOR function can be implemented under two opposite X_{set} setting saturated fields (shown as Figure. 4i to l). The Y_{input} can trigger the direction of X_{set}. A corresponding opposite setting saturated field should be activated when Y_{input} is 'high' or 'low'. Due to the asymmetric magnetization, the output

represents same function of XOR gate that gives a true (high) output when the number of true inputs is odd. And true table exhibits in Table. 3. This XOR gate is a combination of part of OR gate and NAND gate. As shown in the Table. 3, the X_{set} and Y_{input} are bound, which means the X_{set} only related to Y_{input} in XOR gate state. In the real operation, the X_{set} and Y_{input} are executed by a same field driver that represent a single input but control opposite applied magnetic field directions.

Furthermore, if we detect the resistance state of two arms rather than the conductivity, the relative 'high' and 'low' value will be reversed. And this programmable logic could be extended three more logic functions. When '+1' of saturated field X_{set} is selected, the OR gate becomes AND gate due to the fact that all high inputs yield high output. And NAND gate is transferred to NOR because all low inputs yield high output under '-1' setting field X_{set}. Due to the opposite function, the XOR becomes NXOR where the same inputs yield high output. For translating the input signal to magnetic field, the extra field drivers is necessary. The value of '1' or '1/2' refer to the magnitude of external field and they are fixed by each field driver. When the Y-shaped nanostructure is running, the driver switches the direction of the magnetic field according to the input digital signal 0 or 1 (- or +). Therefore, swapped the inputs will not violate the truth table and keep output value correct which satisfy the two inputs should be equivalent and commutable.

In general, this novel nanostructure can implement various Boolean logic functions and thus a real feasible spintronic programmable logic unit could be achieved. In this research, the external magnetic field and MOKE signal detection are the main investigation method. Further improvements could be achieved by patterned electrical contacts nanowire as an input pulse source[20, 28-29]and patterned electrical pads as a detector of domain-wall electrical resistance[23-24, 30]. In addition, we have designed another Y-shaped nanostructure with two nucleation pads which has been investigated by the same method (Detailed of other experiment and simulation

results are analyzed and presented in the Supporting Information, Section S1 to S3). These two nucleation pads nanostructure was found to have the advantage of consuming less energy.

4. CONCLUSIONS

In this article, we report a transistor-like phenomenon occurred in Y-shaped magnetic nanostructure and demonstrate its functions by MOKE imaging and micromagnetic simulations. Based on the asymmetric magnetization process, we propose a feasible paradigm for in-memory computing programmable logic gate, which can reduce significantly the complexity and area of conventional logic circuits. Utilizing the characteristic of DWL for both storage and calculation, in-memory computing can be implemented more efficiently and directly. To further implement the paradigm of the magnetic domain wall based in-memory computing, one may need to combine with one of these newly developed memory techniques including chirality-encoded DWL[20], STT-MRAM[31], Magnon-driven spintronic devices[32]. While the gating-controlled operation of the Y-shaped magnetic nanostructure as demonstrated in this work provides an underlying framework for the in-memory computing architecture, significant efforts are still needed to address the interdisciplinary challenge of integrating spintronic ALU for calculating data and memory for storing data to achieve the practical in-memory computing.

Supporting Information

Detailed device fabrication process; SEM image of the Y-shaped nanostructure with two nucleation pads; Detail experimental and simulation results of the Y-shaped nanostructure with two nucleation pads including MOKE images and ***Mumax3*** results; Input order analysis of the different Y-shaped nanostructure; Simulation animation of the Y-shaped nanostructure with one nucleation pad (Movies S1-S4).

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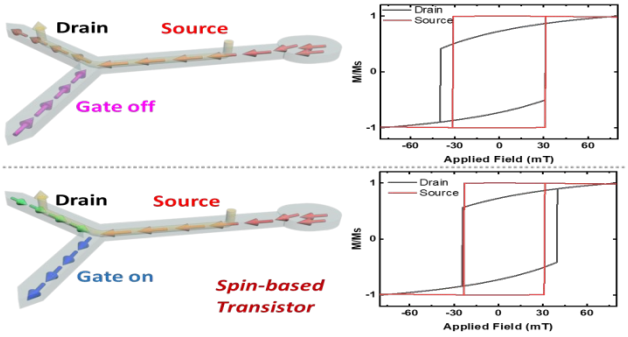

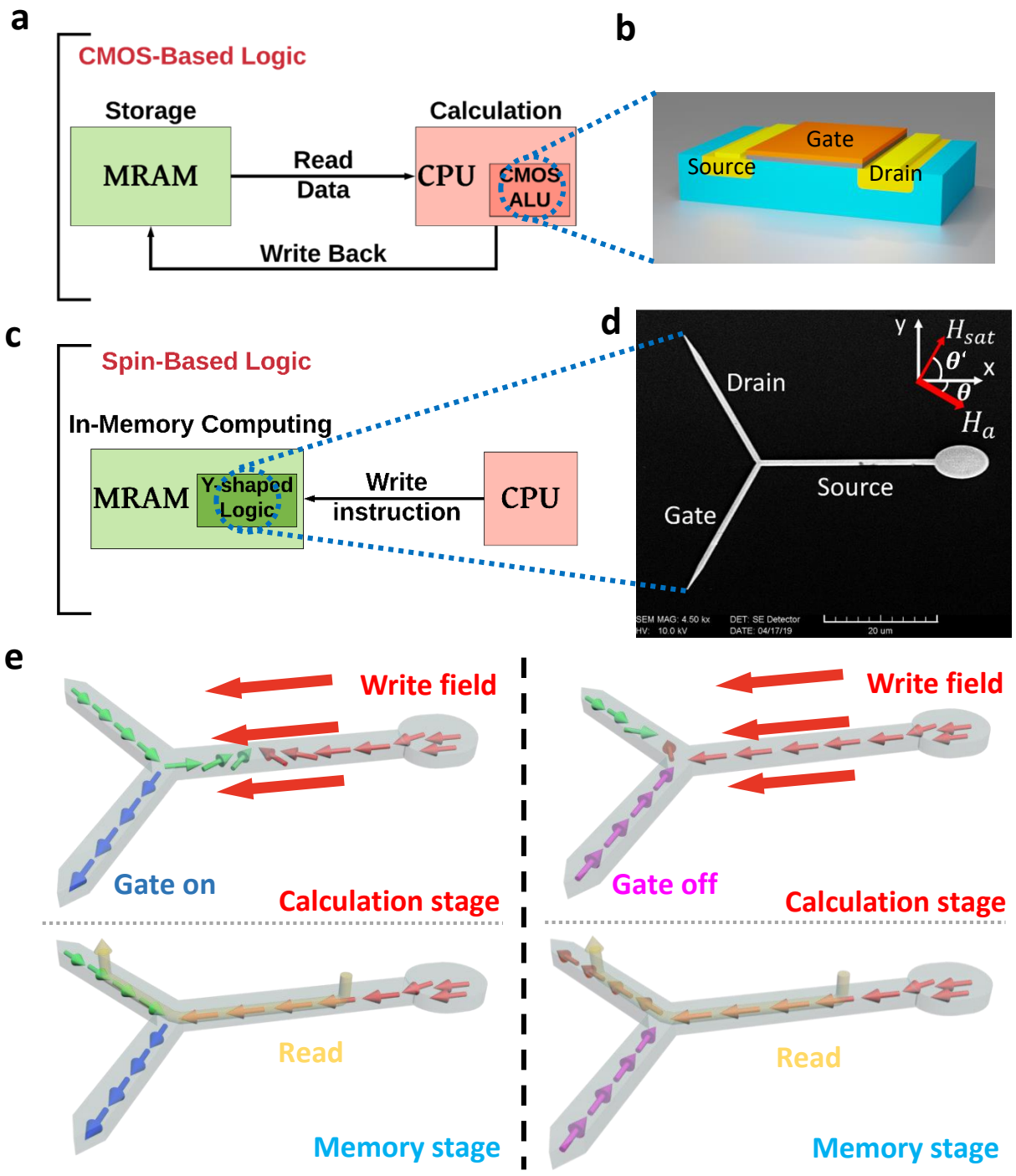

Figure 1. (a) Schematic diagram of conventional CMOS-Based architecture. (b) The conventional transistor used in integrated circuits. (c) The new design of spin-Based In-memory computing implemented Y-shaped logic can be stored and calculated with only one write instruction. (d) SEM image of transistor-like permalloy Y-shaped nanowire with one nucleation pad. Three arms correspond to the 'Drain', 'Source' and 'Gate' of conventional transistor. The red arrows showing at right top indicate the external in-plane magnetic field

directions of H_{sat} and H_a. (e) Schematic diagrams of operation to a Y-shaped nanowire both in calculation stage and memory stage. Left diagrams illustrate that when the 'Gate on', the domain wall pinned at the joint during write field, and the read process will detect a higher conductive at memory state. Conversely, lower conductive will be detected by the read current at same write field due to the 'Gate off' showing on the right diagrams.

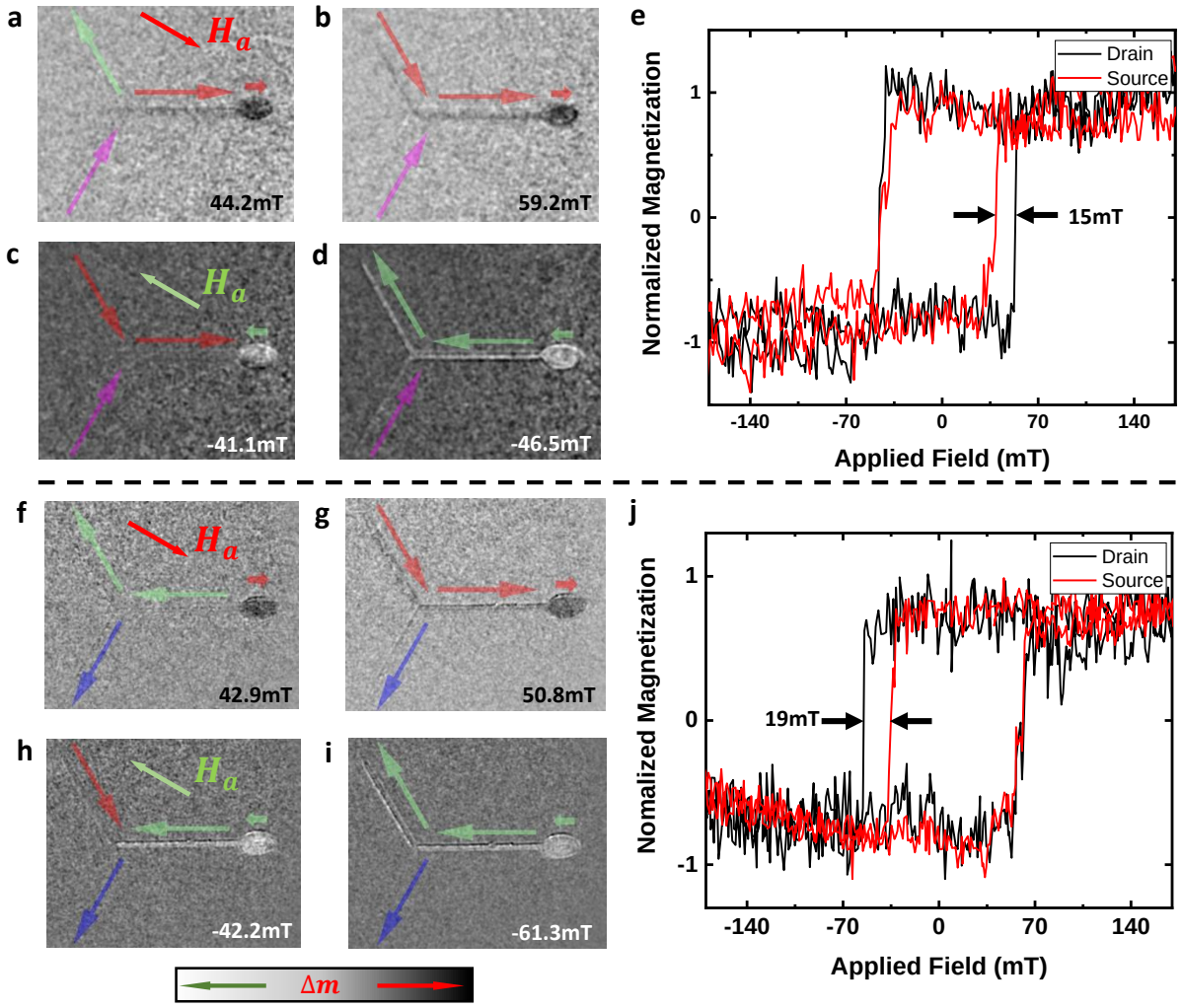

Figure 2. Contrast images show two opposite magnetization process of Y-shaped nanowire with one nucleation pad at two different Gate states (a to d and f to i). Contrast here was generated by dividing the two different initial state image (m_1) by the specific image (m_x) resulting in a magnetization distribution $\Delta m = m_1/m_x$. Various colour arrows represent the magnetization direction along the three arms and nucleation pad that assist the reader's interpretation of the contrast. (e) and (j) are longitudinal MOKE signal taken from 'Drain' arm and 'Source' arm corresponding to black and red hysteresis loop show an asymmetric magnetization process. Approximately 15mT pinning field occurred during the process of the sweep field from negative to positive showing in (e). And approximately 19mT pinning field occurred during the process of the sweep field from positive to negative showing in (j).

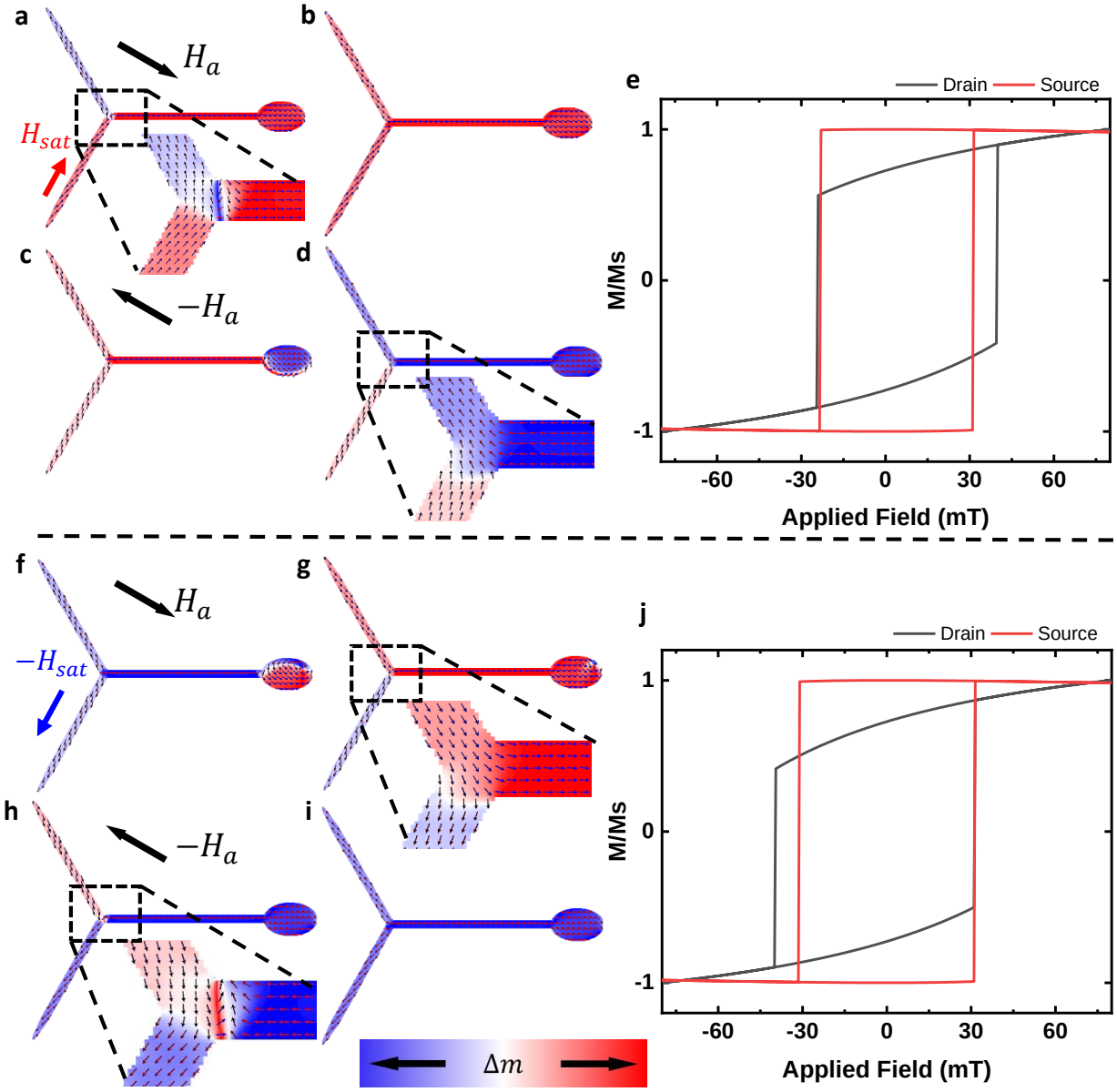

Figure 3. A series of simulation results (a) to (d) showing the detail of magnetization process for Y-shaped nanowire at initial saturated field along $y + \theta$ for H_{sat}. (f) to (i) represent magnetization process under same sweeping magnetic field condition at opposite $-H_{sat}$ saturated field as initialization. The enlarge figures of simulation results indicate more details of magnetization direction inside the junction. (e) and (j) Hysteresis loop taken from two pixels at 'Drain' arm and 'Source' arm corresponding to H_{sat} and $-H_{sat}$ saturated field.

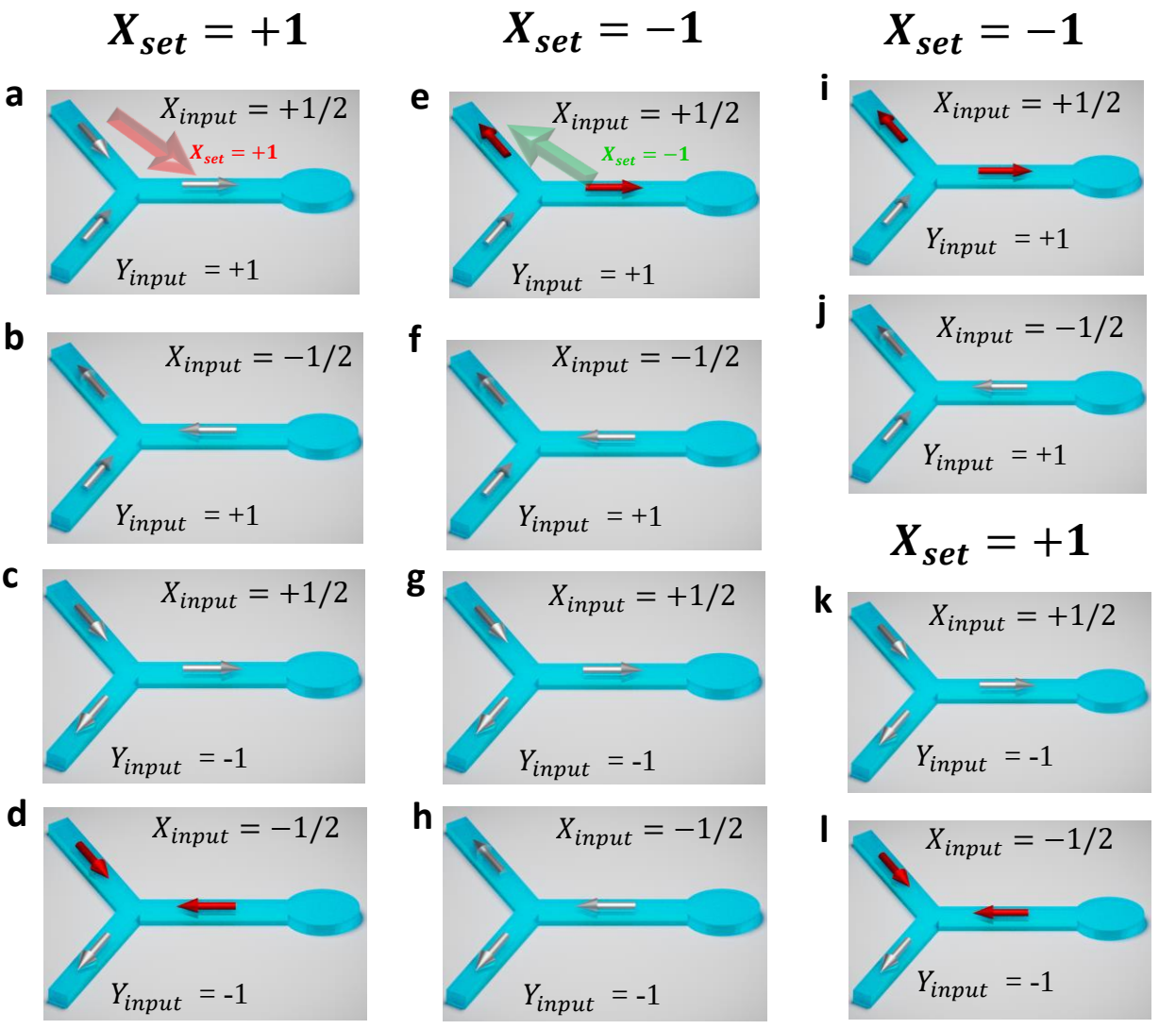

Table. 1 OR GATE

$X_{set} = +1$		
X_{input}	Y_{input}	output
+1/2	+1	+1
-1/2	+1	+1
+1/2	-1	+1
-1/2	-1	-1

Table. 2 NAND GATE

$X_{set} = -1$		
X_{input}	Y_{input}	output
+1/2	+1	-1
-1/2	+1	+1
+1/2	-1	+1
-1/2	-1	+1

Table. 3 XOR GATE

$X_{set} = -1$		
X_{input}	Y_{input}	output
+1/2	+1	-1
-1/2	+1	+1
$X_{set} = +1$		
+1/2	-1	+1
-1/2	-1	-1

Figure 4. (a) to (d) exhibit the operation principle of OR gate. Under the '+1' X_{set} saturated field, the output represents low when only both high inputs come, and Table. 1 illustrates the true table of this magnetic OR gate. (e) to (h) illustrate the operation principle of NAND gate. A low output yield when the both low inputs apply under '-1' X_{set} saturated field. The

functions show in the Table. 2. (i) to (l) represent the operation principle of XOR gate. Y_{input} trigger the different X_{set} saturated field state. Output gives high when the number of true inputs is odd which exhibit in the Table. 3.