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Unni, V., Long, H.Y., Yan, H. et al. (3 more authors) (2018) Analysis of drain current saturation behaviour in GaN polarisation super junction HFETs. IET Power Electronics, 11 (14). pp. 2198-2203. ISSN 1755-4535

https://doi.org/10.1049/iet-pel.2018.5583

Analysis of drain current saturation behaviour in GaN Polarisation Super Junction HFETs

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Abstract: The magnitude of saturation current in a power device significantly impacts its short circuit capability. In conjunction with the unprecedented miniaturisation that GaN offers, there is a compelling rationale to examine this critical parameter in GaN transistors for thermally stable and reliable power converter applications. This article presents a comprehensive analysis of the physical behaviour that yields intrinsically low drain current saturation in GaN Polarisation Super Junction (PSJ) HFETs. The analysis in this work has been performed using electrical characterisation data of conventional and PSJ HFETs, supported by physics-based two-dimensional device simulations. Insight is gained on the differing device architecture-dependent mechanisms that determine the magnitude of drain current density in both types of devices when biased in the saturation region.

1. Introduction

Gallium Nitride (GaN) power semiconductor devices are emerging as chosen candidates for the next generation of advanced power electronics due to its superior intrinsic material properties in comparison to Silicon (Si). One of the key challenges in the design of power semiconductor devices is electric field management under off-state conditions such that it provides the best trade-off between specific on-state resistance (R_{ON}.A) and blocking voltage capability of the device. This is typically accomplished in conventional AlGaN/GaN HFETs using field plates (FP) as illustrated in Fig. 1 (a) [1-4].

In the case of Polarisation Super Junction (PSJ), a 'box' like electric field is attained by engineering the polarisation property inherent to group III-V nitride compound semiconductors and alloys with Wurtzite crystal structure. The basic device architecture is based on a GaN/AlGaN/GaN double hetero-structure where positive and negative polarisation charges of equal charge density coexist at the AlGaN $(000\bar{1})$/GaN (0001) interface with two-dimensional electron gas (2DEG) accumulation and GaN $(000\bar{1})$/AlGaN (0001) interface with two-dimensional hole gas (2DHG) accumulation respectively. This has been illustrated schematically in Fig. 1 (b). With on-state characteristics as in conventional AlGaN/GaN HFETs utilizing the 2DEG for

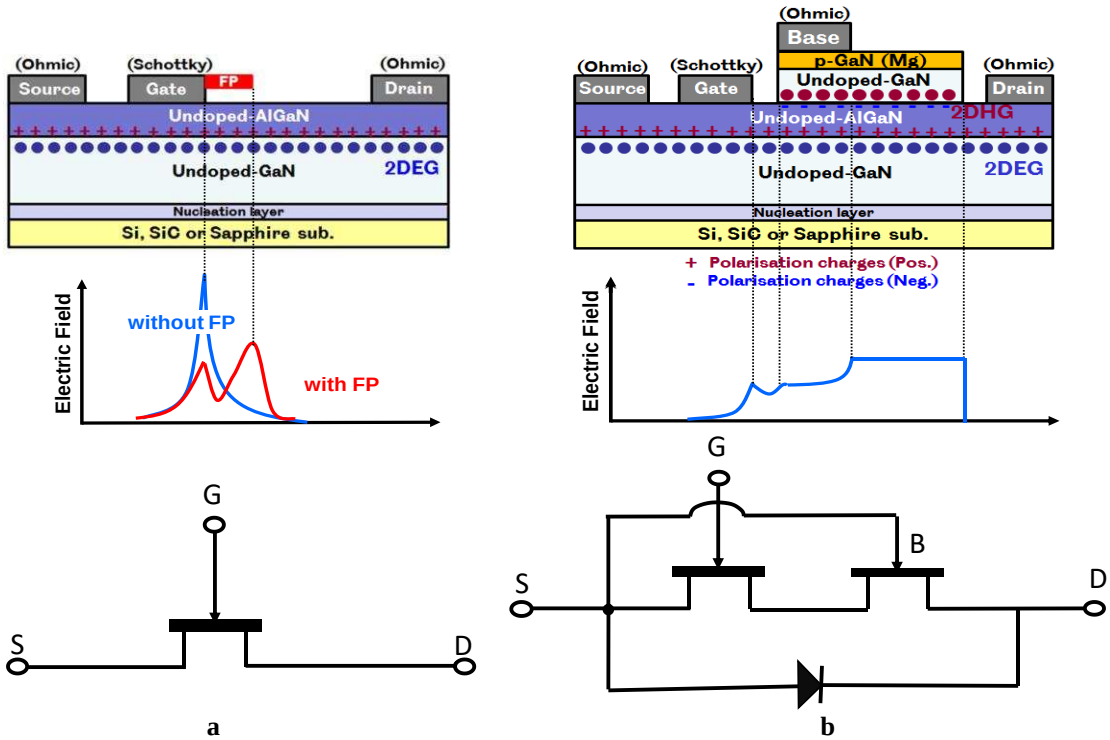


Fig. 1. Schematics and circuit model of device cross-section and simplified electric field distribution under off-state conditions **(a)** Conventional HFET (with/without FP), **(b)** PSJ HFET

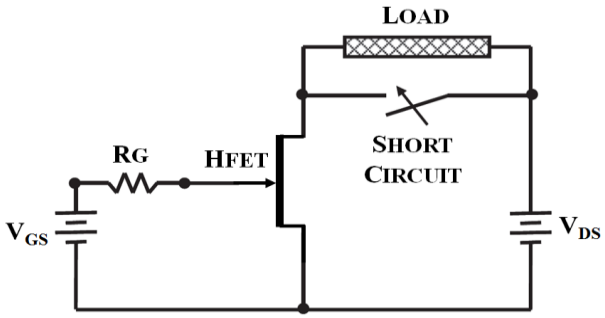
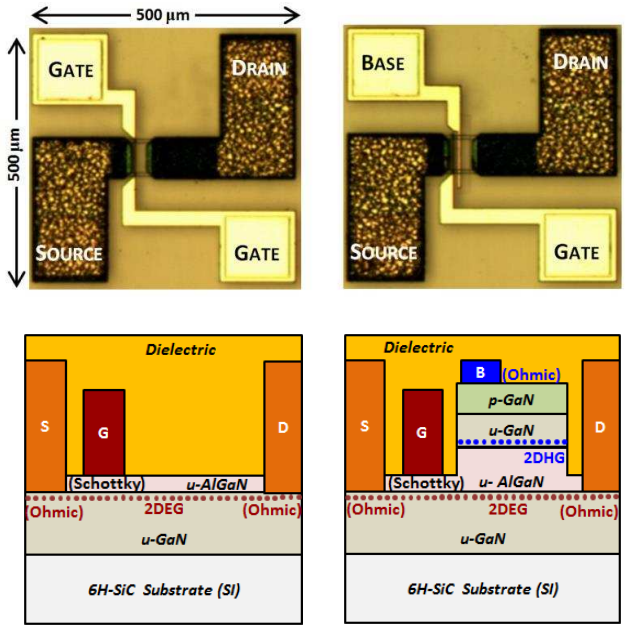


Fig. 2. Simplified schematic depiction of a short circuit operating condition (Adapted from [9])

conduction, PSJ technology employs inherent charge balance in the hetero-structure to enhance the blocking voltage capability for a given drift length [5-8]. As also demonstrated in the circuit models of PSJ HFET, its base terminal can be connected to source terminal internally to form a 3-terminal device and operates in the same way as conventional HFET.

It has been observed in high voltage PSJ HFETs that the drain saturation current (I_D) is less than half of the magnitude of an equivalent conventional AlGaN/GaN HFET with similar on-state characteristics [6]. This behaviour can prove useful in enhancing reliability and be leveraged in power converter applications which demand robust short circuit performance [1].

As illustrated in Fig. 2, during the operation of a power converter in an industrial environment, anomalous events could inadvertently generate a short circuit across the load which is directly connected to the drain terminal of the power switching transistor. This condition results in the simultaneous application of a high voltage (V_{DS}) and a current that is limited by the magnitude of the transistor's drain current at saturation. It leads to high power dissipation within the device and can cause destructive failure if the fault is not detected and cleared within the withstand time (in the order of microseconds typically) of the device [10].



a b

Fig. 3. Micrograph and simplified cross-sectional schematic of (a) Conventional HFET (b) PSJ HFET

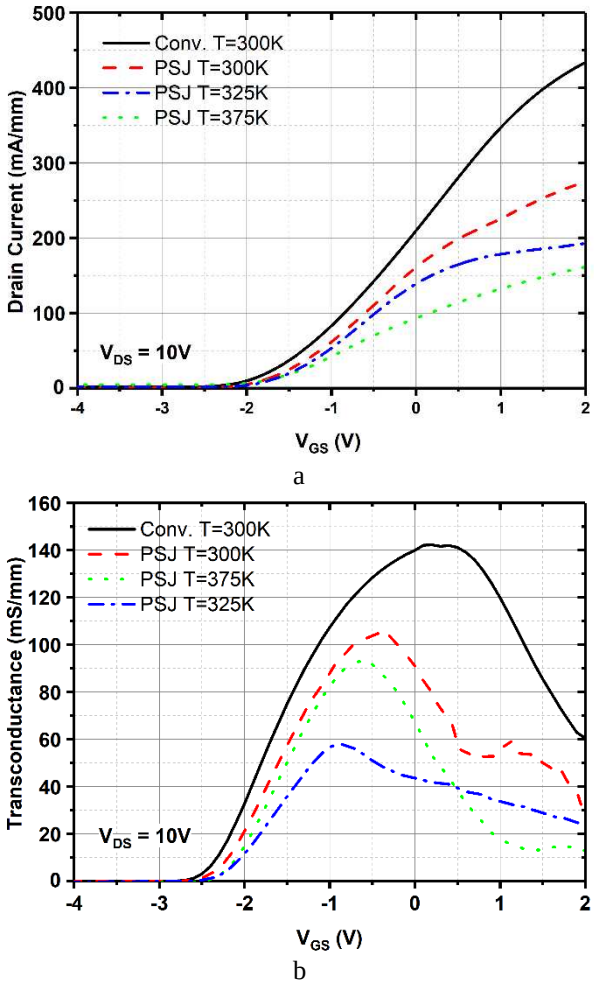


Fig. 4. Measured characteristics of (a) transfer I-V characteristics at V_{DS}= 10V and (b) derived transconductance from (a).

The superior figure-of-merit associated with a wide bandgap semiconductor like GaN enables unprecedented miniaturisation of devices and power management systems. This critical attribute along with ultra-fast switching capability of GaN devices mandates extremely fast-responsive fault detection systems to keep the heat dissipation during a short circuit under control. Huang et al., reported that by operating at low on-state gate bias, the short circuit performance in 650V AlGaN/GaN depletion-mode HFETs could be improved from <0.5 µs to 30 µs in withstand time and from 5 mJ to 85 mJ in energy tolerance, at a bus voltage of 400 V [11]. However, such an approach will compromise the efficiency due to an increase in on-state losses. Having intrinsically low transistor saturation current to start with can also alleviate the need to limit the current externally. The physical mechanism that determines and yields such a characteristic in PSJ HFETs has been examined in detail and described in this work.

2. Device Fabrication

GaN/AlGaN/GaN heterostructure with layer thickness of 20nm, 47nm and 800nm, respectively, was grown by MOCVD on semi-insulating 6H-SiC substrates (370µm). Drain and source electrodes (Ti/Al/Ni/Au) were deposited on a selectively-etched AlGaN surface using ICP etching and

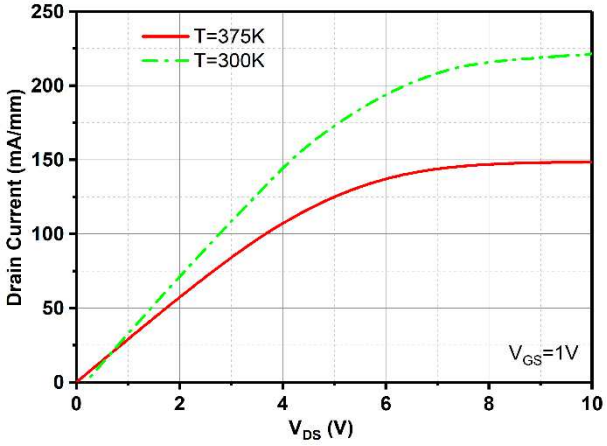


Fig. 5. Measured output characteristics of PSJ HFET at T_J=300K and 375K. and V_G=1V

annealed at 800 °C in N_2 ambient. Base electrode was formed

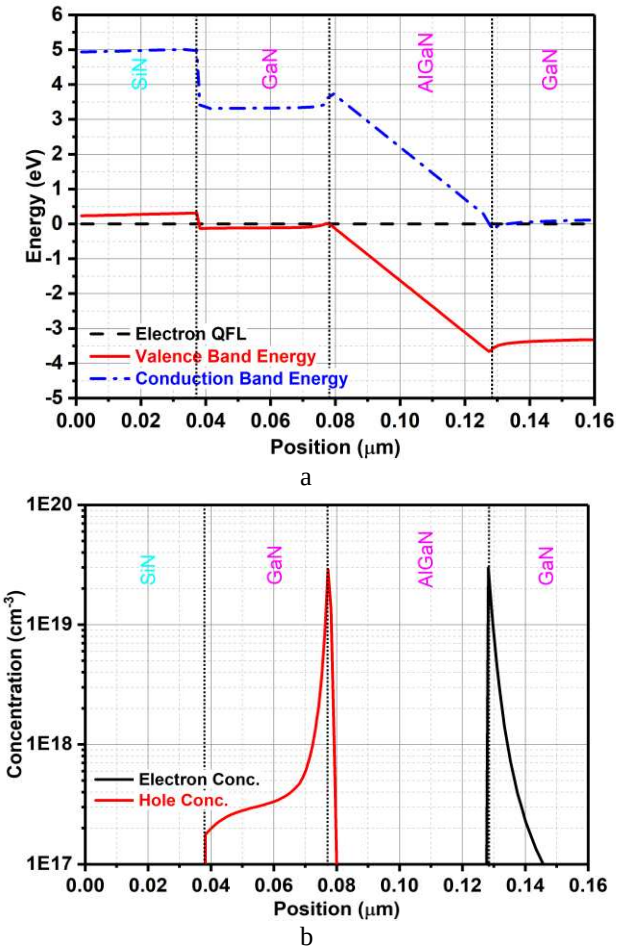


Fig. 6. (a) Energy Band Diagram (b) Carrier concentration of PSJ HFET

in a two-step process with an initial deposition of thin Ni/Au on the p-GaN mesa layer (20nm) followed by a 500 °C anneal in air (for ohmic contact to p-GaN layer/2DHG). This was followed by additional Ni/Au deposition to maintain continuity of metallisation from the surface of the mesa to pads. Gate electrode was formed using thermal evaporation of Ni/Au (Schottky contact to 2DEG). Finally, SiN passivation layer was deposited using PECVD over the

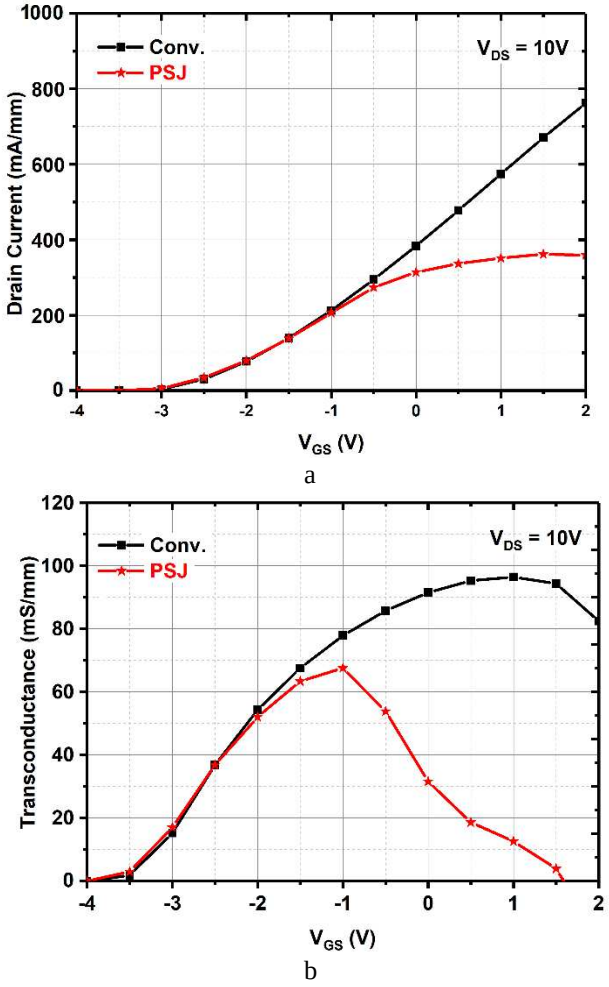


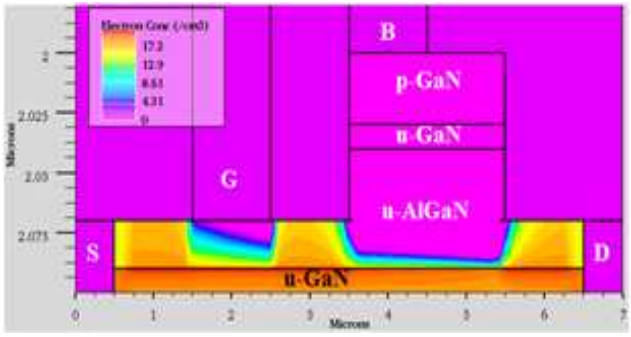
Fig. 7. Simulated (a) transfer I-V characteristics (b) Transconductance at T_j=300K

device area, and pads area etched to complete the fabrication process.

3. Electrical Characterisation Results

Figs.3 (a)-(b) show micrographs and simplified cross-sectional schematics of monolithically fabricated conventional HFET without FP (L_G=3μm, L_{GS}=3μm, L_{GD}=28.5μm, L_{DS}=34.5μm, Width=50μm) and PSJ HFET (L_G=3μm, L_{GS}=3μm, L_{GD}=24.5μm, L_{DS}=30.5μm, Width=50μm) respectively, used in this study.

Amongst the co-fabricated conventional and PSJ HFETs, those with equivalent geometrical and electrical characteristics were chosen for this evaluation. The devices are located within close proximity of each other and should therefore show minimal difference in electrical characteristics attributed to processing variations. Wafer-level electrical characterisation was performed using Agilent B1500A power device analyser. Measured transfer I-V characteristics and derived transconductance have been shown in Figs.4 (a)-(b) respectively. Both types of HFETs have identical threshold voltage (V_{TH} ~ -2V). At V_{DS}=10V, for the conventional HFET, saturation starts at Vgs≈1.5V and reaches a drain current of 430mA/mm at Vgs=2V, while saturation starts at Vgs≈1V and reaches a drain current of 270mA/mm at Vgs=2V for the PSJ structure at room temperature when the base electrode is connected to ground



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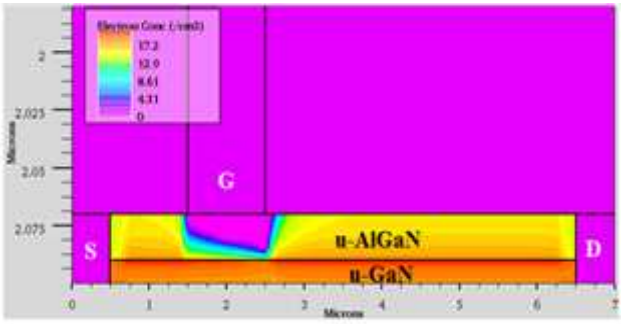


b

Fig. 8. Electron concentration at V_{DS}= 10V and V_{GS}= 1V (a) PSJ HFET (grounded base) (b) Conventional HFET

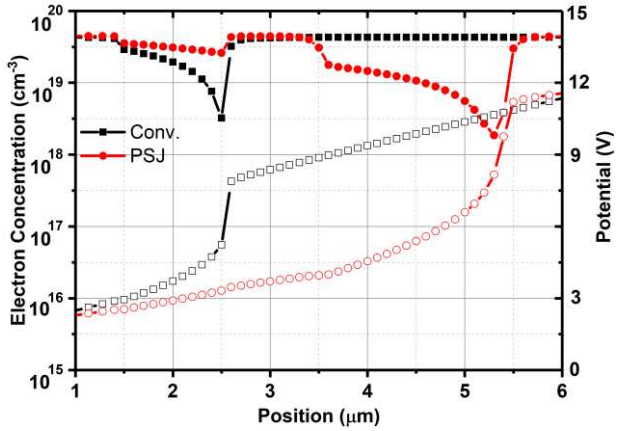


Fig. 9. Profiles of electron concentration (closed symbols) and potential (open symbols) along the AlGaN /GaN interface at V_{DS}= 10V and V_{GS}= 1V

potential. PSJ HFET also shows reduced transconductance at higher temperatures.

As can be observed from Figs.4 (a)-(b), linearity of the drain current over a wider range of V_{GS}, in conventional HFETs translates to a higher magnitude of peak transconductance (g_m) compared to that of a PSJ HFET. It should be noted that although having a high transconductance can be useful during power switching; it is a more critical parameter for radio frequency (RF) applications that require the transistors to operate primarily in the saturation region. Trade-off between transconductance characteristics and obtaining ideal charge balance condition within the device has been previously reported in Superjunction LDMOS on thick-SOI technology for RF applications [12].

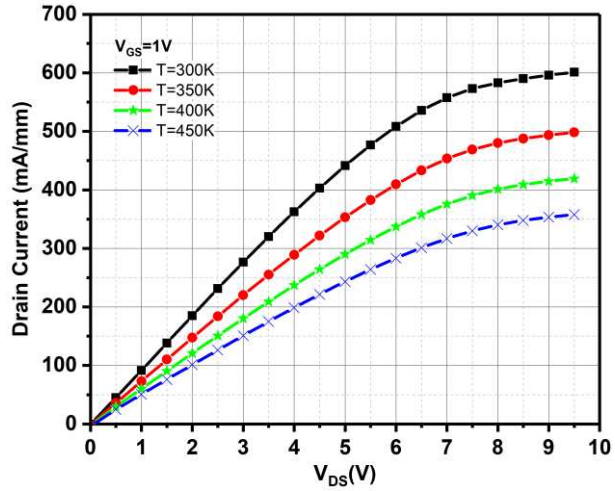
Fig.5. demonstrates the reduction of the drain saturation current with increasing temperature. As the concentration of 2DEG is almost independent of the temperature variation, the decrease in current can be largely attributed to reduction in 2DEG mobility, increased contact resistance between device metal contact and increased phonon related scattering [13].

4. Numerical Simulation Results and Analysis

Physics-based two-dimensional device simulations were performed using Silvaco ATLAS. The physical models included for simulation of the on-state characteristics were – POLAR (spontaneous polarisation), CALC.STRAIN (piezoelectric polarisation), SRH (Shockley-Read-Hall, carrier generation-recombination), and FLDMOB (field dependent mobility) to model electron mobility [14]. The energy band diagram and concentration of carriers (thermal equilibrium) within the drift region composed of the GaN/AlGaN/GaN double heterostructure (to be referred to as the PSJ region henceforth) of the PSJ HFET have been shown in Figs. 6 (a)-(b).

The geometry of simulated structures was set based on the actual design and processing parameters used for the fabricated devices. However, it is to be noted that the objective of this simulation study was to gain an insight on the physical mechanisms at play rather than fitting the exact experimental results. The p-GaN layer (under the base electrode) within the simulated PSJ structure was defined as a uniformly doped p-type region with a doping density of 3 x 10^{17} cm^{-3}. This definition accounts for incomplete ionisation and an activation of 1% within physical GaN structures doped with Mg concentration of 3 x 10^{19} cm^{-3} at 300K [15]. The rest of the regions were defined as undoped. Thickness of the AlGaN layer in conventional HFET was set as 20 nm. AlGaN thickness in PSJ HFET was set as 47 nm in the PSJ region and as 20 nm in the remaining access region between source and drain electrodes. Al mole fraction in the AlGaN layer was fixed as 23% in both structures. Simulated transfer I-V characteristics as well as derived transconductance at V_{DS}=10V, have been shown in Fig. 7 and appear to be generally aligned to the measured characteristics.

The differences observed such as simulated value of V_{TH} being ~ - 3 V (instead of - 2V for the actual structures), and generally higher normalised values of drain saturation current can be attributed to non-ideality (AlGaN thickness in the access regions post ICP etching and corresponding impact on 2DEG concentration, finite contact resistance.) that is introduced during physical processing of the structures. Based on TLM characterisation of test structures within the proximity of the devices, the specific contact resistance was estimated to be in the range of 10^{-4}-10^{-5} ohm.cm^2. I-V characteristics are essentially determined by the distribution of charge carriers (2DEG density) that are available and dependence of their transport characteristics under a given biasing condition. In order to understand the different drain current saturation characteristics between the conventional and PSJ HFETs, carrier distribution within the structures under various bias conditions was examined. Electron concentration within the simulated structures at V_{GS}=1V and V_{DS}=10V, have been shown in Figs. 8 (a)-(b). Profiles of the electron concentration and electric potential along the AlGaN



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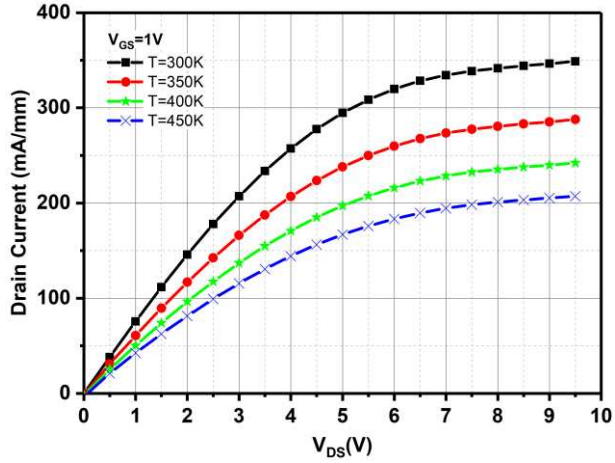

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Fig. 10. Simulated output characteristics of (a) conventional HFET and (b) PSJ HFET at V_{GS}=1V

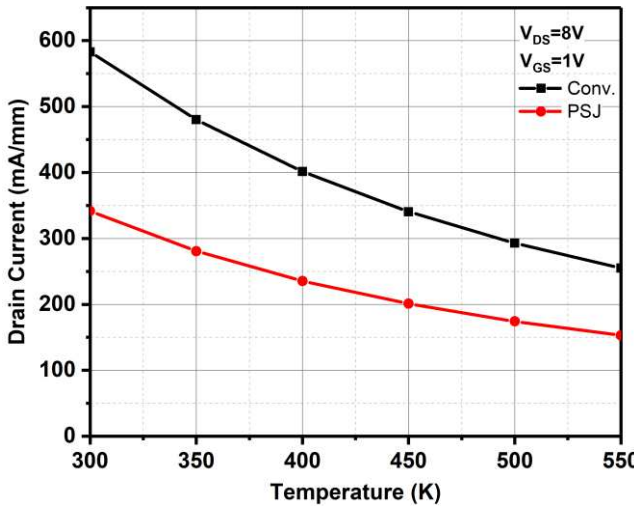

Fig. 11. Simulated temperature dependence of the saturation currents of conventional and PSJ HFET structures at V_{DS}=8V and V_{GS}=1V

(000$\bar{1}$)/GaN (0001) interface (at V_{GS}=1V and V_{DS}=10V) have been shown in Fig. 9.

It can be observed from Fig. 8 and Fig. 9 that the channel (region under the gate electrode) gets pinched-off at the drain-side edge of the gate when biased into the saturation region. This is observed in both conventional and PSJ HFET. However, in PSJ HFET, substantial depletion of electrons from the 2DEG is also observed under the PSJ region (GaN/AlGaN/GaN double heterostructure). Compared to the thermal equilibrium conditions, 2DEG density at the drain-side edge of the PSJ region reduces by more than an order of a magnitude at V_{DS} = 10 V under grounded base condition. As described in the earlier section of this article and as also shown in Fig. 6 (b), the PSJ region has inherent charge balance under thermal equilibrium in the GaN/AlGaN/GaN double heterostructure where positive and negative polarisation charges of equal charge density coexist at the AlGaN (000$\bar{1}$)/GaN (0001) interface with two-dimensional electron gas (2DEG) accumulation and GaN (000$\bar{1}$)/AlGaN (0001) interface with two-dimensional hole gas (2DHG) accumulation respectively. Although there is no metallurgical junction, a PN junction is formed effectively by the 2DHG (p-region) and 2DEG (n-region) intrinsically separated by a thin AlGaN layer (< 50 nm). Under high drain bias conditions, when the base (p-region) is connected to ground, the n-region formed by 2DEG is biased to a high potential, leading to a condition like reverse biasing of a PN junction. The reverse biasing occurs non-uniformly within the PSJ region (causing quasi-vertical depletion of carriers) as most of the drain-source potential (V_{DS}) drops along the PSJ region (as shown in Fig. 9). Due to this, the magnitude of pinch-off that occurs at drain-side edge of the gate is not as much as observed in conventional HFET where drain-source potential (V_{DS}) primarily drops along the channel. In both cases, as V_{GS} is increased, electrons depleted due to pinch-off are replenished only in the channel region. At this point, I_D saturates, as further increase in V_{GS} leads to forward biasing of the Schottky gate. In the case of PSJ HFETs, electrons depleted in the PSJ region are not modulated by the gate electrode, and saturation of I_D with a low magnitude is primarily determined by this physical behaviour.

The simulated output characteristics and temperature dependence of drain current saturation behaviour with variation in temperature from 300K to 450K are presented in Fig. 10 and Fig. 11 respectively. The results are closely aligned to experimental results within the measured temperature range. While both structures show reduced current level at higher temperatures, PSJ HFETs are expected to show superior saturation characteristics also at elevated temperatures.

Simulated breakdown characteristics and potential distribution along the lower AlGaN/GaN interface of a conventional HFET (with Gate FP) and the PSJ HFET are shown in Fig. 12 and Fig.13 respectively. Although only a single approach has been shown for comparison here, the authors recognize that there is no single method of designing high voltage GaN HFETs using metal FPs. The techniques can vary from using just Gate FP to including Source and Drain FPs as well as optimised combinations. The degree of device processing complexity varies depending on the adopted technique. With the scenario considered for numerical simulations, for a given drift length, significantly higher breakdown voltage can be achieved using PSJ without employing any metal FP. This makes PSJ technology based GaN power devices ideally suited for existing and emerging high temperature power electronic applications.

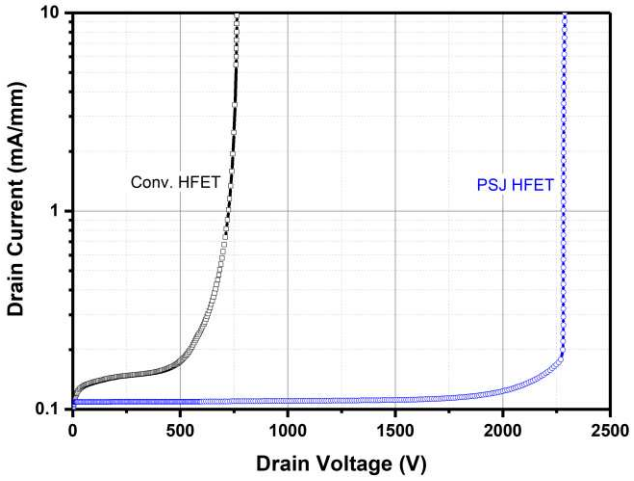

Fig. 12. Simulated breakdown characteristics of conventional HFET, and PSJ HFET structures at V_{GS}=-5V

5. Concluding Remarks

The ability to sustain and respond to inadvertent fault events during operation without compromising functionality and maintaining overall performance, is a key element that governs the health and long-term reliability of a power management system. Although the intelligence embedded in the fault detection and protection systems is crucial in achieving this, inherent power semiconductor device capability can be instrumental in devising innovative high-performance system level solutions. Polarisation Super Junction (PSJ) is a proven technology for developing ultra-high-performance power semiconductor devices in GaN. Attributed to its intrinsic design is also the capability to limit the drain saturation current density to levels that are almost half the magnitude of what is obtained in a conventional AlGaN/GaN HFET that can be achieved without compromising the normal on-state characteristics. The resulting enhancement in short-circuit capability can therefore be leveraged in the overall system-level design. This work presents a comprehensive analysis of drain current saturation behaviour in GaN PSJ HFETs combining electrical measurement data with the results of detailed physics-based device simulations.

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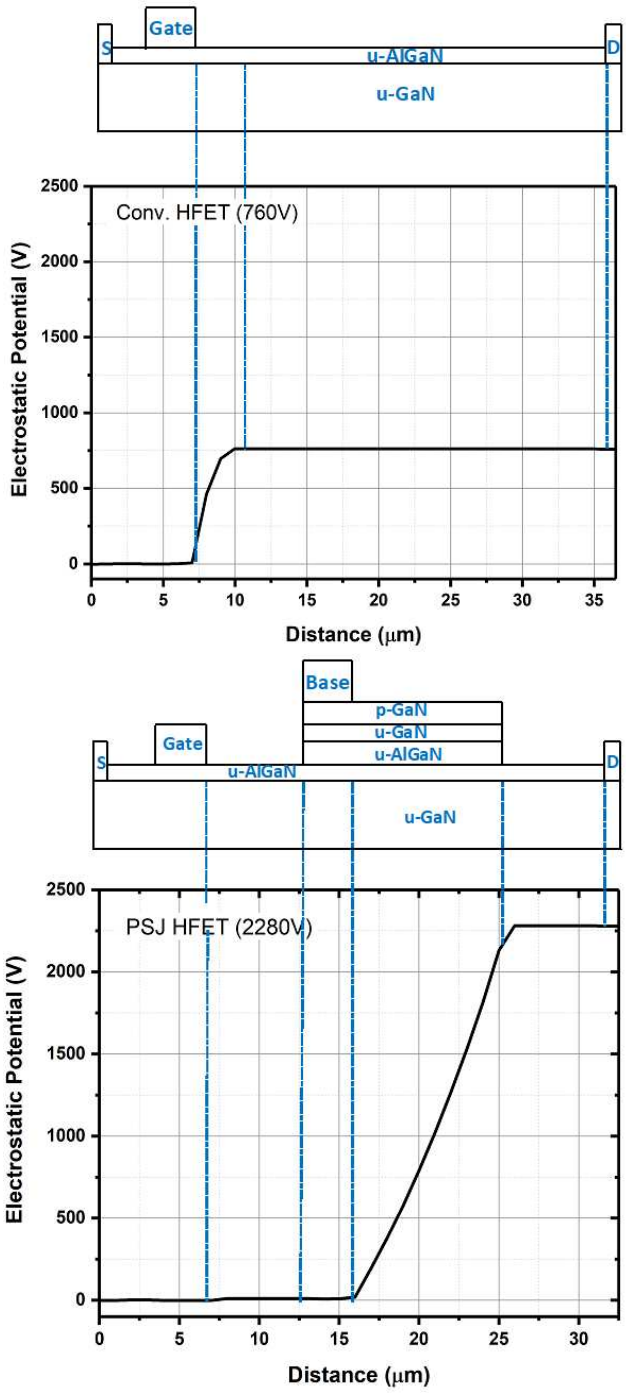

Fig. 13. Potential cutlines along the surface of structures before breakdown at V_{GS}=-5V.

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