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Field Plate Designs in All-GaN Cascode Heterojunction Field Effect Transistors

Sheng Jiang, Kean Boon Lee, Zaffar H. Zaidi, Michael J. Uren, Martin Kuball and Peter A. Houston

***Abstract*— Different source field plate connections are compared for the all-GaN integrated cascode device to address the capacitance matching and turn-off controllability issues reported in the conventional GaN plus Si cascode. Experimental results suggest that the cascode device with a field plate connected to the source terminal can significantly suppress the off-state internode voltage, leading to minimized capacitive energy loss and reduced overvoltage stress at the internode. This is attributed to the reduced ratio of the drain-source capacitance of the depletion mode cascode part to the total capacitance at the cascode internode. An additional field plate on the E-mode cascode part is proposed to further suppress the off-state internode voltage and benefit the device. Cascode devices with the source field plate connecting to the enhancement mode gate have an improved switching controllability via gate resistance during turn-off and hence enhanced dv/dt immunity in the drain loop.**

***Index Terms*—Power electronics, Semiconductor devices, Semiconductor switches, Semiconductor heterojunctions.**

I. Introduction

Cascode devices, with the advantage of a reduced Miller effect, are strong candidates for high voltage, high frequency applications [1-3]. An all-GaN integrated cascode configuration, shown in Fig. 1, was demonstrated with a superior hard switching performance at 200 V compared to the equivalent standalone GaN heterojunction field effect transistor (HFET) [1]. However, further optimization of the integrated cascode is still required to address several known issues from experience in the GaN plus Si hybrid cascode device [4-6], which also apply to the integrated cascode structure. First, the mismatch in intrinsic capacitances between the depletion mode (D-mode) and the enhancement mode (E-mode) devices can lead to an increased off-state voltage at the internode of the cascode configuration [4-5]. This overstress can drive the E-mode Si device into avalanche during the turn-off transient, causing additional losses for the hybrid cascode [4-5]. Although the avalanche effect does not apply to the all-GaN integrated cascode device, a large off-state internode voltage can increase both the breakdown voltage requirement of the E-mode part and capacitive energy loss at the internode. Second, the turn-off speed of the cascode devices is reported to be uncontrollable via the gate resistance (R_g) as a result of the reduced Miller effect, which can cause an issue when control over the switching speed is required to suppress the ringing effect [8-9].

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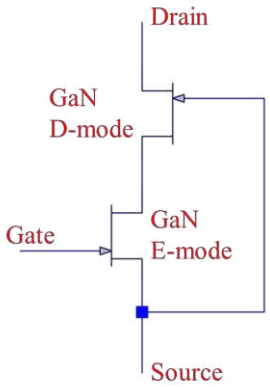


Fig. 1. Circuit diagram of an all-GaN integrated cascode configuration.

Adding an external capacitor between the drain and source of the Si device was proposed in [4] and [5] to match the capacitance in the hybrid cascode device and prevent the Si device from being driven into avalanche during turn-off. Likewise, external capacitors and resistors were proposed to improve the turn-off controllability issue for the cascode devices [8-9]. However, the use of external components has several drawbacks which includes additional parasitic inductance, and presents challenges in the device packaging [8-9].

Field plates (FPs) are commonly employed in GaN HFETs to moderate the surface electric field and hence lead to an increase in breakdown voltage and suppression of surface-related dynamic *Ron* [10-11]. In addition, FP incorporation may also lead to a change in intrinsic capacitances of the transistor depending on the connection method of the field plates [12-13]. Compared to standalone GaN HFETs, the FP of the D-mode part in the cascode device has the flexibility to connect to different locations without the worry of the Miller-effect, as the effective Miller capacitance is shifted to the gate-drain capacitance of the E-mode part ($C_{GD\text{-}E}$) [1]. In addition, different connections redistribute the FP induced capacitances and thus affect the switching behaviour of the cascode device. The connection of the FP is hence important to realize the full optimization of the integrated cascode device [1] but has not previously been discussed. In this study, we examine five different FP connections and compare their influence on the switching performance of the integrated cascode device. We shed new light on the effect of the different FP configurations and demonstrate how both capacitance matching and switching controllability issues can be addressed without increasing the parasitics.

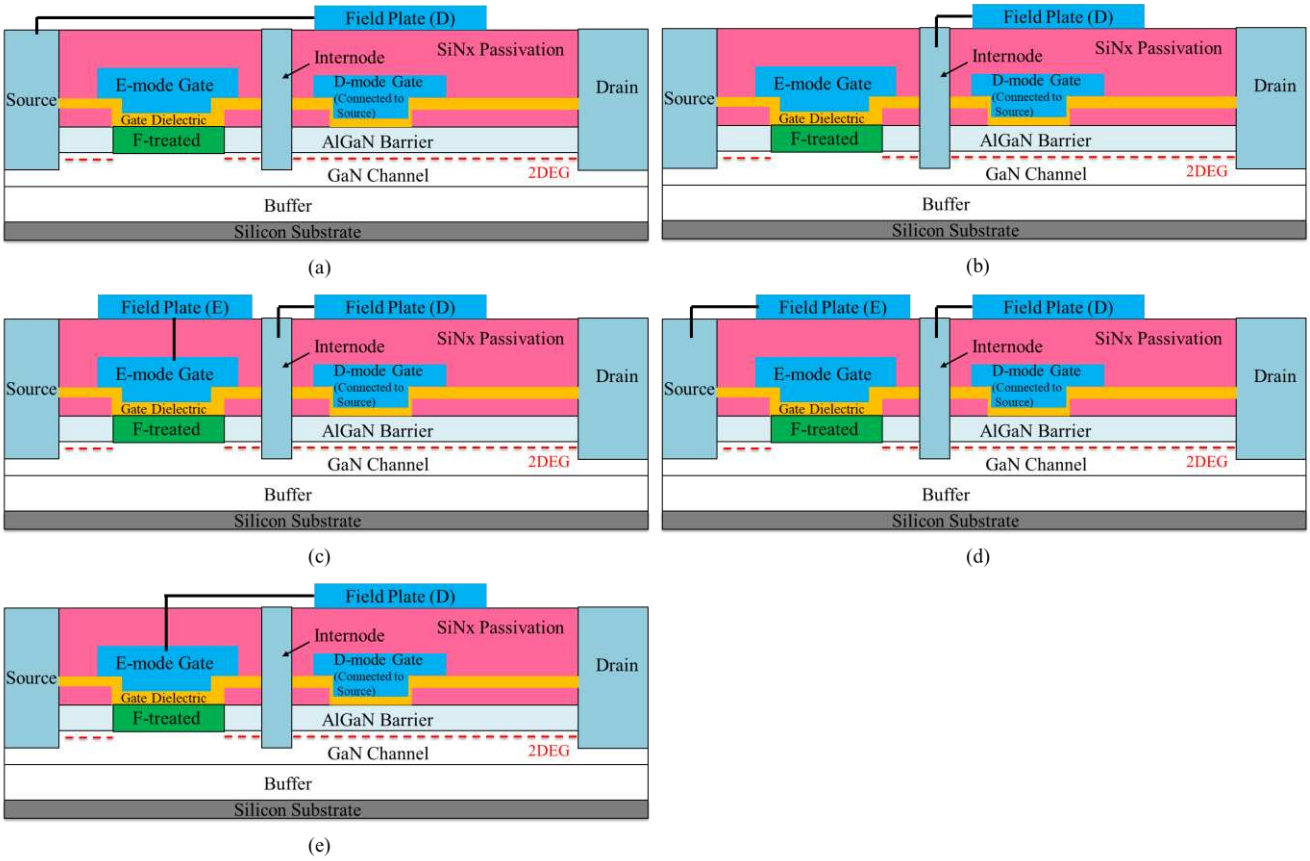


Fig. 2. A schematic diagram of all-GaN integrated cascode devices with five different field plate structures. (a) Device A with D-mode FP connected to the source of the cascode (b) Device B with D-mode FP connected to the internode pad (c) Device C with D-mode FP connected to the internode pad and E-mode FP connected to the E-mode gate (d) Device D with D-mode FP connected to the internode pad and E-mode FP connected to the source of cascode and (e) Device E with D-mode FP connected to the E-mode gate.

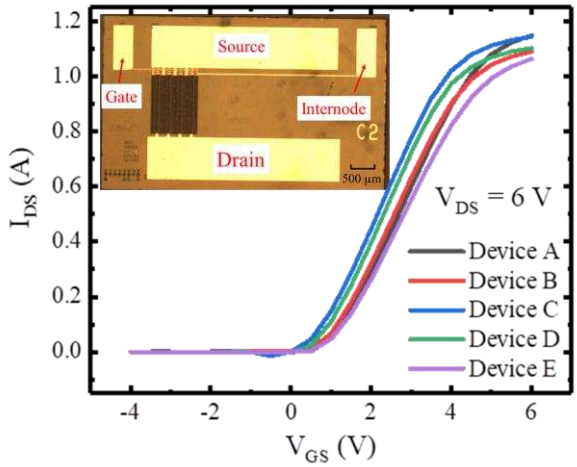


Fig. 3. Pulsed on-wafer gate transfer characteristics of Device A – E at V_{DS} = 6 V, quiescent V_{DS} / V_{GS} = 0 / 0 V, pulse width of 10 ms and pulse period of 100 ms. An optical image of the monolithically integrated AlGaN/GaN HFET cascode configuration with an additional internode contact pad (inset).

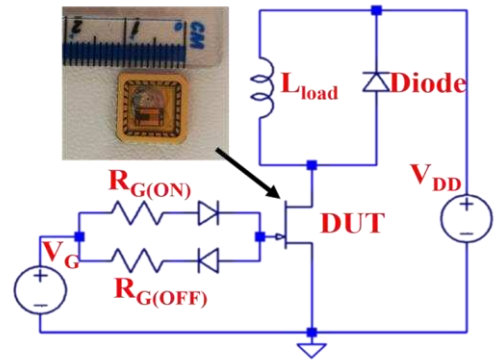
TABLE I
SUMMARY OF DIFFERENT FP CONNECTIONS

	E-mode FP connection	*D-mode FP connection*
Device A	No FP	Source of cascode
Device B	No FP	Internode
Device C	Gate of E-mode part	Internode
Device D	Source of cascode	Internode
Device E	No FP	Gate of E-mode part

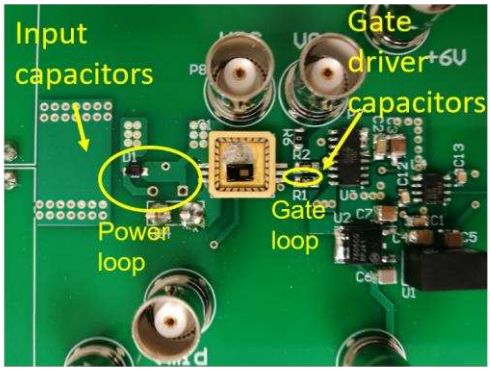
II. FP DESIGN AND DC CHARACTERISTICS

Fig. 2 shows the all-GaN integrated cascode device with five different FP structures (Device A - E) All devices were fabricated on a GaN-on-Si substrate with the standard GaN HFET fabrication procedure described in [1]. The E-mode operation was achieved by CHF_3 plasma-treatment in a reactive ion etch (RIE) system plus a nominally 20 nm thick SiN_x gate dielectric. The D-mode gate also features a metal-insulator-semiconductor (MIS) structure with 20 nm thick SiN_x to improve the current handling of the integrated cascode device [1]. 70 nm SiN_x was deposited using plasma enhanced chemical vapour deposition as the first passivation to support the T-shape gate wings and 200 nm SiN_x was used as the second passivation for the FPs. The E-mode parts for all devices have a gate width of 8 mm, gate length of 1.5 µm, source-drain separation of 6.5 µm and gate wing of 1 µm. While the D-mode parts have the same dimensions, except for a larger source-drain separation of 16 µm to withstand the high voltage. The device parts are separated by an internode ohmic contact of 10µm length. All devices have a FP extension (L_{FP}) of 2 µm on the D-mode part.

Device A (Fig. 2(a)) and B (Fig. 2(b)) have a D-mode FP only connected to the source of the cascode and the internode pad, respectively. Device C (Fig. 2(c)) and D (Fig. 2(d)) are based on Device B with the same D-mode FP connection, except for an additional FP with extension of 1 µm on their E-mode parts connected to the E-mode gate and to the source of cascode, respectively. Device E (Fig. 2(e)) only has a FP on its D-mode part which is connected to the E-mode gate. Table. 1 shows the summary of different FP connections for



(a)



(b)

Fig. 4. (a) Circuit diagram of double pulse tester for switching speed measurement. (b) Circuit implementation.

all fabricated devices.

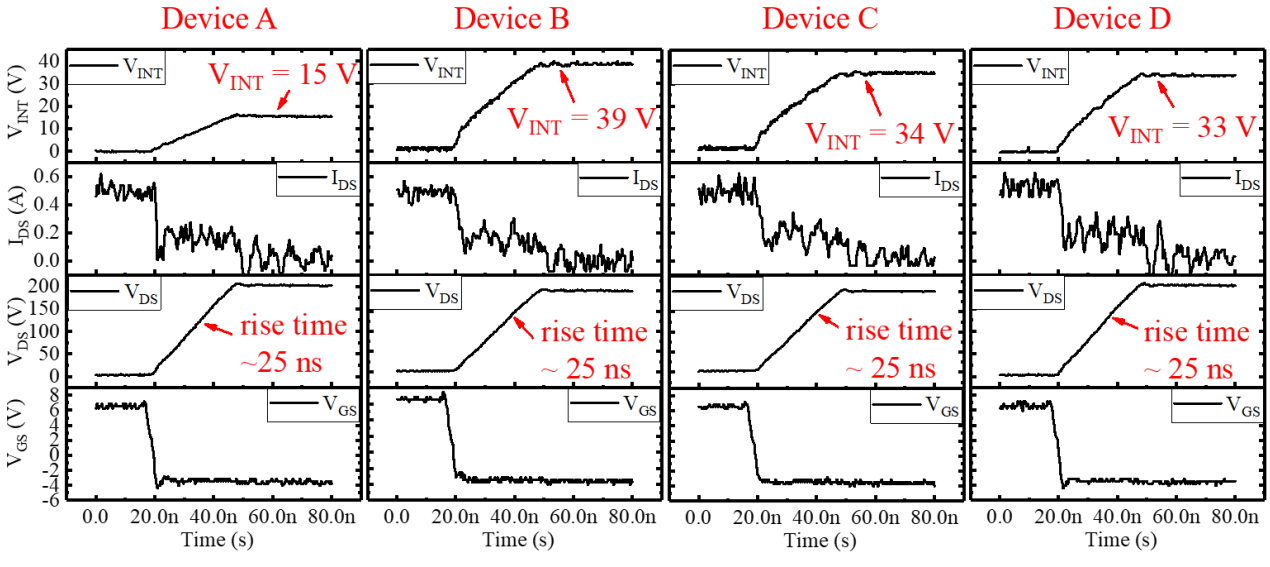
An additional pad to access the internode of the cascode was added to all multi-finger cascode devices, enabling the potential at the internode to be monitored during the switching measurements (inset in Fig. 3). Devices exhibit similar DC characteristic as shown in the on-wafer gate transfer measurement results in Fig. 3. Output currents > 1 A and threshold voltages of the E-mode part ($V_{th\text{-}E}$) > 0 V were achieved for all 8 mm cascode devices. Devices are capable of 200 V operation with drain leakage current below 10 µA/mm.

III. Experimental Setup

The switching performance was measured by an inductive load double pulse tester (DPT) as described in [1]. Fig 4(a) illustrates the circuit diagram of the DPT. Device under test (DUT) was wire-bonded onto commercial air cavity quad flat no lead (QFN) packages (shown in the inset of Fig. 4(a)) to minimize the parasitics [14]. A commercial gate driver IX2204 was used to drive the devices from V_{GS} = -2 V to +6 V. A Coilcraft 470 µH shielded power inductor was used as load inductor and an Onsemi 200 V Schottky diode MBR2H200SF was used as the freewheeling diode. Fig. 4(b) shows the picture of the assembled DPT. The input and gate driver capacitors are placed close to the DUT to minimize the loop distance and thus the parasitic inductance, as highlighted in Fig. 4(b). To prevent the noise from the load coupling into the gate loop, the power and gate loop were also separated, achieved by a source-sense connection in the device packaging. The gate voltage (V_{GS}), internode voltage (V_{INT}) and drain voltage (V_{DS}) were measured using a digital oscilloscope. The drain current (I_{DS}) was monitored by a high bandwidth current sensing resistor T&M SDN-414-10 connected to the source of the DUT.

IV. Results

Fig. 5 shows the turn-off switching waveforms of V_{GS}, V_{DS}, I_{DS} and V_{INT} for Device A, B, C and D at a drain voltage of 200 V, load current of 0.5 A and gate resistance of 10 ohm. Voltage rise times around 25 ns are observed for all devices, extracted from 10 % to 90 % of the operating voltage (V_{DD}). I_{DS} was measured from the voltage across a 0.1 ohm current sensing resistor resulting in less than 50 mV output. While the roughness of I_{DS} is in tens of mV and is consistent with that of V_{GS}, V_{DS}, and V_{INT}, the waveforms of I_{DS} appear to be noisier. This is due to the waveforms of I_{DS} being displayed at 50 mV/div, compared to 10 V/div, 50 V/div and 20 V/div used for V_{GS}, V_{DS}, and V_{INT}. In addition, the step down in I_{DS} is due to the charging of the parallel capacitance in the



(a) (b) (c) (d)

Fig. 5. Switching waveforms of V_{GS}, V_{DS}, I_{DS} and V_{INT} for (a) Device A (b) Device B (c) Device C and (d) Device D, captured at 10 V/div, 50 V/div, 50 mV/div and 20 V/div, respectively.

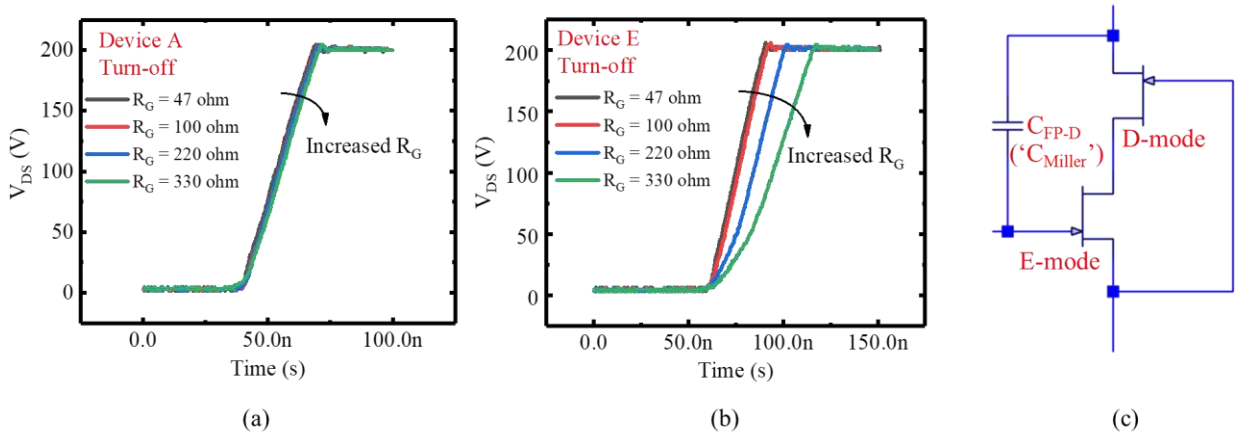


Fig. 6. Turn-off switching waveforms of V_{DS} for (a) Device A and (b) Device E. (c) The equivalent circuit diagram of C_{FP-D} for Device E.

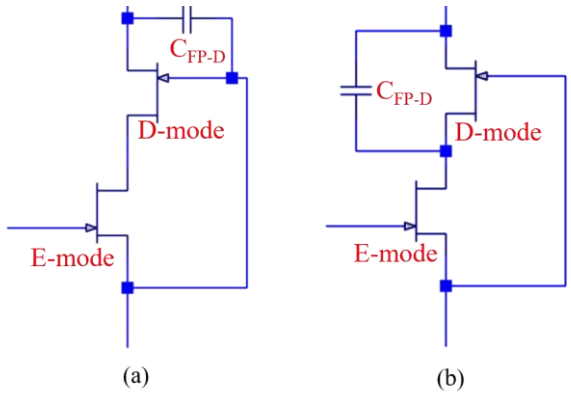


Fig. 7. Equivalent circuit diagrams showing FP induced capacitance in (a) Device A and (b) Device B.

freewheeling diode in the DPT circuit, which will not influence the comparison. On the other hand, V_{INT} varies in the devices with different FP connections. Device A exhibits V_{INT} of 15 V which is the lowest among all devices, while Device B shows the highest (39 V), as shown in Fig. 5(a) and (b), respectively. Device C and D with an additional FP on the E-mode part compared to Device B, exhibit similar V_{INT} close to 33 V, as shown in Fig. 5(c) and (d).

The turn-off controllability via R_G was compared between Device A and Device E with the same switching conditions of V_{DS} = 200 V and I_{DS} = 0.5 A. R_G was varied from 47 ohm to 330 ohm, in order to observe the change in the voltage rise time between the two devices. Fig. 6 (a) and (b) shows the switching waveform of V_{DS} during turn-off for the Device A and Device E, respectively. Device A, as a typical cascode device, shows little control over the voltage rise time with different R_G, consistent with other reported literature on hybrid cascode devices [8-9]. On the other hand, Device E exhibits 100 % increase (25 ns) in the switching time when R_G is varied from 47 ohm to 330 ohm. This is due to the additional 'Miller capacitance' (C_{Miller}) induced by the FP connected to the gate of the E-mode part in Device E, as shown in the equivalent circuit in Fig. 6 (c). As a result, the turn-off switching controllability is improved and can be further enhanced by increasing the FP induced capacitance (C_{FP-D}).

V. Discussion

Despite the different FP connections, Device A – D exhibit similar drain voltage rise times, which is expected as the drain voltage transition during turn-off for the cascode device is mainly determined by the load current and the output capacitance (C_{GD-D} + C_{DS-D}) of the D-mode part [1]. The capacitances at the internode (C_{INT}), which are dependent on FP connection, include the gate-source capacitance of the D-mode part (C_{GS-D}), the gate-drain capacitance of the E-mode (C_{GD-E}) and the drain-source capacitance of the E-mode part (C_{DS-E}). They have little effect on the drain voltage rise time and can be ignored, provided C_{INT} is significantly larger than C_{DS-D} [15]. Meanwhile, the connection difference in the D-mode FP of Device A and Device B (C and D) does not change the geometric capacitance induced by the FP and thus is expected to yield similar switching speed as observed.

TABLE II
Comparison of Calculated and Measured Off-State V_{INT} for Devices A - D

	V_{INT} (Calculated based on device geometries)	V_{INT} (Calculated based on CV measurements)	V_{INT} (Measured)
Device A	17 V	16 V	15 V
Device B	45 V	39 V	39 V
Device C	42 V	33 V	34 V
Device D	42 V	33 V	33 V

FP connections in Device A and B lead to a different ratio of C_{GD-D} and C_{DS-D} and hence affect the off-state V_{INT} as observed. To explore the reason for this, the principle of the increase in V_{INT} in the turn-off transition is now explained. During turn-off, assuming the gate resistance is small enough to prevent the Miller effect from controlling the switching speed of the E-mode part, the E-mode channel is pinched off first, after the gate-source voltage of the E-mode part (V_{GS-E}) drops below V_{th-E}. V_{INT} then starts to increase and pinches off the D-mode channel when it reaches the D-mode threshold voltage (V_{th-D}). After both D-mode and E-mode channels are pinched off, the entire load current shifts into C_{GD-D} and C_{DS-D} to drive the drain voltage rise. The displacement current in C_{DS-D} flows into the internode and charges up C_{INT} [7]. The charging of C_{INT} completes at the same time as the drain voltage transition and is assisted by the displacement current in C_{DS-D}.

Assuming negligible off-state leakage in both D-mode and E-mode parts [6-7] and the gate drive current is sufficiently high that the Miller effect does not control the switching speed, the off-state V_{INT} can be approximated by the voltage division of C_{DS-D} and C_{INT}, and is given by

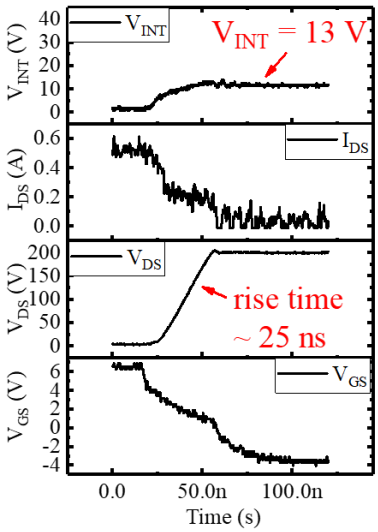


Fig. 8. Switching waveforms of V_{GS}, V_{DS}, I_{DS} and V_{INT} for for Device B with $R_{G(OFF)}$ = 330 ohm, captured at 10 V/div, 50 V/div, 50 mV/div and 20 V/div, respectively.

$$V_{INT} \approx \frac{C_{DS-D} * V_{DD}}{C_{DS-D} + C_{INT}} - V_{th-D} \quad (1)$$

This approximate expression shows that the capacitance matching in a cascode device depends on the ratio of C_{DS-D} to (C_{DS-D} + C_{INT}). By estimating the capacitance based on the device geometries and capacitance-voltage (CV) measurements on standalone devices with equivalent FP geometries, V_{INT} can be calculated using (1) and shows reasonable agreement with the experimental results for all devices (Table. 2).

Device B with the FP connected to the internode pad, increases C_{DS-D}, as illustrated in the equivalent circuit diagram in Fig. 7(a). In contrast, Device A has a reduced C_{DS-D} but larger C_{GD-D} due to the connection of the FP to the source of the cascode, as shown in Fig. 7(b). According to (1), a larger C_{DS-D} can result in an increased ratio of C_{DS-D} to (C_{DS-D} + C_{INT}), and thus an increased V_{INT} and capacitive energy loss ($1/2 * C_{INT} * V_{INT}^2$), as observed from Device B. Note that C_{GD-D} is connected to ground and does not contribute to the Miller effect in the cascode. Therefore, there is no penalty to increase C_{GD-D} for a reduced C_{DS-D}, as observed in Device A.

Note that both Device A and B show off-state V_{INT} larger than -V_{th-D} (-6 V), and it will become larger at higher voltage operation (ie >200 V) as indicated in (1). One route to reduce the internode voltage during turn-off, is to increase the turn-off gate resistance ($R_{G(OFF)}$) as shown in Fig. 8, which shows the switching waveforms of device B under the same conditions except for a larger gate resistance of 330 ohm. Similar drain voltage rise time (25 ns) is observed compared to the results with $R_{G(OFF)}$ = 10 ohm. This is also observed for Device A as shown in Fig. 6(a), and is because $R_{G(OFF)}$ mainly controls the switching speed of the E-mode part in the cascode [8-9]. On the other hand, V_{INT} was reduced to 13 V. Note that (1) is no longer valid for the estimation of V_{INT}, since the equivalent circuit cannot be regarded as a voltage divider consisting of two series connected capacitors (C_{DS-D} and C_{INT}). When $R_{G(OFF)}$ is large enough to cause the Miller-effect to control the switching speed of the E-mode part, the displacement current cannot be fully consumed by charging C_{INT}, which is limited by the insufficient gate

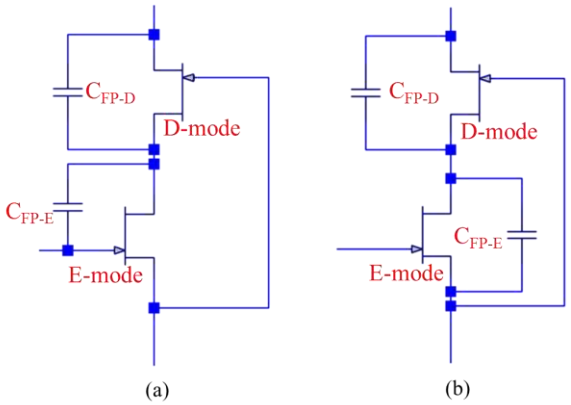


Fig. 9. Equivalent circuit diagrams showing FP induced capacitance in (a) Device C and (b) Device D.

driving current through C_{GD-E}. As a result, part of the displacement current flows through the E-mode channel instead, leaving less current to charge C_{INT}, and therefore, V_{INT} is reduced. However, the use of a large $R_{G(OFF)}$ is not desirable to reduce V_{INT}, because it does not lead to a reduction in the total capacitive energy loss at the internode [7]. Part of the energy which is supposed to charge C_{INT} to the voltage determined by the capacitance ratio (C_{DS-D}/C_{INT}), is dissipated earlier due to the Miller effect (turn-on of the E-mode channel during turn-off) [7]. In addition, a large $R_{G(OFF)}$ can cause a slow switching speed of the E-mode part and limit the overall operating frequency of the cascode device.

Alternatively, we added a FP to the low voltage E-mode part to further reduce the ratio between C_{DS-D} and (C_{DS-D} + C_{INT}), as shown in the equivalent circuit for Device C and D in Fig. 9. The E-mode FP in Device C is connected to the gate of the E-mode part and the FP induced capacitance (C_{FP-E}) is added to C_{GD-E}. On the other hand, the E-mode FP in Device D acts as a source-connected FP in the E-mode part and C_{FP-E} is added to C_{DS-E}. As a result, the off-state V_{INT} is reduced to ~33 V for both devices, 12 % less compared to Device B, as shown in the switching results in Fig. 5. V_{INT} of Devices C and D are still relatively large compared to that of Device A, mostly due to the small value of C_{FP-E}. This could be optimized by varying the thickness of the SiN_x underneath the E-mode FP. However, the minimum value of V_{INT} during turn-off is -V_{th-D}, and an over-engineered C_{INT} can cause delay in the turn-off of the D-mode part and should be carefully designed.

Overall, an FP connected to the source of the cascode (Device A) is preferable as it results in the lowest off-state V_{INT} and thus the smallest capacitive energy loss at the internode. To further suppress V_{INT} for higher voltage operation (>200 V), an additional FP on the E-mode part of Device A can be implemented by connecting to the source of the cascode (Device D) to increase C_{INT} and hence reduce the ratio of C_{DS-D} to (C_{DS-D} + C_{INT}). Here, the E-mode FP structure of Device D is preferable to Device C because the C_{FP-E} in Device C increases the effective Miller capacitance (C_{GD-E}) of the cascode and can limit the switching performance [1].

VI. Conclusion

Different FP connections in all-GaN integrated cascode transistors were compared in order to match the capacitance and improve the turn-off controllability internally without the worry of additional parasitics. Experimental results showed

that a D-mode FP and an additional E-mode FP both connected to the source terminal of the cascode device was optimum for the minimization of the off-state internode voltage leading to reduced overvoltage stress and capacitive energy loss at the internode. Alternatively, connecting the D-mode FP to the gate of the cascode provides additional 'Miller capacitance' and enables the device to be slowed down via gate resistance when necessary.

VII. Acknowledgment

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