
Proceedings Paper:
Petersen, A., Stone, D.A., Foster, M.P. orcid.org/0000-0002-8565-0541 et al. (1 more author) (2018) An investigation into the thermal benefits of multilevel converters. In: IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society. IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, 21-23 Oct 2018, Washington, DC, USA . IEEE . ISBN 978-1-5090-6684-1

https://doi.org/10.1109/iecon.2018.8591675

An Investigation into the Thermal Benefits of Multilevel Converters

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***Abstract*— This paper investigates the benefits of distributing thermal load across multiple devices on a single heatsink, with a focus on how this might be a benefit in the use of multilevel converters. The analysis uses finite element modelling to derive trends in performance, which combined with real world data permits for a bulk analysis in to whether multilevel converters have thermal benefits, and if so, to how great an extent. The paper concludes that there are significant and quantifiable benefits to distributing the thermal load, but high order multilevel converters may yield little benefit over lower order systems.**

Keywords—thermal modelling, finite element, multilevel

I. Introduction

Multilevel converters are a technology that have a large body of existing research and a wide range of industrial applications. For instance, multilevel converters show great promise in the development of next generation grid-attached battery energy storage systems (BESS). In this application a cascaded H-bridge multilevel converter can do much of the work that would normally be done by a separate battery management system (BMS) [1-4], and even allow dynamic avoidance of degraded string elements, potentially facilitating the use of second life and degraded batteries. With grid-attached energy storage forming an essential part of future power grids around the world, as they grow smarter and cleaner [5], new and improved technologies in this field are surely in high demand.

Multilevel converters also have benefits in motor drives applications, largely arising from the lower dV/dt for a given switching frequency. This results in lower total harmonic distortion (THD) [6-8], as well as lower overall noise [9].

That said, multilevel converters currently see very little use in industry. It is the opinion of the authors that a contributing factor to this lack of uptake is that the existing body of research focuses on specific benefits, such as integrated BMS in BESS applications or reduced THD, but there is little to no hard, quantitative analysis of more general costs and benefits in the design and implementation of this class of power converter. This paper seeks to explore and evaluate what, if any, benefits there may be in multilevel converters from the perspective of system thermal performance.

It seems reasonable that there would be benefits to distributing a thermal load more evenly across a heatsink. In the extreme case of just one device mounted to a heatsink, there will be a significant local hotspot where the device is mounted, increasing peak heatsink temperature and, ultimately, junction temperature. The same amount of power dissipated over a larger number of devices spread evenly across a heatsink would presumably suffer from this less – but to how great an extent?

II. Finite Element Investigation

A. Finite Element Thermal Trends with More Devices

Steady-state thermal finite element modelling (FEM) will form the core of the analysis. The large number of test permutations make an experimental investigation prohibitive, as well as the practical difficulty of measuring temperatures in enclosed thermal interfaces without skewing results. The accuracy of the results generated will therefore be based on the coefficients selected to define material properties which, without validation, may challenge the validity of the results. Therefore, the dependency of the results and conclusions on these unvalidated coefficients will be assessed.

To focus the scope of the analysis, a converter specification was created. As it is pertinent to the authors' ongoing research, a domestic scale BESS will be considered. The relevant reference converter specifications are:

- Nominal 500V DC link
- Maximum RMS power capacity of 6kW
- Cascaded H-Bridge configuration

While this is not a complete converter specification, no additional parameters are required for the purposes of these analyses. For reference, a generalised cascaded H-bridge converter is shown in figure 1.

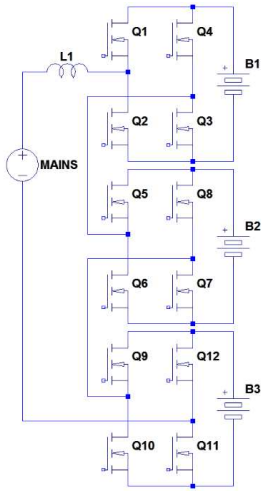

Fig. 1 A simplified schematic of a cascaded H-bridge multilevel converter

FEM simulations were run for a generic heatsink design, with both one device and many devices, in this case twenty-five. In both cases the total power dissipation is the same. This is reasonable, as it has been demonstrated that a higher order multilevel converter needn't have higher total power dissipation [10]. The results for the two instances can be seen in figure 2, and show that there is indeed a great thermal

benefit gained, with a reduction in heatsink temperature under the device of 83.9°C.

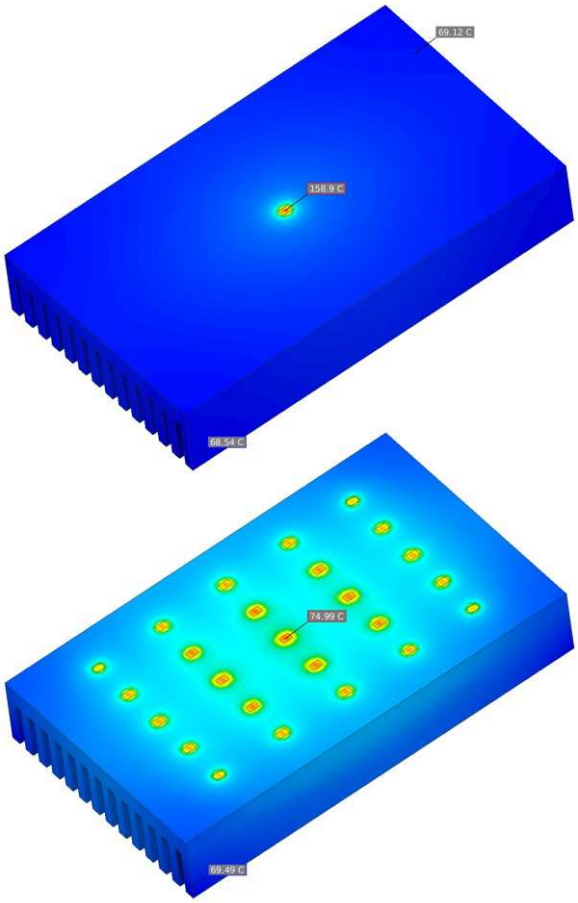

Fig. 2 A comparison of FEM results in the case of a single device dissipated as opposed to many devices.

In order to explore the trend in greater depth, this process was repeated a number of times, from just one device up to twenty-five, in intervals that are easily arranged geometrically: i.e. one by one, one by two, two by two, two by three, etc. The data was plotted as number of devices on the heatsink against peak heatsink temperature, and a line of best fit was found. Said plot is shown in figure 3.

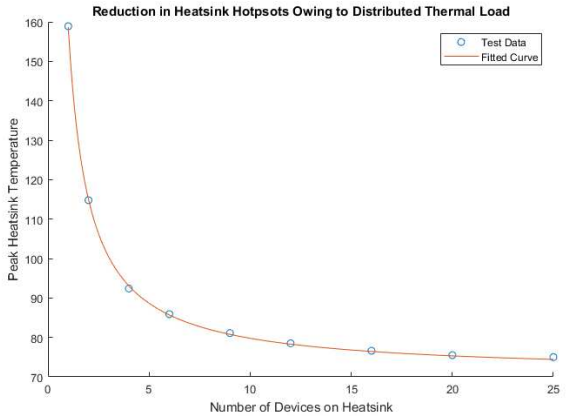

Fig. 3 The resulting trend line from a series of FEM simulations as the number of devices mounted an the heatsink increases, all else being equal.

After some exploration, the optimal best fit curve was found to be of the form shown in equation 1 (r>0.99).

$$y = ax^b + c \quad (1)$$

While this grants us the trend for a heatsink in isolation, that is of little practical use as FEM for almost every case has already been done to grant us this result, which would have already given any results for this heatsink. A solution that requires thousands of FEM iterations should be avoided, if possible.

Furthermore, this is the trend for a single heatsink with unvalidated material property estimations. To allow large scale investigation without large scale FEM and parametric validation, requires further analysis.

To this end, several heatsinks with different power dissipations, material parameters and physical dimensions were simulated in the same way as before to explore whether the trends are independent of these quantities, excusing the unvalidated coefficients (to an extent) and significantly reducing required FEM. The properties of these heatsinks are outlined below in table 1 (all credible values for aluminium) with renders of the heatsink models used shown in figure 4.

	Heatsink Number			
Heatsink Parameters	***1***	***2***	***3***	***4***
Convection Coeff. (W/m²K)	10	12	9	10
Convection Temperature (°C)	20	30	25	28
Emissivity	0.2	0.25	0.2	0.18
Radiation Temperature (°C)	200	180	210	200
Total Power Dissipated (W)	100	100	30	40
Length (mm)	600	500	150	240
Width (mm)	600	300	120	120
Depth (mm)	25	85	50	97

Table. 1 A table of the parameters used in the analyses with results shown in figure 5.

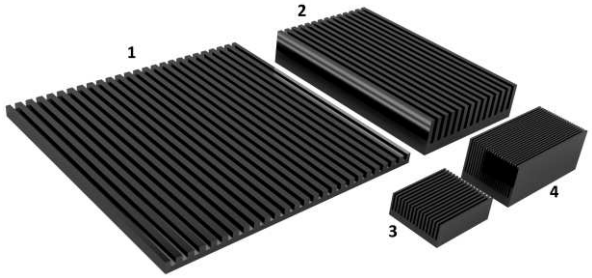

Fig. 4 Renders of the 3D heatsink models used in the analyses to follow. Numbers correspond to those used in table 1.

The results from these were subjected to the same analysis as before. After some experimentation, two key simplifications to the fit function were made. Firstly, the exponent (quoted as *b* in equation 1), was given a fixed value of -1. This was extremely close to the coefficient found for the fit in figure 3. Also, the coefficient *c* (see equation 1) was set to the heatsink average temperature – a figure given by the FE environment and independent of peak temperature. This stands to reason as surely as number of devices tends to infinity, the heatsink will become evenly heated. With these simplifications there is now only one unknown to be solved for, which can therefore be found from a single FEM run. The results of this set of FE simulations and their respective fits are shown in figure 5.

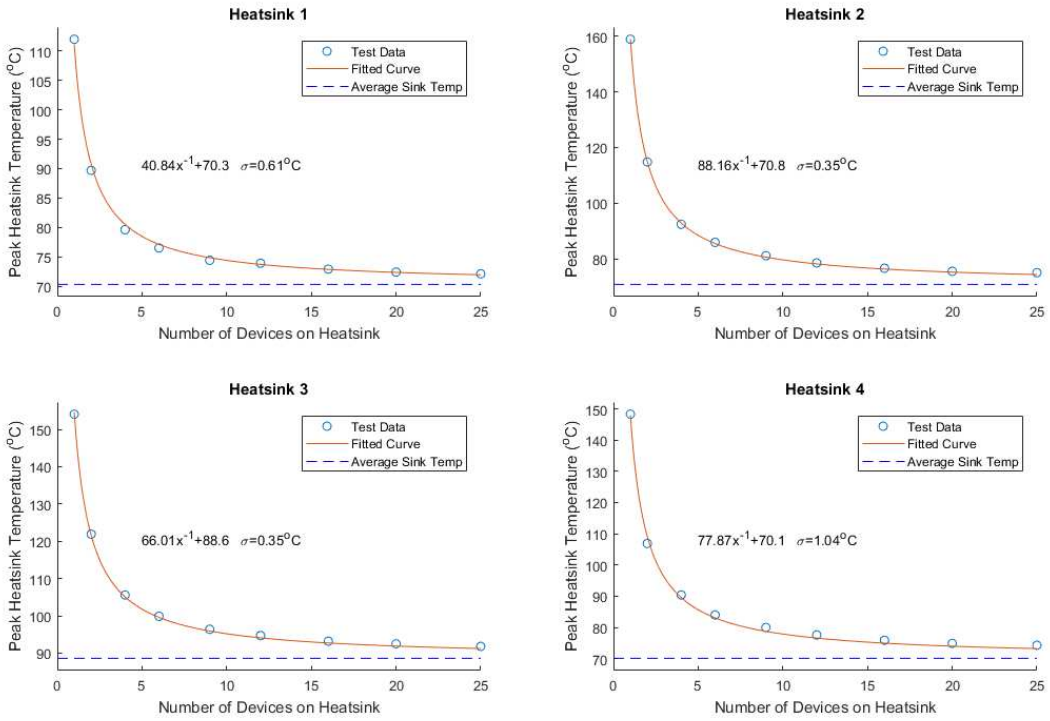

Fig. 5 The resulting trend line from a series of FEM simulations as the number of devices mounted an the heatsink increases, all else being equal, under the four configurations described in table 1. Standard deviation of fitted curve is shown each plot as σ.

Figure 5 shows that in all cases there is a good fit, with small standard deviations and adjusted-r values >0.99 in all cases. Therefore, it can be said that the simplified formula for describing this trend is sound and allows predicting trends from only one datapoint to solve the one unknown. This permits the running of just one FEM model to predict trends over many permutations.

B. Finite Element Thermal Trends with Thermal Pad Size

The key benefit afforded by the use of multilevel converters is that as number of levels in the converter increases, the designer gains access to lower voltage rated devices, which can have higher performance than their higher voltage counterparts in almost all ways. One key, relevant exception to this is that these devices tend to be physically smaller. To investigate whether this has a significant effect, much as before, a pair of FEM runs with a given heatsink under two extremes of pad size, with all other parameters identical, were performed. The results are shown in figure 6.

Figure 6 shows, much as before with number of devices, that pad size does indeed have a significant impact of peak heatsink temperature. To find an expression that describes the relationship between the impact on the peak heatsink temperature and the pad size, the same method as before was utilised. A range of standard packaged were represented in the pad sizes considered:

- TO-247 at 192mm^2
- TO-220 at 120mm^2
- D^{2}PAK at 48mm^2
- TDSON-8 at 16mm^2
- TSDSON-8 at 4mm^2

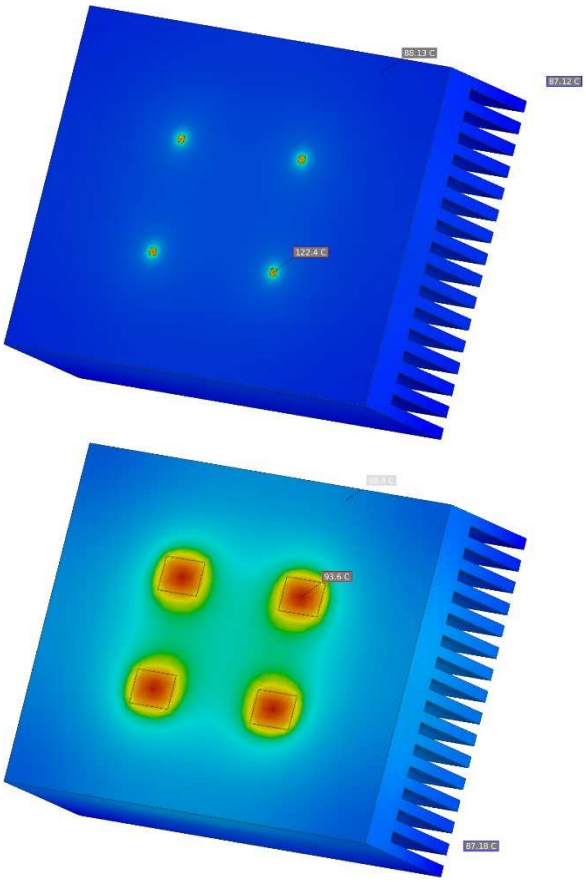

Fig. 6 A comparison of FEM results in the case of four small devices dissipated as opposed to four large devices.

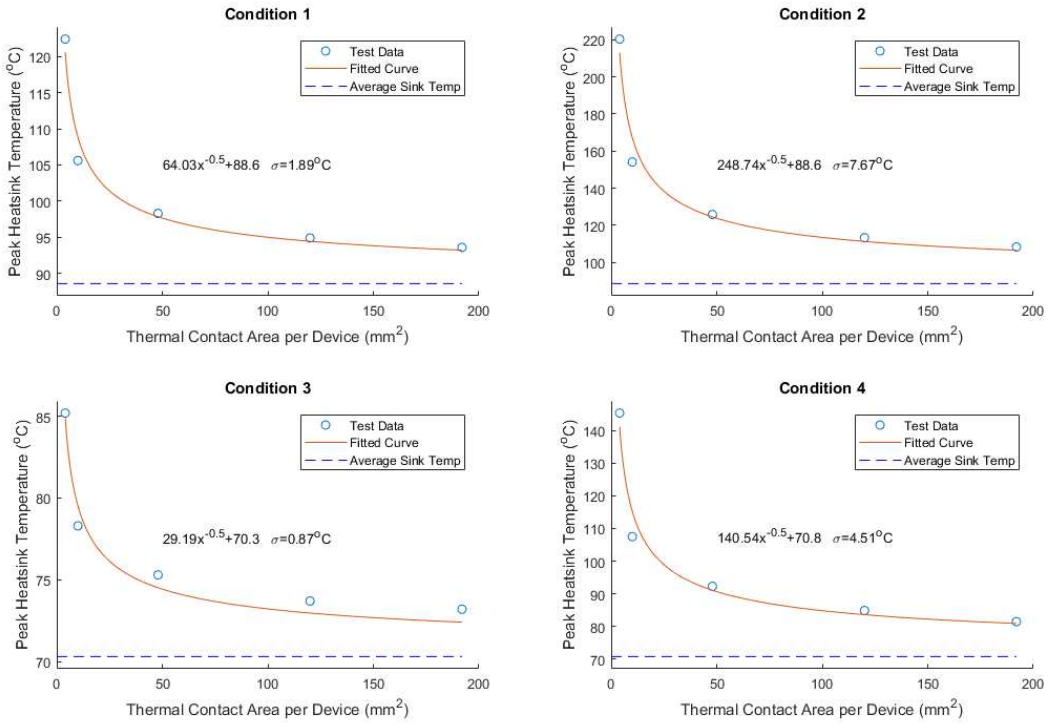

Fig. 7 The resulting trend line from a series of FEM simulations as the number of devices mounted an the device thermal pad size increases, all else being equal, under the four test conditions described in table 2. Standard deviation of fitted curve is shown each plot as σ.

	Test Condtion Number			
Heatsink Parameters	***1***	***2***	***3***	***4***
Convection Coeff. (W/m²K)	9	9	10	12
Convection Temperature (°C)	25	25	20	30
Emissivity	0.2	0.2	0.2	0.25
Radiation Temperature (°C)	210	210	200	180
Total Power Dissipated (W)	30	30	100	100
Length (mm)	150	150	600	500
Width (mm)	120	120	600	300
Depth (mm)	50	50	25	85
Number of Thermal Pads	4	1	12	6

Table. 2 A table of the parameters used in the analyses with results shown in figure 7.

Figure 7 shows the trends in peak heatsink temperature with respect to pad size for four different sets of thermal conditions. The conditions of these four cases are defined in table 2. The data points in figure 7 are accompanied by the line of best fit. The function describing the fit takes the same form as that shown in equation 1. Once again, *c* is made to be the negative of the average heatsink temperature, while *b* is set to -0.5 in this case, leaving just *a* to be found for each case.

Figure 7 shows that there are, once again, strong correlations between the data and the fits. While the correlations are not as strong as those in figure 5, they still have adjusted-r values >0.92 in all cases. Therefore, it can again be concluded that the simplified trend line, with only one variable to be derived from a single FEM model, can allow reliable predictions, in this case of the impact of pad size on peak heatsink temperature.

III. Analytical Method and Results

The two trends found previously explore the two key variations in the device-heatsink interface as a system uses a larger number of lower voltage rated devices, as would be the case in a multilevel converter of increasing order.

In order to evaluate real world thermal performance, a dataset of real world devices was compiled, along with a number of relevant thermal performance metrics extracted from manufacturer datasheets. The full list of the devices considered can be found in appendix A. All devices considered are rated to between thirty and fifty amps, in line with the reference converter specification. The key device parameters extracted from the datasheets of those listed in appendix A are: maximum drain-source voltage rating, maximum junction temperature, size of thermal contact area, thermal resistance from junction to thermal contact area, and whether the it has an electrically insulated thermal contact.

To evaluate junction temperature of a device under a given set of conditions is now possible. The number of levels in a converter determines whether a device is suitably rated, as a greater number of levels reducing voltage stresses on each device. The number of levels in the converter will give the number of thermal pads, and the compiled dataset will yield the pad size – this enables calculation of the peak heatsink temperature for the results of the single FE analysis conducted at any state. The junction temperature is then the sum of the peak heatsink temperature and the product of the power dissipated in each device and the thermal resistance to the heatsink. The thermal resistance from the junction to the case was extracted from the datasheet, a small thermal resistance of $0.3KW^{-1}$ for thermal grease, and the thermal resistance of an insulated medium (if required), in this case using a typical thermal resistivity of a Kapton insulator of $0.46WK^{-1}m^{-1}$.

Some of these devices are surface mount and are designed to sink their heat through the PCB that they are electrically bonded to. To calculate the junction temperature in this case, they will be considered as mounted to an aluminium backed PCB. These integrate an insulator, and can have a typical thermal resistivity of $1WK^{-1}m^{-1}$, according to a reference page from Epectec [11].

To explore the total impact of multilevel converters on thermal performance - given a specific heatsink, power dissipation and ambient temperature – FE is used to calculate the peak and average temperature for some number of pads of some size. From here, for every number of levels (and, by extension, number of devices), the junction temperature is calculated for every device of a sufficient voltage rating.

The results of this method for a given heatsink are shown in figures 8 and 9. The y-axis shows the 'junction temperature margin', which is the difference between the calculated junction temperature and its rated maximum, as found on the datasheet. Figure 8 shows the trend for a total power dissipation of 30W, while figure 9 shows the trend for a system with the same peak and average heatsink temperature but with a total dissipation of 200W. Results for PCB bonded heatsinking and conventional, external heatsinking are shown separately, as noted in the legend.

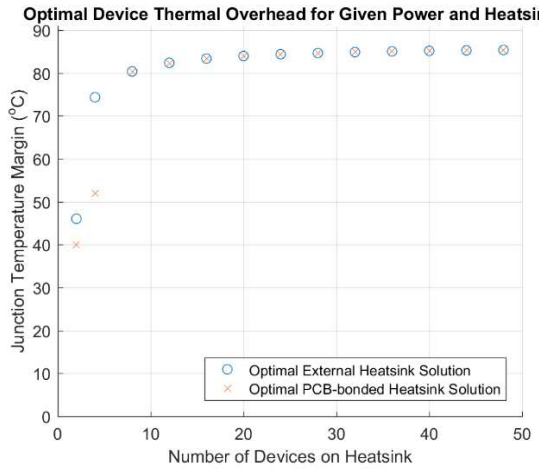

Fig. 8 Trend in junction temperature margin with an increasing number of devices for a total dissipation of 30W.

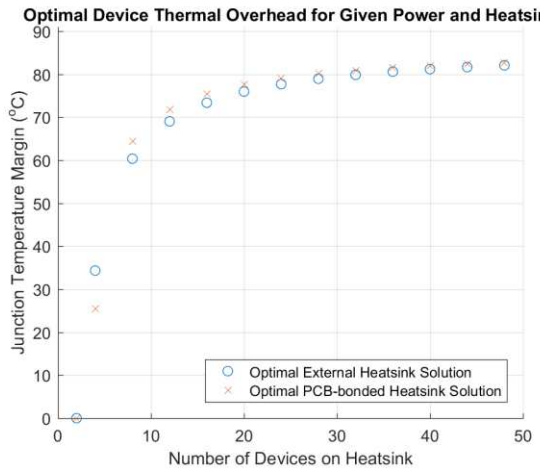

Fig. 9 Trend in junction temperature margin with an increasing number of devices for a total dissipation of 200W.

IV. Discussion

Figures 8 and 9 show that there are significant benefits to be gained from distributing a thermal load across a larger number of devices on a single heatsink. While in this case the results assume heatsink remains unchanged and the headroom simply improves, thereby improving reliability and mean time before failure - clearly this means that a smaller heatsink could be used or greater power dissipation could be tolerated instead.

Looking closer at the results, and specifically at which devices are optimal, it is also shown that the smaller thermal contact area of devices with a low voltage becomes much less of an issue with a larger number of devices, as the power being transferred over each thermal interface is much reduced.

Figure 8 seems to show that the benefits of increasing number of devices suffers from rapidly diminishing returns. Figure 9, however seems to show this less so. The root of the diminishing return is the fact that at high number of levels the power dissipated in each device is so small that there is little thermal benefit to be gained, and the performance of the junction to heatsink thermal interface in negligible. The fact that figure 9 continues to improve significantly at larger numbers of devices is due to the fact that the total power dissipation is higher, so the power through each device remains relatively high.

V. Conclusion

To conclude, an analytical method has been derived that permits the bulk analysis of the benefits of distributing a thermal load, as one might in a multilevel converter of increasing order, without bulk FE analyses. This can be of great utility in system optimisation and grants some quantitative, numerical justification for the use of multilevel converters over conventional counterparts. The key results of the analytical method are that there are significant thermal benefits to be gained through the distribution of a thermal load, but that at lower total power levels there is less reason to distribute over a very large number of devices.

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APPENDIX A

List of all silicon MOSFET devices used in main analysis:

Inf BSC076N06NS3G	Inf IPD053N06N	Fairchild FDD86540
Inf BSB165N15NZ3	Inf BSZ040N06LS5	Inf IPB65R045C7
Inf IPP65R045C7	ST STW62N65M5	Toshiba TK49N65W
ST STW56N65M2	ST STI57N65M5	Inf BSC320N20NS3
Fairchild FDP2710	IR IRFP4229	Vishay SUM45N25-58
Inf AUIRFP4409	Toshiba 2SK3176	ST STB40NF20
IXYS IXFT50N30Q3	Inf IPA075N15N3	IR IRFI4228
Inf BSC190N15NS3	Fairchild FDMS86255	Fairchild FDMS86200
Toshiba TK40A10N1	Vishay IRFP064PBF	Inf IRFI4410ZPBF
Toshiba TK46A08N1	Fairchild FDMC86340	Toshiba TK35A08N1
Toshiba TPCA8048-H	Inf IRFI1010N	Inf IPD30N06S2
Vishay SQD50N05-11	Inf AUIRFZ44N	Toshiba TK50P04M1
Toshiba TPCA8015-H	Vishay SQD50N04-4	Inf IPD50N04S4L-08
Toshiba TPCA8026	Fairchild FDMC8010	Inf IRFH5301TR2PBF
Vishay SIR862DP-T1	Fairchild FDMS3602S	Inf BSZ036NE2LS
Inf IPW65R045C7	IXYS MKE38RK600	Inf AUIRFZ46NL
ST STW56N60DM2	Fairchild FCH47N60N	Toshiba TPCA8045-H
Inf IPP320N20N3	IR IRFP260N	ONSemi NVTFS5811
Toshiba 2SK2995	Toshiba 2SK2967	Inf BSZ0904NSI
Inf IRFB4137	Fairchild FQA44N30	Inf IRFZ44NPBF
Inf BSB165N15NZ3G	Inf IPP200N15N3	Inf BSZ042N04NS
Inf BSC360N15NS3G	ST STF100N10F7	TI CSD17573Q5B
Toshiba TK34A10N1	Fairchild FDMS86103	Inf IRF6717MTR1
Renesas RJK0852DPB	Inf IPD30N08S2	Inf BSZ042N06NS
ST TF100N6F7		