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Towards Chirality-Encoded Domain Wall Logic

*K.A. Omari[1,2], T.J. Broomhall[1], R.W.S. Dawidek[1], D.A. Allwood[1], R.C. Bradley[1], J.M. Wood[1], P.W. Fry[3], M.C. Rosamond[4], E.H. Linfield[4], M.-Y. Im[5,6,7], P.J. Fischer[8,9], and T.J. Hayward[1]**

[1]*Department of Materials Science and Engineering, University of Sheffield, Sheffield, S1 3JD, UK*

[2]*Department of Physics, University of Nottingham, Nottingham, UK*

[3]*Nanoscience and Technology Centre, University of Sheffield, Sheffield, S3 7HQ, UK*

[4]*School of Electronic and Electrical Engineering, University of Leeds, LS2 9JT, UK*

[5]*Center for X-ray Optics, Lawrence Berkeley National Laboratory, CA, 94720, USA*

[6]*Daegu Gyeongbuk Institute of Science and Technology, Daegu 711-873, Republic of Korea*

[7]*School of Materials Science and Engineering, Ulsan National Institute of Science and Technology (UNIST), Ulsan 44919, Republic of Korea*

[8]*Materials Sciences Division, Lawrence Berkeley National Laboratory, CA, 94720, USA*

[9]*Department of Physics, University of California, Santa Cruz, CA, 94056, USA*

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*T.Hayward@sheffield.ac.uk

Non-volatile logic networks based on spintronic and nanomagnetic technologies have the potential to create high-speed, ultra-low power computational architectures. This article explores the feasibility of "chirality-encoded domain wall logic", a nanomagnetic logic architecture where data are encoded by the chiral structures of mobile domain walls in networks of ferromagnetic nanowires and processed by the chiral structures' interactions with geometric features of the networks. High resolution magnetic imaging is used to test two critical functionalities: the inversion of domain wall chirality at tailored artificial defect sites (logical NOT gates) and the chirality-selective output of domain walls from 2-in-1-out nanowire

junctions (common operation to AND/NAND/OR/NOR gates). The measurements demonstrate both operations can be performed to a good degree of fidelity even in the presence of complex magnetisation dynamics that would normally be expected to destroy chirality-encoded information. Together, these results represent a strong indication of the feasibility of devices where chiral magnetisation textures are used to directly carry, rather than merely delineate, data.

1. Introduction

As CMOS approaches the limits of its scaling potential there is substantial interest in exploring emerging devices that could either replace CMOS, or work alongside it in heterogeneous systems targeted at overcoming specific limitations of existing hardware.[1]

Nanomagnetic and spintronic devices are considered promising "Beyond-CMOS" technologies due to their fast operating speeds, non-volatile nature and well-developed routes to reading and writing data.[1] Motivated by this, there have been a variety of proposals to create spintronic logic networks, where the non-volatile nature of magnetically encoded data would allow memory and processing to occur in the same medium. Most prominent amongst these have been nanomagnetic logic/quantum cellular automata networks in which data are represented by the magnetisation states of individual, bistable magnetic islands.[2,3] These are placed in complex geometric arrangements such that dipolar interactions between elements implement logic operations and propagate data through the network. There have also been proposals to create logic networks from magnetic tunnel junctions (MTJ) of the type used in commercially available magnetic random access memory (MRAM) chips.[4] In these devices signals are propagated either by spin[5] or conventional electrical currents,[6] and logical operations performed by the switching of the MTJ's layer configurations.

In the devices described above, the magnetisation states of discrete magnetic elements are used to represent data, an approach broadly equivalent to that utilised for data storage in MRAM.

However, other proposed logic devices are more closely related to the approach of racetrack memory,[7–9] where data are encoded along the length of continuous magnetic nanowires. For example, in magnetic domain wall logic (DWL), data streams are encoded by the positions of domain walls (DWs) along soft ferromagnetic nanowires.[10] Rotating magnetic fields drive these domain wall sequences through a variety of junctions to realise logic operations on the data. Similarly, there have been propositions for nanowire-based logic schemes where trains of skyrmions are used to represent data.[11]

In conventional DWL domain walls essentially delineate data, rather than encode it directly. However, in many systems DWs also have an internal degree of freedom, chirality, that could also be used to encode data. The realisation of significant Dzyaloshinskii-Moriya interactions (DMI) in thin magnetic films has made chirality a key topic in contemporary nanomagnetism research.[12–14] For example, manipulating DMI in thin films with out-of-plane magnetisation allows DW chirality and structure to be uniquely defined, allowing efficient spin torque driven domain wall transport via the spin Hall effect,[13–15] although this obviously precludes devices where chirality is used as a data carrier. In a contrasting exploitation of chirality, we previously used micromagnetic simulations to demonstrate the feasibility of a logic architecture in which the chiralities (clockwise or anticlockwise circulation) of "vortex" type domain walls (VDWs) [16] were used to encode and process data,[17] A later publication by *Vandermeulen et. al.* also showed the feasibility of a similar architecture based on the chirality of transverse domain walls.[18]

Chirality-encoded architectures have an important advantage over conventional DWL: in conventional, field-driven DWL, data cannot be moved entirely coherently due to the half-field-cycle lag of the motion of head-to-head (H2T, 1-to-0 data transitions) and tail-to-tail (T2T, 0-to-1 data transitions) around the circuits. This makes useful circuit design architecturally challenging. In chirality-encoded logic, where data are carried by a continuous

alternating stream of H2H and T2T DWs this is no longer an issue. Chirality-encoded logic also encodes data within the structures of inherently digital magnetic textures with sizes dictated by fundamental length scales of magnetism, making such approaches highly scalable. However, challenges are presented by the fact that DW structures are typically unstable during propagation due to complex Walker breakdown dynamics,[19–21] effects that could lead to data loss.

In this paper, we use magnetic imaging experiments to indicate the feasibility of two of the critical operations of chirality-encoded logic architectures. Firstly, we demonstrate inversion of VDW chiralities at artificial defect sites; a Logical NOT operation in the proposed architecture. Secondly, we show that in 2-in-1-out nanowire junctions outputted VDW chiralities are controlled by the sequence in which the input nanowires switch. This is a common functionality required for the operation of AND/NAND/OR/NOR gates.[17] Our results are of particular significance as they have been performed in standard soft magnetic wires composed of $Ni_{80}Fe_{20}$ at fields above Walker breakdown. That these operations are still possible with good fidelity in the presence of complex magnetisation dynamics is a strong indication of the robustness of the approach.

2. Results and Discussion

2.1. NOT Gates

The basic geometry of a NOT gate in the chirality-encoded logic architecture is illustrated schematically in **Figure 1(a)**. The NOT gate consists of a deep, double notch, which is intended to invert the chirality of clockwise (CW) VDWs (binary 0) to anticlockwise (ACW) VDWs (binary 1) and vice versa as they are driven through it **(Figure 1(b))**.[17]

The operating principle of the NOT gates is illustrated using quasi-static (gilbert damping parameter, $\alpha = 0.5$) micromagnetic simulations in **Figure 2(a) & (b)**, which respectively show

ACW and CW VDWs being inverted as an applied field ramp was used to drive DWs through a pair of notches (width (w_n) and depth (d_n) = 135 nm) in a 50 nm thick, 400 nm wide nanowire. We note slight differences in the reversal mechanism and propagation fields for the two VDW chiralities; we attribute this to the ripple domain structure that formed around the notches, which was invariant when the chirality of the input VDW was flipped, and thus could break the symmetry of the system.

Our understanding of the NOT gates can be assisted by the topological charge model of DWs, as originally proposed by Tchernyshyov *et. al.*[22] Within this framework, a VDW is described as a combination of two -½ edge topological charges at the edges of the nanowire, and a single +1 charge at the centre of the vortex (**Figure 2**). The chirality of the VDW is controlled by the positioning of the -½ charges; For H2H VDWs, if the leading charge lies on the bottom (top) edge of the nanowire the VDW has ACW (CW) chirality. Using **Figure 2(a)** as an example, one can see that the leading -½ charge of the initial ACW VDW lay at the lower edge of the nanowire. As the DW was pushed through the notch, the nanowire on its left-hand side underwent a complex series of vortex and antivortex nucleation/annihilation events (that none-the-less retained zero net charge[22]), resulting in switching progressing further on the upper edge of the nanowire than the lower edge. This placed a new, leading -½ charge at the upper edge of the nanowire, such that the outputted VDW was CW. Thus, passing VDWs through the notches exchanged the positions of their -½ topological charges, inverting their chiralities.

To demonstrate this behaviour experimentally we fabricated the nanowire device shown in **Figure 3(a)**. The device consisted of a 400 nm wide, 50 nm thick $Ni_{80}Fe_{20}$ nanowire connected to a nucleation pad and contained a double notch ($w_n = d_n$ = 135 nm) at the nanowire's centre. A 2 μm wide Au/Ti current line was fabricated directly over the notch, transverse to the magnetic nanowire.

The behaviour of the device was characterised using Magnetic Transmission X-ray Microscopy (MTXM), which allowed their magnetisation configurations to be imaged in the presence of *in-situ* applied magnetic fields. The experiment proceeded by first saturating the device along the –x direction with an applied field of H = -1 kOe. A reversed applied field of H = 100 Oe was then used to nucleate VDWs from the pad and move them to the double notch. The Au/Ti current line prevented imaging of the nanowire beneath it. Thus, to determine the initial VDW chiralities we applied a -20 V amplitude, 5 ns duration pulse to the current line, producing a localised field ~-230 Oe along -x, while simultaneously applying a small global applied field of H = -15 Oe. Thus, the VDWs experienced a strong combined field (H ~ -245 Oe) when under the current line, but a much weaker field H = - 15 Oe (of the order of the pinning field of intrinsic nanowire defects) as they emerged from under it. The net effect of this was to push the VDWs out from under the current line and propagate them backwards until they became pinned at intrinsic defects in the nanowire, allowing their initial chirality to be imaged. Following measurement of the VDWs' initial chiralities, a field of H = 100 Oe was applied to push the VDWs back to the double notch. We then applied a 20 V pulse while applying a field H = 15 Oe. Together these pushed the VDWs through the double notch and caused them to pin just beyond the current line's edge, allowing their final chiralities to be determined. This relatively complex protocol was required so that we could place the VDWs in locations where they could be imaged, without causing them to interact with geometric features (e.g. corners, larger notches) that could induce additional modifications of their chiralities.[23–25]

Figure 3(b) presents typical MTXM results obtained from applying this protocol. In the upper image, taken after the first current pulse application (and referenced to negative saturation), a VDW was present before the current line, with its ACW chirality determinable from the asymmetry in contrast between the lower and upper edges of the nanowire. In the lower image,

taken after the VDW had been driven through the notches (and referenced to the upper image), a CW VDW was visible just beyond the current line, thus indicating the NOT gate was operating as expected. VDWs were propagated left-to-right across the notches in this way a total of 13 times, with only a single anomalous measurement showing VDW chirality to be preserved, rather than inverted.

Figure 3(c) presents a further series of MTXM images in which a VDW was repeatedly passed back and forth across the notches to alternate its chirality. Here, MTXM contrast was produced by referencing images prior to each passage, to those after each passage, such that the presented images show the changes in the nanowire's magnetisation configuration in each operation. The resulting images, which can be understood with the help of the schematic diagrams in the figure, clearly show repeated switching of the VDW chirality over four consecutive toggles. **Figure 3(d)** plots the toggling of the VDW chirality over a larger number of experiments; we observed a total of nine successful toggles before an event where chirality was preserved across the gate occurred. Our experimental results thus show the NOT operation to be successfully performed by a double notch.

The simulations previously presented in **Figure 2** show the operation of the NOT gates under a quasi-static approximation ($\alpha = 0.5$) and with a globally applied field. To more accurately simulate the nanowires dynamics we performed further simulations with a realistic value of damping ($\alpha = 0.02$), and with the field from the current line applied over a 2 μm window in the centre of the simulation. As our experimental setup did not allow direct determination of the profile of the pulse in the current line we performed simulations for a relatively large range of feasible field amplitudes (H_{line} = 140 - 290 Oe) and rise/fall times ($t_{rise/fall}$ = 0 - 2.5 ns). Details of how these values were selected can be found in this article's supporting information.

Figure 4(a) & (b) present dynamic simulation results for H_{line} = 230 Oe and $t_{rise/fall}$ = 1 ns. While the observed dynamics were much more complex than in the quasi-static simulations, the results agreed with those observed experimentally, with an ACW DW inverting to CW on moving left-to-right across the notches, and a CW VDW inverting to ACW on moving right-to-left. However, the complexity of the dynamics also appeared to affect the reliability of the process. For example, for the parameters described above, chirality inversion was not observed for an ACW VDW moving right-to-left across the notches. Furthermore, across the full range of simulation parameters studied (see supporting information), we observed a range of behaviours including chirality rectification (i.e. both input chiralities producing the same output), chirality transmission (neither chirality inverting) and the intended inversion process. This suggested that the dynamics of the system were highly sensitive. It was therefore surprising that we observed such robust chirality inversion in our experimental measurements. One possible explanation is that the edge roughness of the nanowires, which was not included in the simulations, helped suppress dynamic complexity, as has previously been suggested for the case of free-propagating DWs.[26]

2.2. 2-in-1-out junctions

The operating principles of 2-in-1-out junctions is illustrated in **Figure 1(c)**. The key property is that the chirality of the outputted VDW is controlled by the order in which the input wires switch; if the top wire switches first a CW VDW is outputted, while if the bottom wire switches first an ACW VDW is outputted. As we showed in our previous modelling study [17], this behaviour can be used to realise logic functions (AND/NAND/OR/NOR) if single notches, which exhibit chirality dependent pinning fields, are added to each of the two input wires (**Figure 1(a)**). The input notches allow the chirality of the inputted VDWs to determine the order in which the input nanowires switch, and thus the chirality of the outputted VDW. For example, to realise a NAND gate a larger notch would be placed in the upper edge of the upper

input nanowire, and a smaller notch in the lower edge of the lower input nanowire. Under these conditions, the top input would switch first, and output a CW VDW (0), only if both inputs contained ACW VDWS (1); for all other input chirality combinations, the bottom input would switch first, producing an ACW VDW (1) at output, thus realising the truth table of a NAND gate. Changing the locations of the two notches allows the junctions to realise AND/OR/NOR gates [17]. In the following we focus on a demonstration of the universal operation of the junctions themselves, i.e. the dependence of the outputted VDW chirality on the switching order of the input nanowires.

Figure 5(a) presents the results of quasi-static micromagnetic simulations of junctions in 40 nm thick, 400 nm wide nanowires. The input nanowires each made an angle of 15° with the output nanowire. As expected, the results showed that, independent of the chirality of the inputted VDW, the switching of the first input nanowire resulted in the formation of a transverse DW (TDW) spanning between the centre of the junction and the point where the input nanowire meets the output. The switching of the second input nanowire completes the switching of the junction, producing a VDW in the output nanowire. The chirality of the outputted VDW depended on the nanowire switching order as expected; if the top (bottom) nanowire switched first the outputted chirality was CW (ACW).

As for the NOT gates, the behaviour of 2-in-1-out junctions can be understood using the topological charge model of DW structure. **Figure 5(b) & (c)** show the switching process of the junction in detail. As previously, inputted VDWs consisted of a central +1 charge and two -½ edge charges. As the first VDW reached the junction (Figure 5(b)) the central +1 charge annihilated the upper -½ charge, leaving a +½ charge at the centre of the junction and a -½ charge at the point where the input nanowire met the output, thus creating a TDW. As the second VDW approached the junction (Figure 5(c)), a complex series of vortex

nucleation/annihilation events occurred where the moving charges of the VDW combined with the static -½ charge at the junction to create new +1 and -½ charges. These respectively formed the core and trailing -½ edge charge of a new VDW in the output wire. The leading -½ charge of the outputted VDW was that of the previously deposited TDW, and as this lay on the lower edge of the output nanowire, the outputted VDW had ACW chirality. Hence, the switching order of the input nanowires determined the positioning of the leading-edge charge in the outputted VDW, and thus its chirality.

To demonstrate this behaviour experimentally we fabricated nanowire devices of the design shown in **Figure 6(a)**. The devices consisted of 2-in-1-out junctions with nucleation pads attached to each of the input nanowires to act as sources of DWs. Double notches (w_n = 160 nm, d_n = 130 nm) were placed ~2 μm after the junction to pin the outputted VDWs and allow their chiralities to be observed. In some devices, a single notch was added into one of the input nanowires to try to modify the input nanowire switching sequence, although in practice the stochastic nature of DW pinning[24,27] meant these perturbed rather than strictly determined this. The nanowires' width, thickness and junction angle were as described for the simulations above.

Figure 6(b) presents the results of an example MTXM imaging experiment on the 2-in-1-out junctions. Here, both the junction and output notches were imaged while the applied field was ramped, such that both the switching order of the input nanowires, and the chiralities of the outputted VDWs could be observed. For example, in the results shown in **Figure 6(b)**, the bottom input switched first, forming the expected TDW across the end of the input nanowire. This was followed by switching of the top input, resulting in the propagation of an ACW VDW to the output notches.

Figure 6(c) presents further data showing all four of the possible input switching/output chirality combinations, as observed from a single device with no notches in its input nanowires. As expected, these results did not manifest with equal probability: Across 18 total measurements we observed ten occurrences where the top input switched first; these favoured CW over ACW output by a factor 8:2. In the remaining eight events, where bottom input switched first, ACW output was favoured by a factor 7:1. Thus, the device strongly favoured the behaviours predicted by the quasi-static simulations. To confirm this was a property of the junctions we performed a total of 67 measurements across six different devices. The results of these measurements are summarised in **Figure 6(d)**, and clearly show the strong correlation between input switching order and output chirality. Full details of the results from each device measured can be found in this article's supporting information.

To gain understanding of the minority of events where the output VDW chirality was not correlated to the input nanowire switching order we performed dynamic simulations of the junctions' behaviours. **Figure 7(a)** presents example results for the switching of the first (in this case lower) input nanowire via the propagation of a CW VDW at H = 105 Oe. This field was lower than those in the experimental measurements, as with higher fields the DWs propagated straight through the junction without stopping. We suggest that nanowire edge roughness assisted pinning in the experimental measurements, and note that the applied field in the simulation was still substantially above the Walker breakdown field (~20 Oe in the measured/simulated nanowires).[27] The DWs behaved as observed in the experiments and quasi-static simulations, forming a TDW across the junction between the input and output nanowires. Equivalent behaviour was observed for all permutations of which input switched first and input VDW chirality.

More complex behaviour was observed during switching of the second input nanowire. **Figure 7(b) & (c)** contrast the dynamics observed for the switching of the second (top) input at two applied fields, H = 105 and 95 Oe. The Walker breakdown dynamics of the two simulations were broadly similar during the switching of the top input wire, but diverge substantially as the DWs reached the output nanowire; while the simulation for H = 105 Oe formed the expected ACW VDW, that at H = 95 Oe formed a CW VDW. The results of further simulations performed for fields in the range H = 85 - 110 Oe are summarised in this article's supporting information. Each of these showed similar results, such that for a given field some combinations of input nanowire and chirality would produce the expected output, while others would not. We note that the field amplitude here was primarily used as a handle with which to explore variations in the Walker breakdown dynamics. In real devices similar variations in dynamics would be produced by thermal perturbations, even for a single well defined applied field.[28]

The results above indicate that complex Walker breakdown dynamics can cause the operation of 2-in-1-out junctions to break down. However, much like for the NOT gates, the experimental devices were more reliable than would be anticipated from the complex, dynamical simulations. We again suggest that edge roughness may play a role in simplifying DW dynamics[26] such that they replicate the functionality observed in quasi-static simulations to a reasonable level.

3. Conclusions

In this paper, we have used magnetic imaging and micromagnetic simulations to indicate the feasibility of two functions critical to the operation of chirality-encoded domain wall logic: the inversion of VDW chirality by artificial defect sites (NOT gate) and the control of output VDW chirality in 2-in-1-out junctions (essential for AND/NAND/OR/NOR gates).

Our experimental results were found to reproduce the basic functionalities observed in quasi-static simulations, with a modest number (<20 %) of anomalous events. We attribute these to complex Walker-breakdown dynamics, which are capable of flipping the chirality of VDWs.[19–21,28] Interestingly, the results of our experiments lay closer to those expected from the quasi-static simulations, than from true dynamical simulations, perhaps suggesting that nanowire edge roughness had an inhibiting effect on the complexity of DW dynamics [26]. However, that the required functionalities could be observed with a good degree of reliability even in systems with low damping is an excellent indicator of the feasibility of chirality-encoded logic schemes. Despite these successes, fully reliable behaviour would be required to create a digital logic device. Further improvements could be achieved by manipulation of the nanowires' damping constants to simplify DW dynamics, e.g. by doping with rare-earth materials such as Ho or Tb [29–31]. As we have shown in a previous paper,[32] this would also allow for deterministic pinning at artificial defect sites, which is the final function required to fully realise AND/NAND/OR/NOR gates. It may also be interesting to investigate whether chirality-encoded approaches could be applied to neuromorphic computing, where tolerance to stochastic behaviour is higher.[33]

Further work will certainly be required to realise full chirality-encoded logic circuits. However, our work provides a promising foundation for experimental investigations into the remaining elements required to create these (e.g. FAN-OUT, cross-over elements). Methods of inputting and outputting data will also need to be developed. We note that the functionality of 2-in-1-out junctions already offers a clear route to writing chirality-encoded data, for example by using patterned current lines to selectively address input wires, thus dictating the chiralities of VDWs emerging from the junctions. Furthermore, an inversion of this structure (1-in-2-out) has already been shown to be an excellent detector of chirality, with VDWs selectively switching one of the two output wires depending on their chirality.[34] Magnetoresistive monitoring of the

output wires of such a junction would therefore offer a sensitive readout mechanism. Another important question is whether chirality-based logic can be realised in materials systems where DWs can be driven efficiently by spin-torque. This is an interesting challenge, as in the current state of the art, where DWs are driven by the spin Hall effect, DW chirality is no longer a degree of freedom.[13,14,35] Nevertheless, our results represent a substantial step towards realising logic networks where information is carried, rather than merely delineated, by magnetic domain walls.

4. Experimental Section

4.1. Sample Fabrication

$Ni_{80}Fe_{20}$ magnetic nanowire devices were fabricated on x-ray-transparent silicon nitride membranes by electron-beam lithography, thermal evaporation and lift-off processing. 2-in-1-out devices were 40 nm thick, while NOT gate devices were grown to an increased thickness of 50 nm to enhance magnetic contrast. Vector network analyser ferromagnetic resonance (VNA-FMR) measurements of equivalent continuous films provided values of saturation magnetisation, M_s = 715 kA/m, Gilbert damping constant, α = 0.02, respectively higher and lower than would be expected for stoichiometric $Ni_{80}Fe_{20}$, suggesting our films were slightly nickel rich. The film's anisotropy field H_k was found to be negligible. Where required, additional Ti(5 nm)/Au(150 nm) current lines were added via a second lithography, evaporation and lift off step.

4.2. Magnetic Imaging

Magnetic Transmission X-ray Microscopy (MTXM) imaging of the nanowire devices was performed at beamline 6.1.2 of the Advanced Light Source (ALS).[36] In all cases, MTXM contrast was produced via dividing a reference image, m_1, by the image of interest, m_2, such that the presented images show the change in the magnetisation configuration $\Delta m = m_1/m_2$. In-

plane magnetic fields with amplitudes of up to 1 kOe were applied using an in-situ electromagnet. Where current pulses were required these were provided by an Avtech AVM-4 pulse generator with a maximum pulse length of 5 ns.

4.3. Micromagnetic Simulations

Micromagnetic simulations were performed with the mumax[3] simulation package. Material parameters were taken from the VNA-FMR measurements described above, aside from the exchange stiffness, which was assigned a standard value of A_{ex} = 13 pJ/m. For quasi-static simulations the Gilbert damping constant was set to an artificially high value, $\alpha = 0.5$, while for dynamic simulations it was given the measured value of $\alpha = 0.02$. In simulations of NOT gates, we used cell sizes of 4 x 4 x 5 nm^3, while for the larger-scale (and more computationally demanding) 2-in-1-out junctions we used cell sizes of either 4 x 4 x 40 nm^3 (quasi-static simulations) or 4 x 4 x 10 nm^3 (dynamic simulations). All cell sizes used for dynamic simulations were found to show phenomenologically similar Walker Breakdown dynamics to those for a 2.5 x 2.5 x 2.5 nm^3 (i.e. fully sub-exchange length) mesh.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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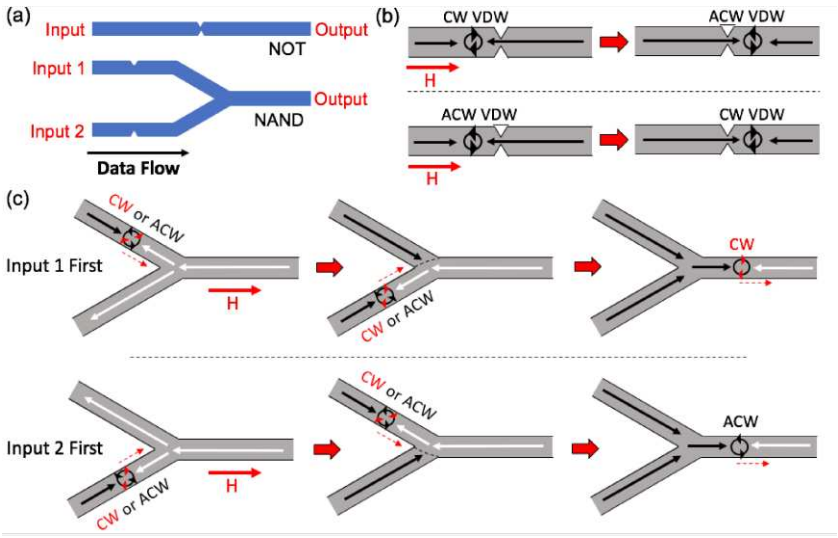


Figure 1: (a) Schematic diagrams illustrating the geometry of NOT and NAND gates in chirality-encoded domain wall logic schemes. (b) Illustration of the operating principle of the NOT gates; as the domain walls pass through the double notch their chiralities are inverted. (c) Illustration of the operating principle of the 2-in-1-out junctions in AND/NAND/OR/NOT gates; the chirality of the domain wall in the output wire is determined by the switching order of the input nanowires.

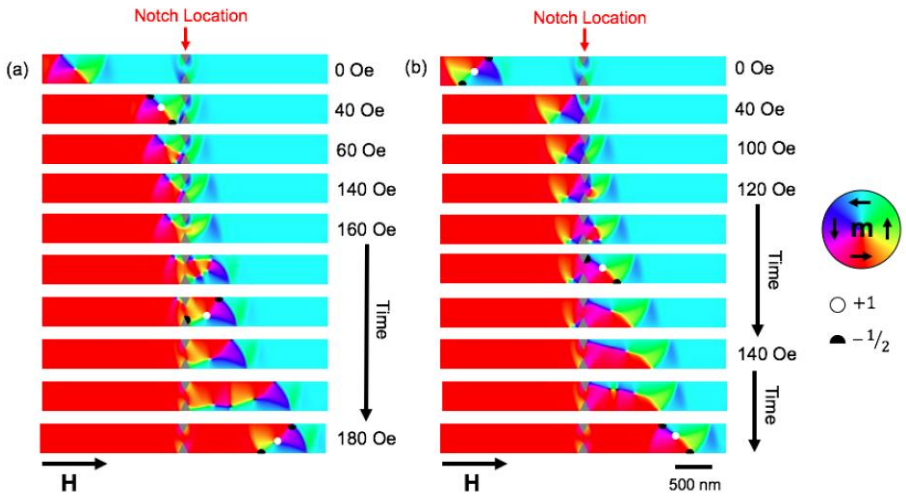


Figure 2: Quasistatic micromagnetic simulations showing the operation of a NOT gate in a 400 nm wide, 50 nm thick nanowire. $w_n = d_n = 135$ nm. (a) an initial ACW VDW is inverted to a CW VDW (b) an initial CW VDW is inverted to a ACW VDW. In some images symbols are used to represent the locations of topological charges in accordance with the key on the right of the figure.

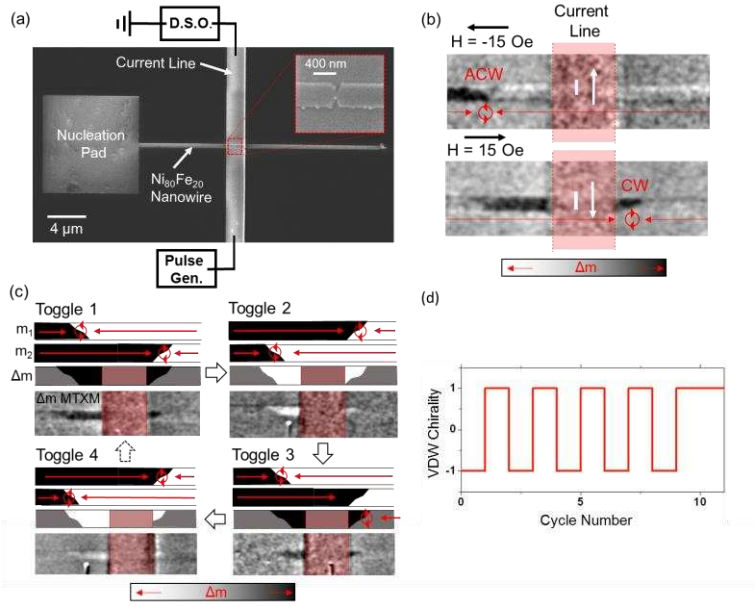


Figure 3: (a) SEM image of the NOT gate device. The inset figure shows an expanded image of the notched region (viewed through the gold current line). (b) MTXM images showing an ACW VDW being inverted to CW chirality on being passed through the double notches. The shaded red region represents the location of the current line, which obscures magnetic contrast. (c) Series of four MTXM images illustrating the toggling of a VDWs chirality as it was passed back and forth across the double notches. Contrast here was created by dividing the initial image (m_1) by the final image (m_2) resulting in an image of $\Delta m = (m_1/m_2)$. Schematic diagrams are provided above the MTXM images to assist the reader's interpretation of the contrast. (d) Plot showing how the chirality (CW = 1, ACW = -1) of a VDW varied for 10 passages back and forth across the notches.

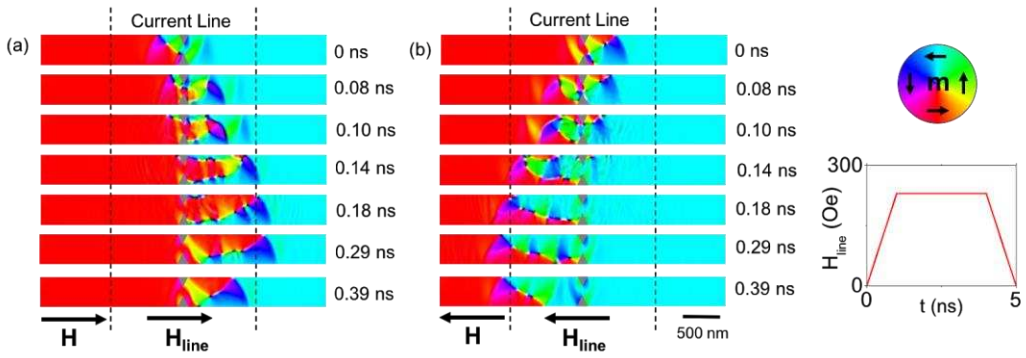


Figure 4: Dynamic micromagnetic simulations of VDWs passing through a NOT gate in a 400 nm wide, 50 nm thick nanowire. $w_n = d_n = 135$ nm (a) ACW VDW passes left-to-right through notches. (b) CW VDW passes right-to-left through the notches. The simulated field from the current line was localised between the two dashed lines and had the profile shown in the plot on the right of the figure ($H_{line} = \pm 230$ Oe and $t_{rise/fall} = 1$ ns). A uniform field of $H = \pm 15$ Oe was also applied to emulate the externally applied field in the experimental measurements.

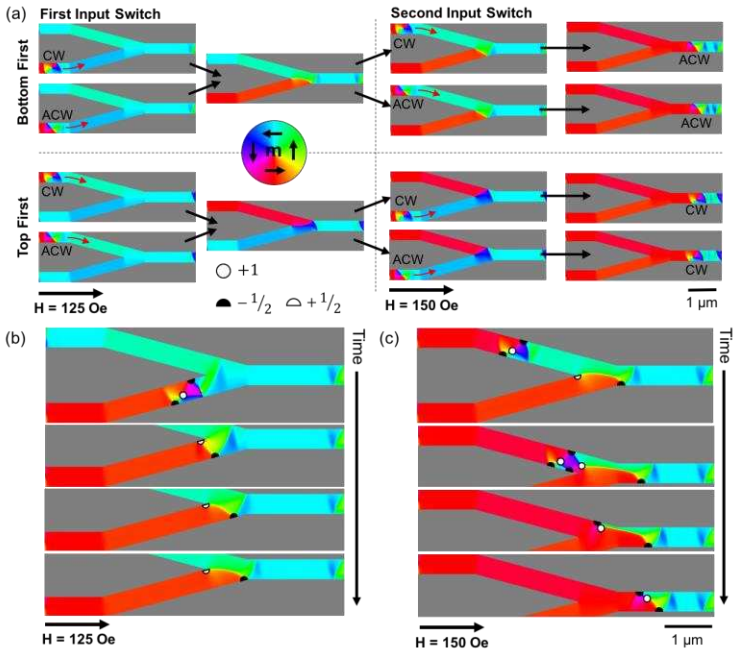


Figure 5: (a) Results of quasi-static micromagnetic simulations showing the various switching paths available for a 2-in-1-out junction. The input and output nanowires all had widths of 400 nm and thicknesses of 40 nm. (b) Detailed images showing the interaction of a CW VDW with the junction during the switching of the first (bottom) input nanowire. (c) Images showing the interaction of a CW VDW with the junction during the switching of the second (top) nanowire. In (b) & (c) the locations of topological charges are indicated with symbols in accordance with the key in the centre of the figure.

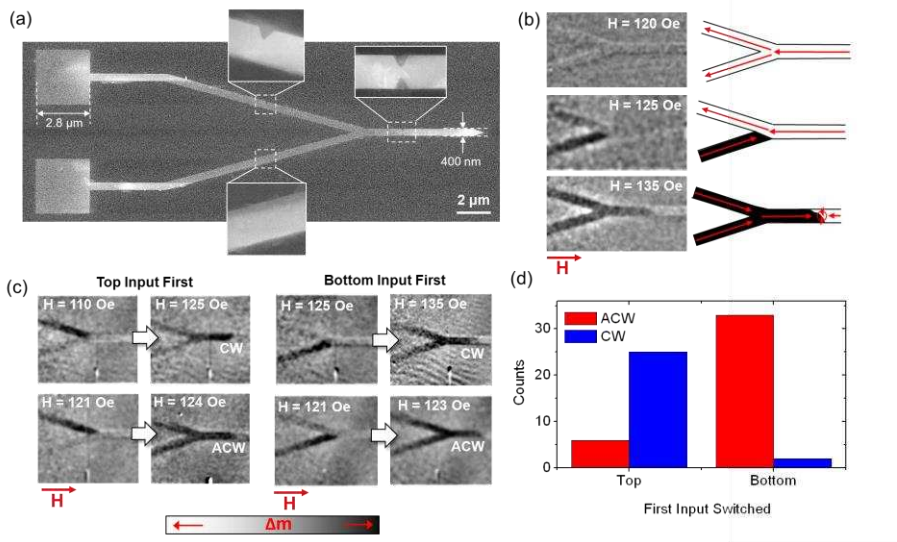


Figure 6: (a) SEM images showing one of the 2-in-1-out junctions measured in this study. The inset figures show the notched regions of the nanowires in detail. For the device shown only the top of the two input nanowires contained a notch. (b) Example MTXM images showing the switching of a 2-in-1-out junction as the applied field was ramped. In this case the bottom input switched first, followed by the top input, resulting in an ACW VDW at the output notches. (c) MTXM images illustrating the four possible switching paths for the 2-in-1-out junctions, as observed in a single device. In all cases the presented MTXM images have been referenced to images taken after saturation with a negative applied field. (d) Distribution of switching paths observed over a total of 67 measurements across 7 different devices.

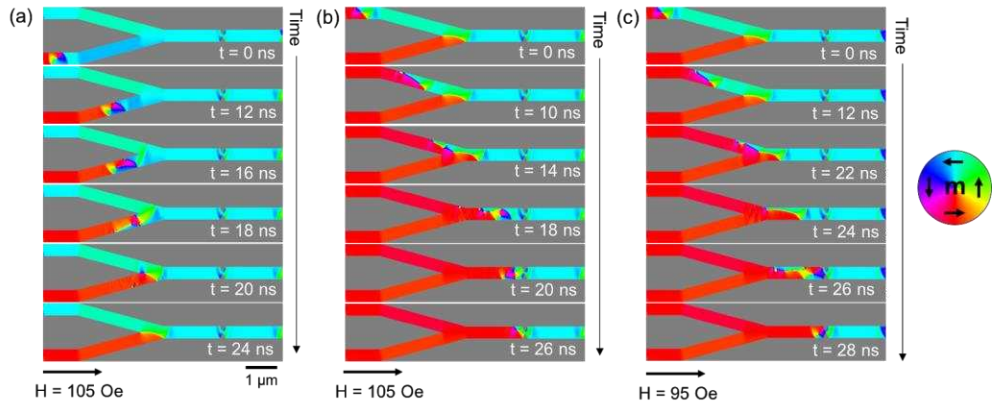
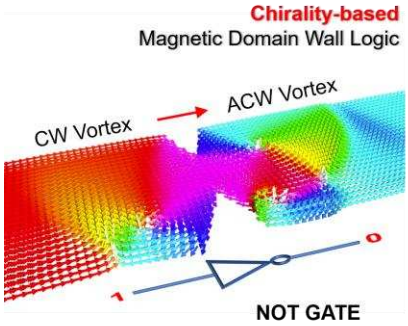


Figure 7: Dynamic micromagnetic simulations of the switching of 2-in-1-out junctions. The input and output nanowires all had widths of 400 nm and thicknesses of 40 nm. (a) Switching of the first (bottom) input by a CW VDW at H = 105 Oe. (b) Switching of the second (top) input by an ACW VDW at H = 105 Oe. (c) Switching of the second (top) input by an ACW VDW at H = 95 Oe.

Table of Contents Entry:

Keyword: Magnetic Materials

Towards Chirality-Encoded Domain Wall Logic

K.A. Omari, T.J. Broomhall, R.W.S. Dawidek, D.A. Allwood, R.C. Bradley, J.M. Wood, P.W. Fry, M.C. Rosamond, E.H. Linfield, M.-Y. Im, P.J. Fischer, and T.J. Hayward

Magnetic logic devices where data are encoded within the winding of chiral domain walls are proposed. High-resolution magnetic imaging techniques are used to show the feasibility of NOT, AND, NAND, OR and NOR gates. The work lays the ground for new forms of magnetic devices where domain walls are used to carry, rather than merely delineate information.