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Everard, Jeremy Kenneth Arthur orcid.org/0000-0003-1887-3291, Burtichelov, Tsvetan Krasimirov and Ng, Keng (2019) Ultralow Phase Noise 10-MHz Crystal Oscillators. IEEE Transaction of Ultrasonics Ferroelectrics and Frequency Control. pp. 181-191. ISSN 0885-3010

https://doi.org/10.1109/TUFFC.2018.2881456

Ultralow Phase Noise 10-MHz Crystal Oscillators

Jeremy Everard, Tsvetan Burtichelov, and Keng Ng

***Abstract*— This paper describes the design and implementation of low phase noise 10-MHz crystal oscillators [using stress compensated (SC) cut crystal resonators] which are being used as a part of the chain of a local oscillator for use in compact atomic clocks. The design considerations and phase noise measurements are presented. The design includes a low-noise transformer coupled differential amplifier, spurious resonance rejection filter, and electronically tuned phase shifter. Phase noise measurements demonstrate a performance of −122 dBc to −123 dBc/Hz at 1-Hz offsets and −148 dBc/Hz at 10-Hz offsets. The phase noise at 1-Hz offset is very similar to the phase noise produced by the low-noise version of a doubled 5-MHz BVA resonator-based oscillators (model number 8607) previously produced by Oscilloquartz. The noise floor of the oscillators presented in this paper is around −161 dBc/Hz. These designs can be used as the reference oscillator to control the timing of many modern electronics systems.**

***Index Terms*— Frequency control, low noise crystal oscillators, low noise oscillators, noise, oscillators, phase noise.**

I. Introduction

THE phase noise and jitter in oscillators set the ultimate performance limits in communications, navigation, radar, and precision measurement and control systems. It is, therefore, important to develop simple, accurate linear theories which highlight the underlying operating principles and to present circuit implementations based on these theories.

Crystal oscillators offer a solution for precision oscillators due to the precise resonant frequency, very high Q, and controllable temperature coefficients.

Many papers have been written on high frequency, very high frequency, and ultra-high frequency bulk crystal and surface acoustic wave oscillators [1]–[10] including a significant tutorial review of crystal oscillators [11].

Key aspects to be considered to achieve low phase noise in crystal oscillators are the $1/f$ flicker noise of the amplifier, the flicker-of-frequency noise in the resonator [1], and the amplitude modulation to phase modulation (AM-to-PM) conversion at higher crystal drive power levels due to nonlinear effects in the crystal [2], [3], [5]. There is transposition of this flicker noise onto the carrier which typically produces a $\sim 1/f^3$ phase noise contribution in the oscillator.

Methods to reduce the drive-level dependence include, for example, cancelation of two opposing effects by operating a quartz crystal oscillator at a point slightly above the crystal series resonance where a change in oscillator phase would result in a change in crystal drive level. This produces a shift in crystal frequency exactly equal to but opposite to the frequency shift resulting from the resonator phase versus frequency characteristic [2]. Another method to reduce drive dependence uses multiple resonators to share the power [4].

The far from carrier noise floor is reduced by increasing the crystal power so this should be considered at the same time as the drive-level dependence of the crystal [3].

The effect of resonator out-of-band impedance on the sustaining stage white noise should be considered [6]. Multiple amplifiers with inter-amplifier attenuation can also be used to improve performance [7].

A variety of self-limiting amplifier/oscillator types are discussed in detail in [3], which highlight the requirement for high Q and adequate suppression of $1/f$ flicker-of-phase-type noise, and improvement in oscillator noise floor signal to noise. A number of oscillator topologies are also discussed including the Pierce, Miller, Butler, and bridged-T configurations. Measurements of the AM-to-PM conversion are also important [9].

However, there are very few papers (if any) showing complete designs with phase noise near or below −120 dBc/Hz at 1 Hz offset in 10-MHz crystal oscillators. Ultralow-phase noise oscillators using Boîtier à Vieillissement Amélioré (BVA) [12] stress compensated (SC) cut resonators have been described [13], [14] but the detailed oscillator circuit descriptions were not included.

The quoted phase noise for the low-noise version of the BVA oven-controlled crystal oscillator (OCXO) 8607 oscillators in previous data sheets at 1-Hz offset is −130 dBc at 5 MHz and −122 dBc/Hz at 10 MHz. The phase noises of the oscillators described in this paper, which use standard SC cut resonators, are very similar to the doubled 5-MHz output (+6 dB) and directly to the 10-MHz output.

A number of low phase noise commercial designs are available, along with their phase noise specifications; however, circuit diagrams are not provided. For example, the preliminary data sheet for the Morion MV3336M specifies −119 to −120 dBc at 1-Hz offset so the oscillator presented in this paper is 2.5–3.5 dB better than the specification. The "extraordinary range" of low phase noise 10-MHz OCXOs manufactured by NEL states −120 dBc at 1-Hz offset.

The short and medium-term phase noise and Allan deviation of the local oscillator are limiting factors of the performance of

Manuscript received August 6, 2018; accepted November 8, 2018. Date of publication November 19, 2018; date of current version January 14, 2019. This work was supported by EPSRC under Project EP/J500598/1 and Project EP/L505122/1, in part by Leonardo MW, Ltd. (formerly Selex ES Ltd.), in part by BAE Systems, and in part by HCD Research, Ltd. *(Corresponding author: Jeremy Everard.)*

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Digital Object Identifier 10.1109/TUFFC.2018.2881456

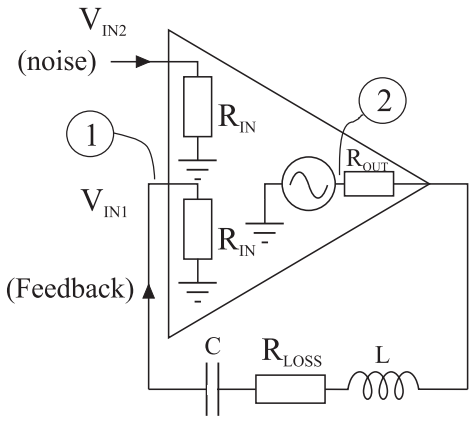

Fig. 1. Oscillator model.

most systems including, for example, vapor cell atomic clocks. Extremely low phase noise can be achieved by combining the close to the carrier performance of crystal oscillators with the medium offset and the low noise floor of a dielectric resonator oscillator (DRO) [15] and also including narrowband digitally controlled direct digital synthesizers [16]–[18].

It is interesting to note that the DRO described in [15] and [16] had similar or better phase noise performance than multiplied 100-MHz crystal oscillators, but the 10-MHz oscillator was able to improve the performance and stability below 10-Hz offsets. The resulting system [16] is highly versatile in terms of tuning and locking the flywheel frequency to the atomic resonance and is capable of providing multiple highly stable output signals at both RF and microwave frequencies.

In this paper, which is a significant extension of a paper submitted to the joint EFTF–IFCS 2007 Conference [19] and the 2017 IFCS Conference [16], we present the detailed design information for all the elements required for an ultralow phase noise 10-MHz crystal oscillator.

This paper is organized as follows. Section II describes the underlying phase noise theories and resultant optimum conditions. Section III describes the oscillator design with Section III-A covering the amplifier design, Section III-B the resonator modeling, Section III-C the spurious rejection filter, and Section III-D the electronic phase shifter tuning. Section III-E describes the complete oscillator circuit. Section IV covers the phase noise measurements, and Section V describes the implementation of a double-oven OCXO version. Section VI describes further work and potential improvements, and Section VII provides the conclusion.

II. Phase Noise Theory

It is important to develop a simple model to calculate and predict the noise performance of an oscillator. Leeson [20] demonstrated an equation which gives useful information about the phase noise but the optimum conditions for minimum noise are not clear. Parker [21] demonstrated an optimum condition for a modified version of Leeson's equation. It is useful, however, to develop a simple model, from first principles, which enables an accurate and clearly understood equation to be derived.

A suitable model is shown in Fig. 1 [22]–[25]. This consists of an amplifier with two inputs which are added together. These represent the same input but are separated to enable one to be used to model the noise input and the other for feedback. The resonator is represented as an LCR circuit where any impedance transformation is achieved by varying the component values. This circuit, through positive feedback, operates as a Q multiplication filter. It also contains the additional constraint that the AM noise is suppressed in the limiting process. This means that the phase noise component of the input noise drops to $kT/2$ which has been confirmed by NIST [26] and this research group. This limiting also causes the upper and lower sidebands to become coherent and has been defined as conformability by Robins [27]. The model is put in this form to highlight all the effects, which are often not clear in a block diagram model.

A general equation for the phase noise can be derived as shown in [24] and [25] which incorporate a number of operating conditions including multiple definitions of output power from the amplifier, the input and output impedances, the ratio of loaded to unloaded Q factor (Q_L/Q_0), and operating noise figure F.

The specific phase noise equation, where $R_{OUT} = R_{IN}$ and power is defined as the power available at the output of the amplifier (P_{AVO}), simplifies to the following equation:

$$L(f) = \frac{FkT}{8Q_0^2\left(\frac{Q_L}{Q_0}\right)^2\left(1-\frac{Q_L}{Q_0}\right)^2 P_{AVO}}\left(\frac{f_0}{\Delta f}\right)^2. \quad (1)$$

Equation (1) will be used in the analysis for the noise performance and gain requirements in the thermal noise regime and is minimum when $Q_L/Q_0 = 1/2$ and, hence, the insertion loss of the resonator is 0.25 (−6 dB) [24].

This minimum occurs when maximum power is dissipated in the resonator. This is described in detail in [25], where it is shown that the equation for power available to the resonator is very similar to the denominator of the phase noise equation. Everard *et al.* [25] also show how a similar phase noise derivation can be applied to the negative resistance oscillators and compare the noise performance of the two types.

As $S_{21} = (1 - Q_L/Q_0)$, a plot of phase noise versus insertion loss for the resonator (which is the same as the closed-loop gain of the amplifier) is shown in Fig. 2. It can be seen that less than 1 dB of phase noise degradation occurs when the insertion loss is within the bounds of 3.5–9.5 dB.

It should be noted that the optima, just discussed, apply if the noise is thermal (additive) noise and also only apply to the skirts of the phase noise. For far out noise to be minimum, the gain should be kept low (Q_L/Q_0 low), and for reduced transposed flicker noise, the loaded Q should be higher. However, it is a good starting point.

The more complete equation used to calculate the phase noise, used in the simulations and measurements shown in Section IV, is shown in (2) at the bottom of the next page [19]. The right-hand term (D) is based on (1) where F_1 is the noise figure of the oscillation sustaining amplifier.

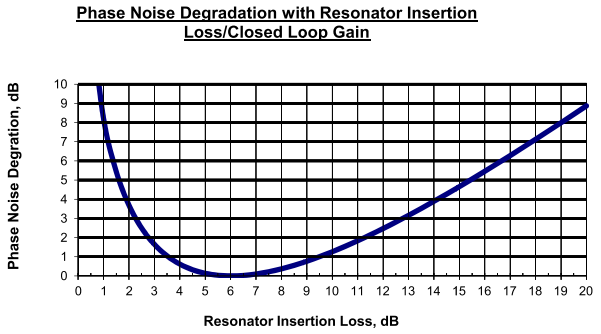

Fig. 2. Phase noise degradation with resonator insertion loss/open-loop gain.

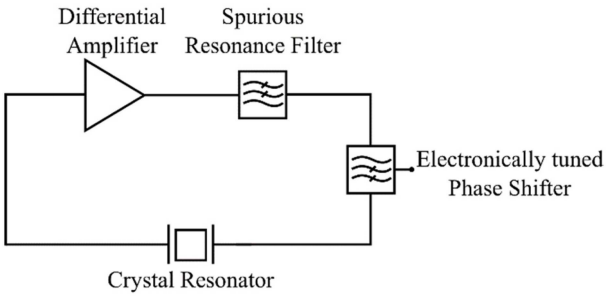

Fig. 3. 10-MHz crystal oscillator block diagram.

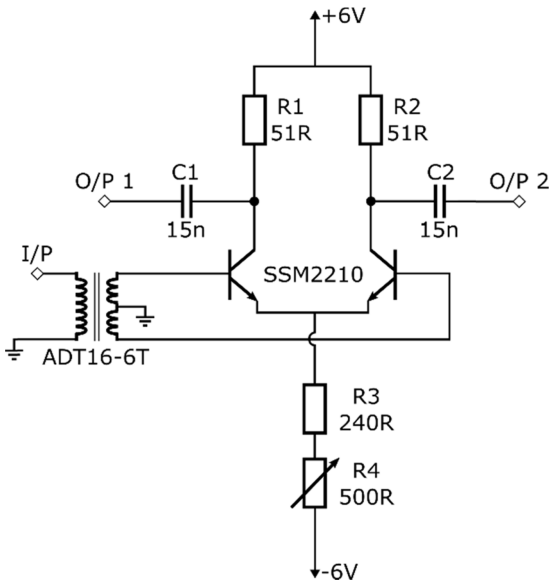

Fig. 4. Differential amplifier circuit diagram.

The middle term (C) shows the noise floor outside the resonator bandwidth (far from carrier noise) caused by the closed-loop amplifier gain. Both these terms are multiplied by a flicker noise component (B) $(1 + F_C/f)$, where F_C is the flicker noise corner. The left-hand term (A) includes the buffer amplifier after the output coupler and is still assumed to be limited to the phase noise component (therefore $2P$). F_2 is the noise figure of the buffer amplifier. C_0 is the coupling coefficient which relates the power available to the resonator to the power available to the buffer amplifier which is 1 in this case. The "1" just after the "log" refers to the phase noise of a single oscillator. This is changed to 2 when the combined noise of two identical oscillators is being displayed.

III. Oscillator Design

The block diagram of the feedback low phase noise 10-MHz crystal oscillator is shown in Fig. 3. It comprises a differential amplifier, a spurious resonance rejection filter, a voltage-tuned phase shifter, and the crystal resonator. Details on the design of each of these elements and their circuit diagrams are described in this section.

A. Differential Amplifier

The circuit diagram of the differential amplifier is shown in Fig. 4. The amplifier uses a low-noise supermatched n-p-n transistor pair (SSM2210 or SSM2212) to ensure good symmetry and low-noise performance. This particular device also has a very low flicker noise corner (<10 Hz), which is important for achieving low close to the carrier phase noise. The flicker noises of both n-p-n and p-n-p supermatched pairs are discussed by Rubiola and Lardet-Vieudrin [28] for dc/LF amplifier design.

An advantage of using a differential amplifier is that two outputs can be obtained simultaneously with a phase difference of 180°. One of these outputs can be used to close the loop (preferably the one with phase shift closer to N× 360°), while the other can be used directly as the output of the oscillator. This eliminates the need for an output coupler.

The differential design also offers nonsaturated limiting and accurate control of the limiting output power and near zero second-order (and even order) nonlinearities.

The amplifier is differentially driven using a 1:16 impedance transformer. This provides biasing for the bases of both transistors (connecting them directly together at dc and LF), while the impedance ratio ensures the optimal noise matching. For collector currents around 6.5–7.5 mA, used in these oscillators, the equivalent noise voltage is around 0.8 nV/$\sqrt{\text{Hz}}$, and the equivalent noise current is about 2 pA/$\sqrt{\text{Hz}}$; therefore, the optimum source impedance is about 400 Ω for a single device and thereby 800 Ω in the differential mode. This is 16× the source resistance of 50 Ω.

$$L(f) = 10\text{Log}\left[1\left[\underset{\text{A}}{\frac{F_2kT}{C_0 2P}} + \underset{\text{B}}{\left(1 + \frac{Fc}{f}\right)}\left(\underset{\text{C}}{\frac{F_1kT}{2P}\left(\frac{1}{\left[1 - \frac{Q_L}{Q_0}\right]^2}\right)} + \underset{\text{D}}{\frac{F_1kT}{8(Q_0)^2\left(\frac{Q_L}{Q_0}\right)^2\left(1 - \frac{Q_L}{Q_0}\right)^2 P}\left(\frac{f_0}{f}\right)^2}\right)\right]\right] \quad (2)$$

The minimum noise figure available for these noise sources is given in the following equation [24]:

$$\mathrm{NF}_{\min} = 10\log\left(1 + \frac{e_n \times i_n}{2kTB}\right) = 0.8 \text{ dB}. \tag{3}$$

The noise figure was measured to be 1.8 dB, and the difference is most likely due to the losses in the transformer.

Resistors $R1$ and $R2$ ensure that the output impedance is about 50 Ω for both outputs. Resistors $R3$ and $R4$ set the current through the transistors at about 6.5–7.5 mA. Capacitors $C1$ and $C2$ are used for coupling the RF signal to the outputs.

The bias current is set by resistor $R3$ and potentiometer $R4$ which also sets the gain and P_{AVO} at the output of the amplifier. The gain should be larger than the losses around the loop to ensure the oscillation under all conditions including the high turnover temperature, and the power should be correct for the best operation of the crystal. The power should be low enough not to cause damage, AM–PM conversion, or excessive aging but large enough to maintain low phase noise and low phase noise floor.

A simple calculation for the limiting output power can be obtained by assuming that the dc voltage across the output resistors ($R1$ and $R2$) under quiescent collector current conditions for a single transistor (I_{CQ}) is

$$V_{\mathrm{dc}} = I_{\mathrm{CQ}} \times R_{\mathrm{L}}. \tag{4}$$

The peak-to-peak voltage swing in $R1$ and $R2$ in terms of the collector currents is twice this

$$V_{\mathrm{p-p}} = 2 \times I_{\mathrm{CQ}} \times R_{\mathrm{L}}. \tag{5}$$

The peak voltage is half this value. As these limiters only saturate very lightly, they produce an output which is very nearly sinusoidal (not a square wave) so the rms value is, therefore,

$$V_{\mathrm{rms}} = \frac{I_{\mathrm{CQ}} \times R_{\mathrm{L}}}{\sqrt{2}}. \tag{6}$$

This is the equivalent open-circuit voltage so the power available into a 50-Ω load is

$$P_{\mathrm{AVO}} = \frac{V_{\mathrm{rms}}^2}{4 \times R_{\mathrm{L}}} = \frac{I_{\mathrm{CQ}}^2 \times R_{\mathrm{L}}}{8}. \tag{7}$$

The quiescent current in terms of the power available at the output is, therefore,

$$I_{\mathrm{CQ}} = \sqrt{\frac{8 \times P_{\mathrm{AVO}}}{R_{\mathrm{L}}}}. \tag{8}$$

For an available output power of 250 μW (−6 dBm), which appeared to be optimum, this predicts a collector current of 6.32 mA. The quiescent collector current measured in the original prototype (which used high-Q components) was 6.6 mA. Phase noise measurements versus power for the original prototypes are discussed in [19].

The typical gain and phase shift were measured using a network analyzer. Fig. 5 shows the frequency response of a later amplifier operating at 7.5 mA. The measured gain at 10 MHz was 8.3 dB, while the phase shift at one of the outputs was 84.7°.

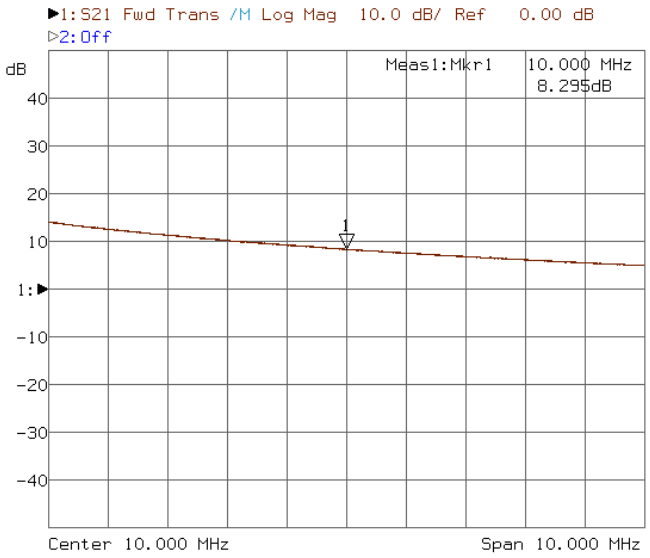

Fig. 5. Differential amplifier frequency response.

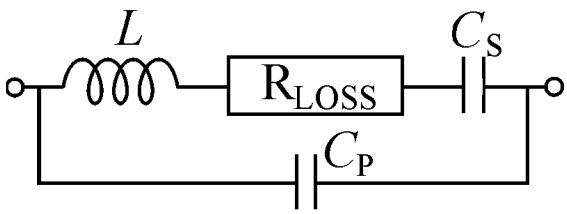

Fig. 6. Model for crystal resonator.

B. Crystal Resonator

SC cut 10-MHz crystal resonators manufactured by Nofech Ltd. were used. The characteristics specified by the manufacturers were approximately: RR ∼ 53 Ω, Q_0 ∼ 1.3 M, and turnover temperature TO ∼ 82 °C.

A simple model of the crystal resonator is shown in Fig. 6 and includes series and parallel resonant components. The crystal was placed on a test board with 50 Ω microstrip transmission lines, and its frequency response was measured using a vector network analyzer (VNA). Fig. 7 shows the measurement of the series resonance. The measured loaded Q was 491,580 (which corresponds to a bandwidth of about 20 Hz), and the insertion loss was 3.79 dB. Note that care should be taken to ensure that the sweep rate is sufficiently low to obtain accurate results. It is also quite easy to see ringing on the network analyzer if the sweep is too fast.

It is also worth noting that a low-cost compact USB-controlled VNA (VNWA v2) made by SDR kits was used as this offers subhertz resolution, easy measurement, calibration, internal crystal modeling, and the use of 50 000 points in a single sweep allowing full simultaneous measurements of all the wanted and spurious modes over 100 MHz. The stability of this network analyzer was also found to be sufficient to obtain highly accurate readings.

Simplifying the model to just the series resonant elements, it is possible to use the equation $S_{21} = (1 - Q_{\mathrm{L}}/Q_0)$ to

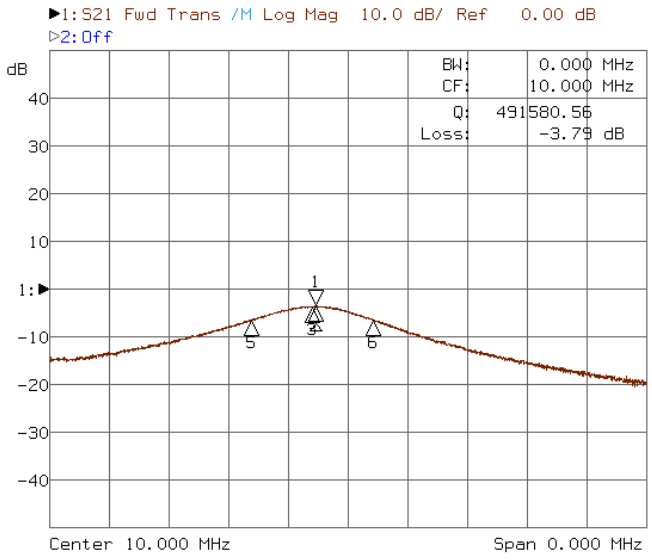

Fig. 7. Crystal resonator series resonance (span = 100 Hz).

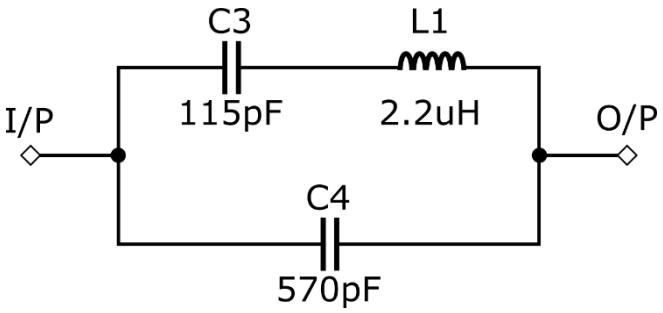

Fig. 8. Spurious resonance filter circuit diagram.

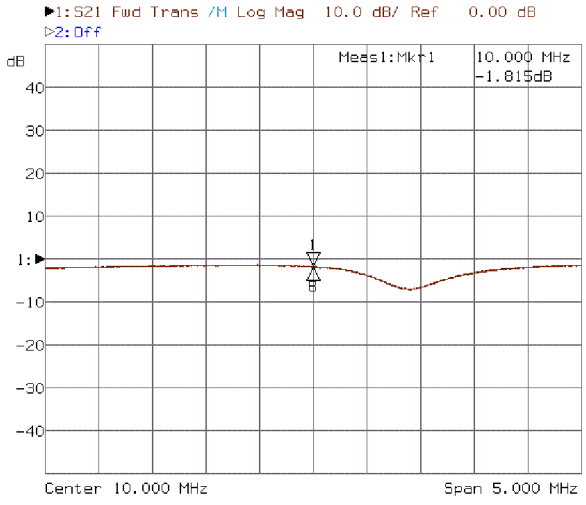

Fig. 9. Spurious resonance filter frequency response.

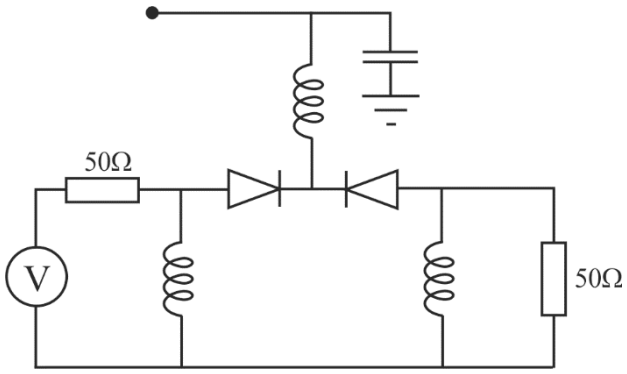

Fig. 10. Tunable phase shifter based on the fifth-order Butterworth filter.

estimate the unloaded Q. From this equation, $Q_0 = 1.39$ M (which is a about 7% higher than the manufacturer parameters). Note that more accurate modeling can be achieved by including further components in this model. By using the ratio of the series and parallel resonances, the other components can be calculated using

$$\frac{f_P}{f_S} = \sqrt{1 + \frac{C_S}{C_S + C_P}}. \tag{9}$$

C. Spurious Rejection Filter

Aside from the useful 10-MHz resonance, the crystals exhibit an unwanted spurious resonance at about 10.9 MHz. This can cause the oscillator to begin oscillating at the wrong frequency. In order to suppress this resonance, a filter was designed and incorporated into the loop. It is essential that this filter does not interfere with the main resonance, while filtering out the unwanted one. The design that was used in this case is inspired by the model of the crystal resonator. Fig. 8 shows the circuit diagram of the filter. The series *LC* resonance is tuned to 10 MHz, while the parallel resonance is tuned to 10.9 MHz. This enables an increased insertion loss in the unwanted resonance, while the loss in the useful resonance is kept to a minimum while using only three components. It also provides the correct open-loop phase shift for the oscillator. The frequency response of the filter is shown in Fig. 9.

D. Tuning Elements

Frequency tuning is typically achieved by incorporating the varactor diodes either into the resonator or by using phase-shift tuning separate from the resonator as illustrated in Fig. 3. The phase-shift tuning has the advantage that it does not degrade the resonator unloaded Q, and the phase noise degradation can be accurately calculated. This group has shown (theoretically and experimentally) that the noise performance degrades with a $\cos^4\theta$ relationship [24], [29]. Therefore, an open-loop phase error of 45° causes 6-dB degradation + the insertion loss of the phase shifter. The phase noise degradation for ±20° of phase shift is <1 dB.

The phase shifter should have low insertion loss and a near linear phase versus frequency response. A voltage-controlled phase shifter was, therefore, designed.

1) Electronic Phase Shifter: The electronic phase shifter consists of a tunable high-pass filter, as shown in Fig. 10. The design process uses a tunable high-pass filter based on a fifth-order Butterworth filter prototype used by the

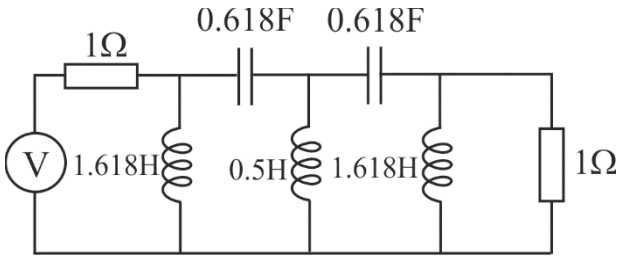

Fig. 11. Normalized high-pass Butterworth filter prototype.

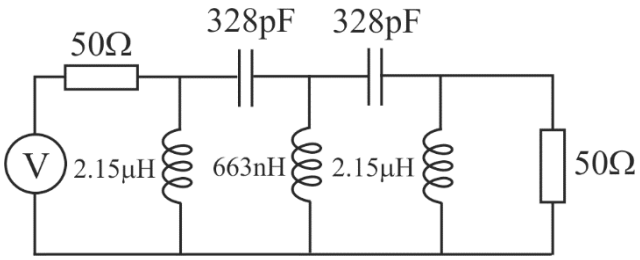

Fig. 12. 6-MHz high-pass Butterworth filter.

author for a commercial CRO design [30] and ultralow phase noise DROs [15]. The low insertion loss is ensured by always operating in the passband. As the cutoff frequency is changed, the passband phase shift (near cutoff) varies. A high-pass design was used as low-pass designs often suffer from parasitic series resonances causing increased loss [31]. The design also incorporated back-to-back diodes to enhance the power-handling capability. The network can be tuned directly from a voltage (low impedance) source ensuring no resistor thermal noise.

The initial fifth-order normalized high-pass Butterworth prototype circuit is shown in Fig. 11.

The high-pass parameters were then calculated for a cutoff frequency of $0.6\times$ fc as this was found to give good phase-shift tuning with negligible change in the insertion loss. The final 6-MHz circuit is shown in Fig. 12. The terminating impedances were chosen to be 50 Ω.

$C1$ and $C2$ are now replaced by a combination of varactors and fixed capacitors where $0.6f$ c occurs when $C1 = C2 = 328$ pF.

The varactors were chosen by considering the total capacitance and capacitance variation required in the phase shifter. The BB201 was chosen from the C–V characteristic shown in Fig. 13 (taken from the data sheet). The early prototype oscillator used BB147 varactors but these were replaced here as they are no longer available.

2) Final Circuit and Measurements: The final circuit is shown in Fig. 14, where the center inductor is now used to bias the varactors. This point should be decoupled correctly. Note that the modulation sidebands rolloff at 6 dB per octave only inside the 3-dB bandwidth of the resonator.

Two varactor diode pairs (BB201) were used in series–parallel in order to have increased tuning capability. Fixed value capacitors $C5$ and $C6$ were also added to bring the capacitance up to the filter design specifications. Capacitor

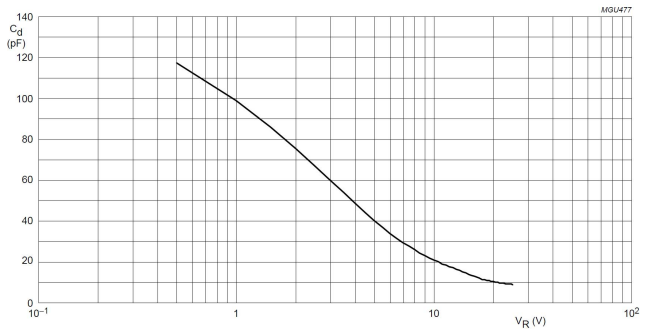

Fig. 13. C–V characteristics for BB201.

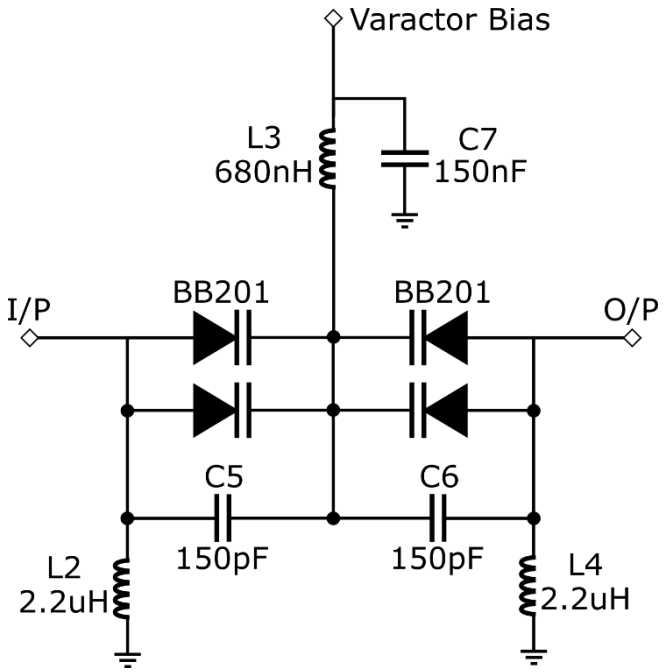

Fig. 14. Voltage-tuned phase shifter circuit diagram.

$C7$ is for decoupling inductor $L3$. This point should be driven by a low impedance source. The inductors chosen were the closest standard values to the calculated ones.

The insertion loss versus phase shift, of the phase shifter shown in Fig. 14, is shown in Fig. 15. It should be noted that the cutoff frequency of this filter starts to become close to 10 MHz (causing increased insertion loss) when the bias voltage is above 6 V, so this circuit should not be used above this point. If higher/different voltage operation is required the ratio of fixed-to-variable capacitance can be varied, and the varactors can be changed.

Using this phase shifter, the oscillation frequency can be electronically tuned within a range of a few hertz. A theoretical curve showing phase noise degradation (dB), resonator insertion loss (dB), and tuning range (linear) plotted against phase shift (degrees) is shown in Fig. 16. The normalized factor for the absolute tuning range is shown in the lowest curve in Fig. 16. For Q_{L} of 491,580 and $\pm 20^\circ$ of tuning, this predicts a tuning range of $0.36F0/(2QL) = \pm 3.7$ Hz with <1 dB of phase noise degradation.

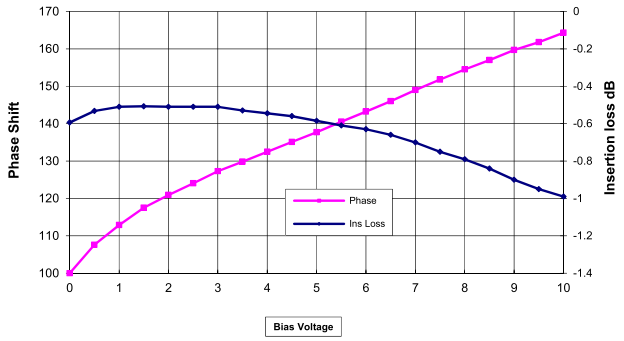

Fig. 15. Insertion loss and phase shift versus voltage.

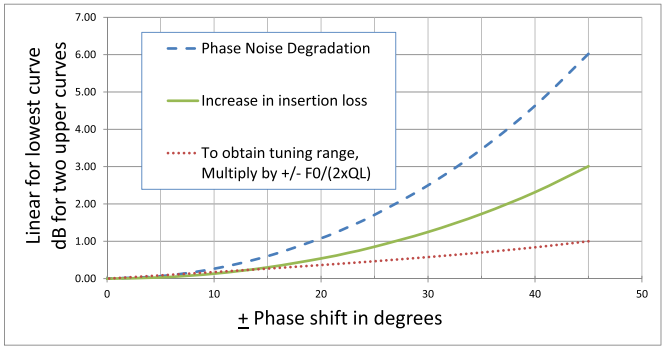

Fig. 16. Phase noise degradation, resonator insertion loss, and tuning range plotted against phase shift (degrees).

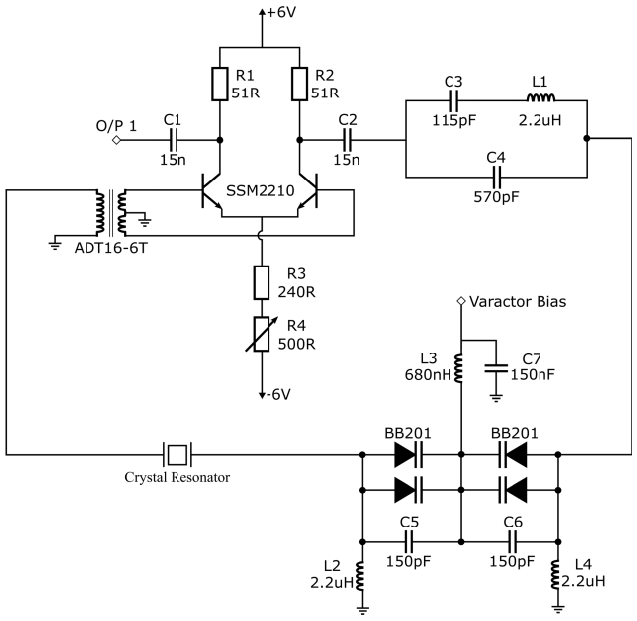

Fig. 17. 10-MHz crystal oscillator complete circuit diagram.

E. Complete Oscillator Circuit Diagram

The complete circuit diagram for the 10-MHz crystal oscillator is shown in Fig. 17. The circuit was tested in the open-loop configuration, and the transmission between the input of the transformer and the output of the resonator was measured to ensure that the correct conditions for oscillation were met. Note that the circuit was broken at the junction between

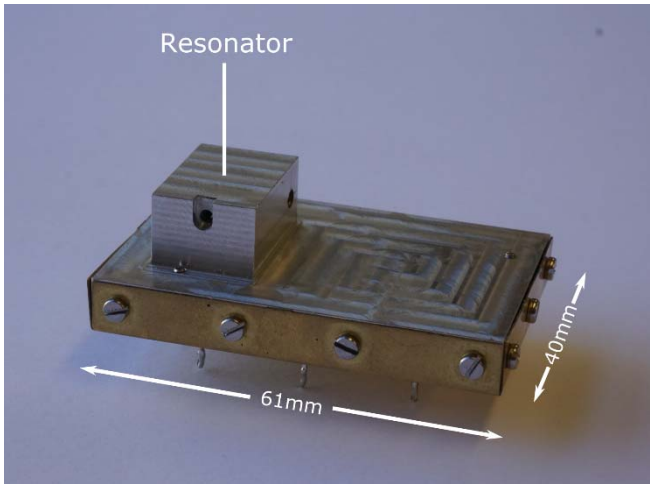

Fig. 18. Crystal oscillator in aluminum jig (Oscillator 2).

$R2$ and $C2$ as this has a 50 Ω source impedance enabling correct use of the total S-parameters. With a varactor diode bias of 1.5 V, the phase shift through the complete circuit was about 3°, and there was an excess gain of at least 1.4 dB at 10 MHz. These conditions were enough to sustain oscillation at the desired frequency. Oscillator switch-ON time is of course very slow.

IV. Phase Noise Measurements

A prototype crystal oscillator was built and powered by 4 × 1.5 V AA batteries, for both the positive and negative supplies. A 1.5-V AA battery was used for biasing the phase shifter. The oscillator was then placed inside a metal screened box.

A second, smaller oscillator was also built and placed in a specially machined aluminum jig, which provides screening and heating capabilities for both the circuit board and the crystal resonator. The jig was then covered with a brass lid, and feedthrough pins were used to provide interfaces to the bias input, output, and power supply to the oscillator (Fig. 18). This oscillator was also powered by batteries.

The phase noise was measured using the Symmetricom 5120 A (opt 01) phase noise measurement system. A total of three sets of measurements were taken: one for each individual oscillator using the internal reference of the Symmetricom instrument and one in which the two oscillators were measured against each other.

It is important to use high-quality passive components (inductors, capacitors, and resistors) for construction. Poor choice of components could degrade the phase noise by as much as 10 dB. The best phase noise results were achieved with high-Q coilcraft surface mount inductors and high-quality polystyrene capacitors. This is possibly due to the piezoelectric properties of the dielectrics, nonlinearity, and/or added flicker noise.

A. Oscillator 1

The phase noise of the first oscillator was measured using the internal reference of the measurement system. In order to

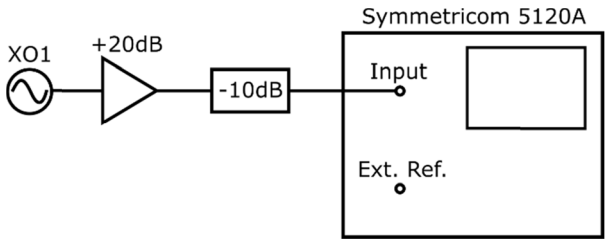

Fig. 19. Block diagram of the measurement configuration with internal reference.

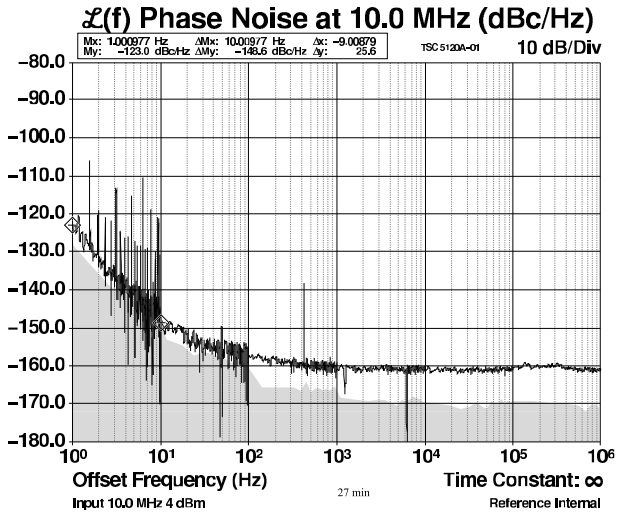

Fig. 20. Oscillator 1 phase noise performance.

TABLE I
OSCILLATOR 1 PHASE NOISE RESULTS

Offset frequency (Hz)	Phase noise (dBc/Hz)
1	-123.0
10	-148.6
100	-157.8
1,000	-161.0
10,000	-161.1

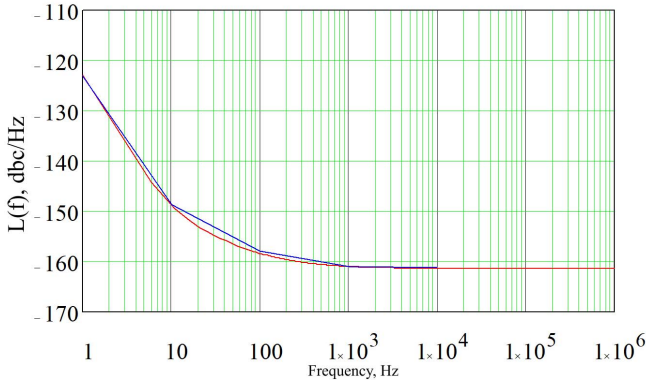

Fig. 21. Phase noise simulation using (8) and parameters from Table II.

TABLE II
PARAMETERS USED IN PHASE NOISE SIMULATION

Q_0	1.39M
Q_L	491,580
P_{AVO}	-6dBm
F_1, Noise figure of oscillating amplifier	1.8dB
F_2, Noise figure of Buffer Amplifier	4.7dB
F_c, Flicker noise corner of circuit	150Hz

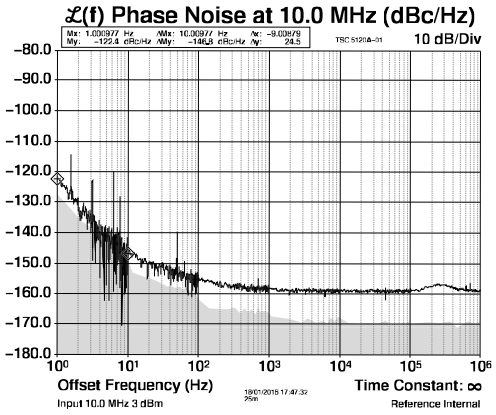

Fig. 22. Oscillator 2 phase noise performance.

bring the signal level to the value required by the instrument, a ZFL-1000 VH Mini Circuits 20-dB low-residual phase noise amplifier was used. A 10-dB attenuator was added to make sure the instrument's input was not overloaded. A block diagram of the measurement configuration is shown in Fig. 19.

The measured phase noise performance is shown in Fig. 20. The measured values are shown in Table I.

It can be seen that the oscillator shows the excellent phase noise performance down to 1-Hz offset frequency. There are multiple spurs visible between 1- and 10-Hz offsets. These could be attributed to insufficient screening, pickup from the interconnecting cables, or spurs generated by the instrument.

A theoretical phase noise plot is shown in Fig. 21 based on (2). The parameters used in (2) are shown in Table II.

The 150-Hz transposed flicker noise corner takes into account the flicker noise in the amplifier, the flicker-of-frequency noise in the resonator, and the drive level-dependent AM-to-PM conversion in the resonator.

B. Oscillator 2

The second oscillator was measured using the same measurement configuration as Oscillator 1 (Fig. 19). The measured phase noise performance is shown in Fig. 22. The values are shown in Table III.

It can be seen that there is a small increase in the phase noise at all offsets. This may be attributed to the differences in the resonators, the tolerance of the components, or the smaller volume of Oscillator 2. When the inductors are placed too close to each other, there may be magnetic coupling between them, which could alter the response of the filter and phase shifter. The spurs below 10-Hz offset are reduced in this case.

TABLE III
OSCILLATOR 2 PHASE NOISE RESULTS

Offset frequency (Hz)	Phase noise (dBc/Hz)
1	-122.4
10	-146.8
100	-155.3
1,000	-158.2
10,000	-159.0

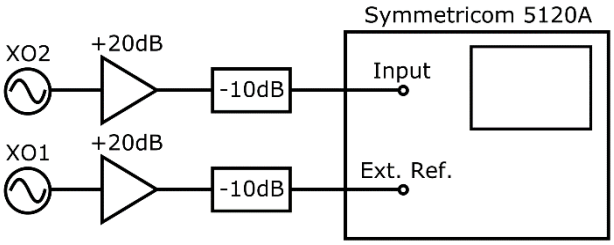

Fig. 23. Block diagram of the measurement configuration with external reference.

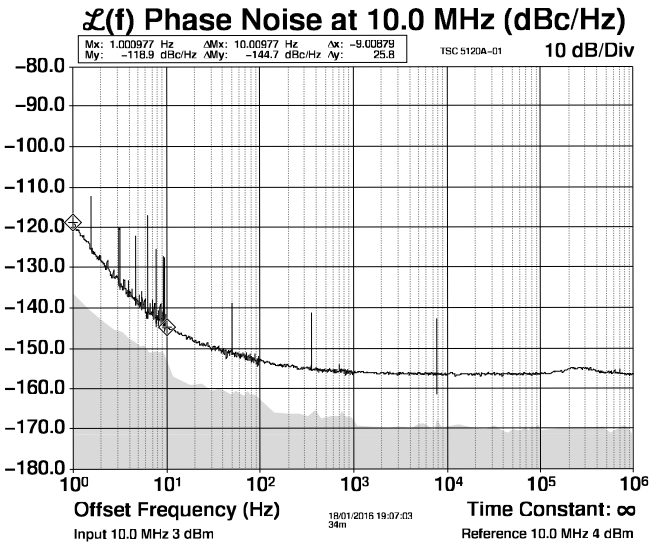

Fig. 24. Phase noise performance with Oscillator 1 as a reference and Oscillator 2 as an input.

C. Oscillator 1 Versus Oscillator 2

Both oscillators exhibit good phase noise performance when measured using the internal reference of the Symmetricom system. However, when using the internal reference, the system's noise floor is specified as "−120 dBc/Hz at 1 Hz" by the manufacturer. Therefore, it is unclear whether these results are accurate. Also, the 5120A uses cross correlation which can be prone to cross spectrum collapse [32], [33]. In order to confirm the performance, the two oscillators were measured against each other, one used as a reference and the other as the input signal, as shown in Fig. 23. This brings the noise floor of the measurement down significantly (down to −145 dBc/Hz at 1 Hz offset according to the datasheet).

The results of the phase noise measurements are shown in Fig. 24, and the values are tabulated in Table IV.

TABLE IV
OSCILLATOR 1 VERSUS OSCILLATOR 2 PHASE NOISE RESULTS

Offset frequency (Hz)	Phase noise (dBc/Hz)	Phase noise (dBc/Hz), -3dB
1	-118.9	-121.9
10	-144.7	-147.7
100	-153.2	-156.2
1,000	-156.2	-159.2
10,000	-156.5	-159.5

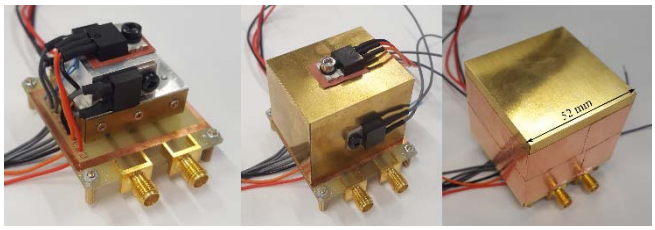

Fig. 25. Three stages of the construction of the double-OCXO.

The resulting graph shows the added noise of the two oscillators. Therefore, it is safe to estimate that the phase noise of any of the two oscillators is at least 3 dB lower than the displayed graph. This ties in with the measurements taken on each individual oscillator.

V. DOUBLE-OVEN 10-MHz CRYSTAL OSCILLATOR

The latest version of the crystal oscillator was built in a more compact package and was temperature stabilized around the inversion temperature of the resonator (82 °C) in a double-oven configuration. In this version, the polystyrene capacitors were replaced with high-quality ceramic surface mount capacitors from American Technical Ceramics. This was done for two main reasons: the polystyrene capacitors are larger, which increases the volume of the construction, and their maximum operating temperature (85 °C) is too close to the desired oven temperature. A photograph of the construction of the oscillator is shown in Fig. 25.

The oscillator circuit and resonator are contained in the aluminum jig, which is a smaller version of Fig. 18 and serves as the first oven. Power transistors and resistors were used as heating elements. They are placed around the resonator enclosure in such a way as to enable a more symmetrical and uniform distribution of heat. A layer of insulation is placed over them, followed by a brass box, which serves as the second oven. A second layer of insulation and an outer brass box complete the construction. The temperature controllers were built on FR4 boards and attached under the box using offset screws. The complete oscillator is shown in Fig. 26.

The inner oven of the oscillator was stabilized at 82 °C and the outer oven around 20° lower. The phase noise was measured in this configuration and was found to be close to the previously measured results at room temperature, with only a small degradation of about 0.6 dB.

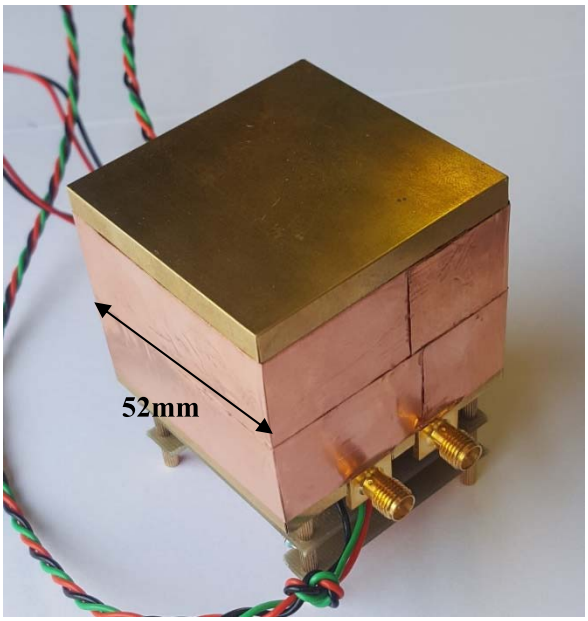

Fig. 26. Complete double-oven crystal oscillator.

VI. Further Work and Potential Improvements

The emitter resistors, as shown in Fig. 4, could be replaced with a current source. This could offer reduced sensitivity to supply ripple but could affect the flicker noise performance. It is interesting to note that the collector voltage can be reduced and the oscillator will even run with the collector shorted to ground (0 V) but the phase noise has not been checked under these conditions.

Parallel configurations of transistors could be used to reduce the noise figure, flicker noise, and the impedance transformation ratio.

VII. Conclusions

It is shown that oscillators with the excellent phase noise performance can be built using relatively simple but highly accurate linear theories and these can be implemented using a modular approach to oscillator designs, utilizing transformer coupled differential amplifiers, a three-element filter, and high-pass phase shifter designs.

Further improvements in the longer term phase noise performance are expected through the improved and optimized temperature stabilization of the resonator at turnover temperature (82 °C). Certain types of components have been found to be more effective in keeping the phase noise low.

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