Proceedings Paper:

Jung, G, Rashid, MW, Carpenter, TM orcid.org/0000-0001-5676-1739 et al. (5 more authors) (2018) Single-Chip Reduced-Wire Active Catheter System with Programmable Transmit Beamforming and Receive Time-Division Multiplexing for Intracardiac Echocardiography. In: Digest Of Technical Papers. 2018 IEEE International Solid-State Circuits Conference (ISSCC), 11-15 Feb 2018, San Francisco, CA, USA. IEEE , pp. 188-190. ISBN 978-1-5090-4940-0

https://doi.org/10.1109/ISSCC.2018.8310247

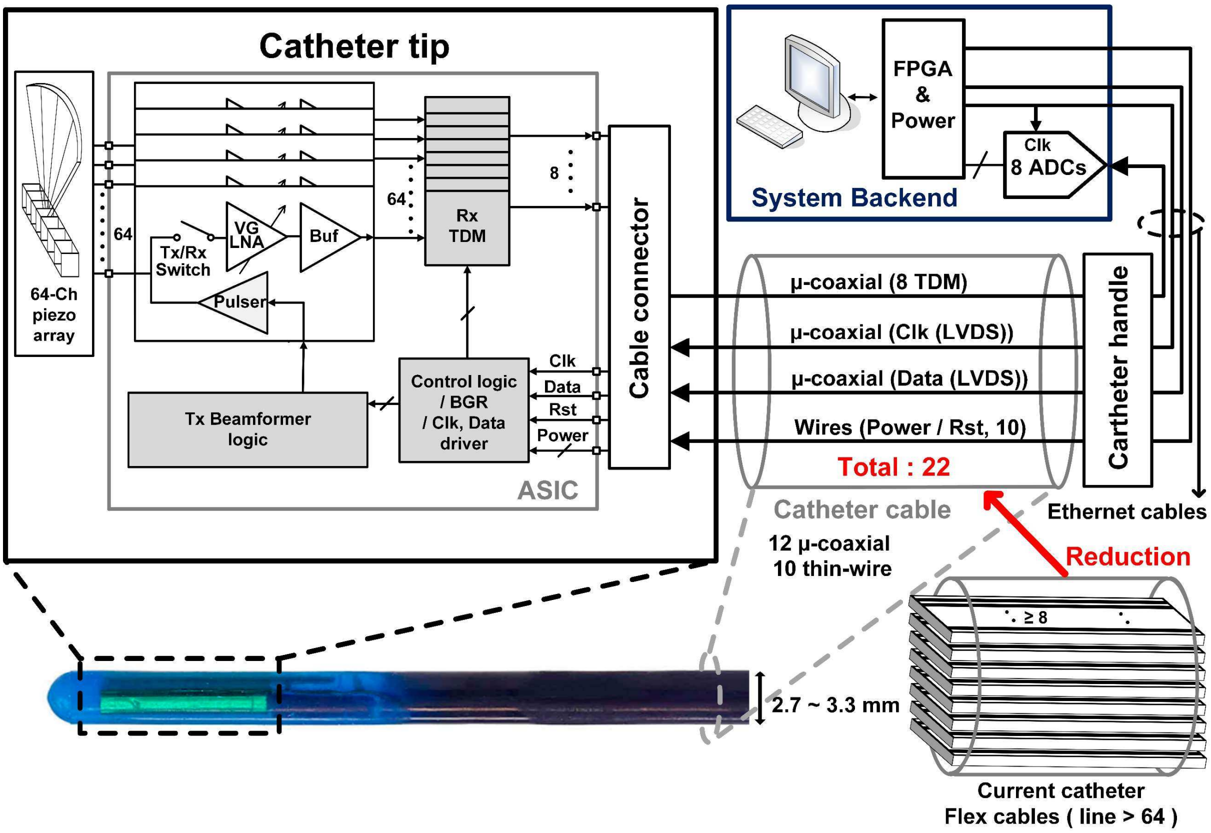

Fig. 1. Top level block diagram of the proposed intracardiac echocardiography system, including the backend, in comparison with a generic catheter.

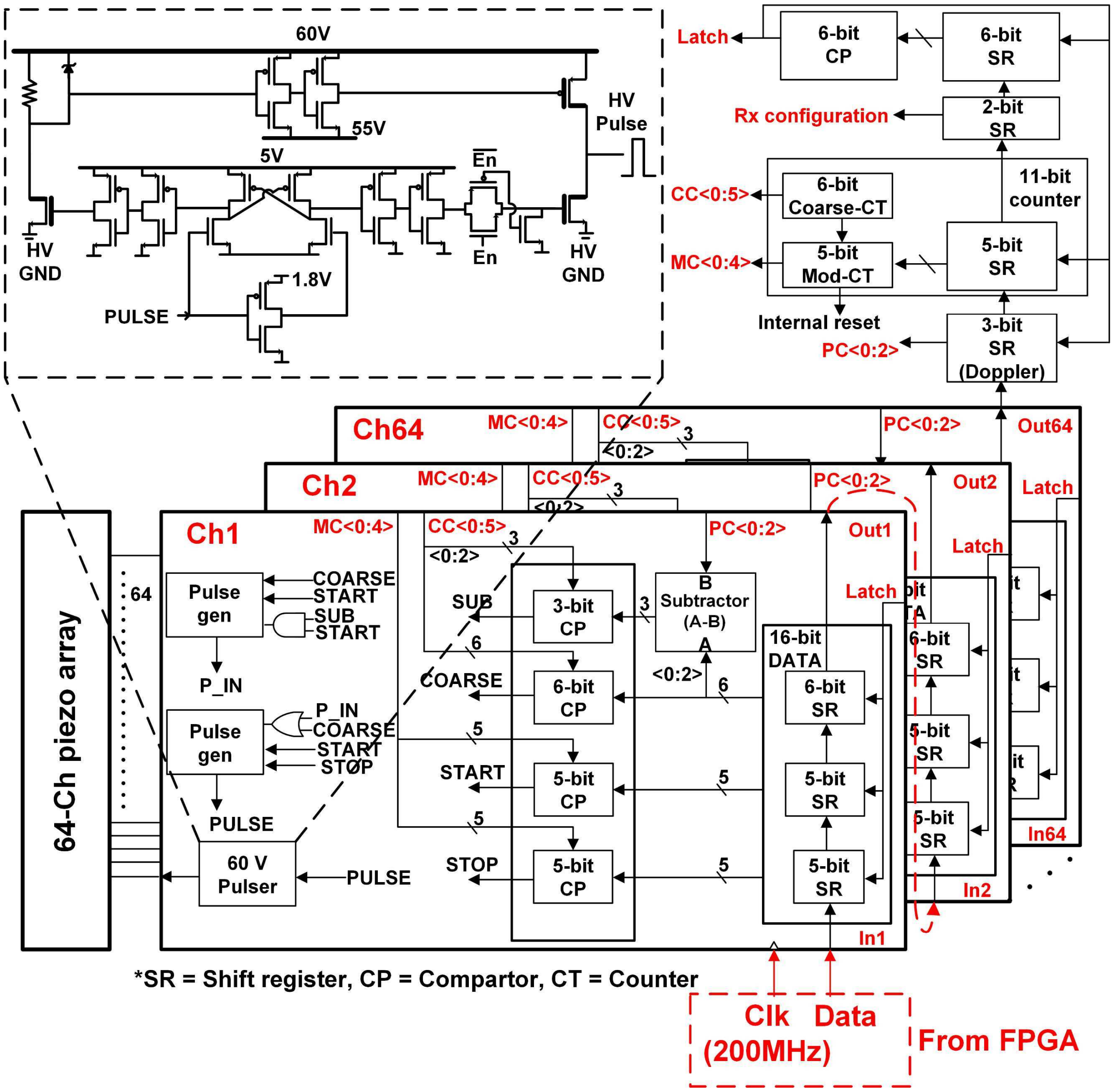

Fig. 2. Block diagram of the transmit beamformer and pulser sections of the ASIC.

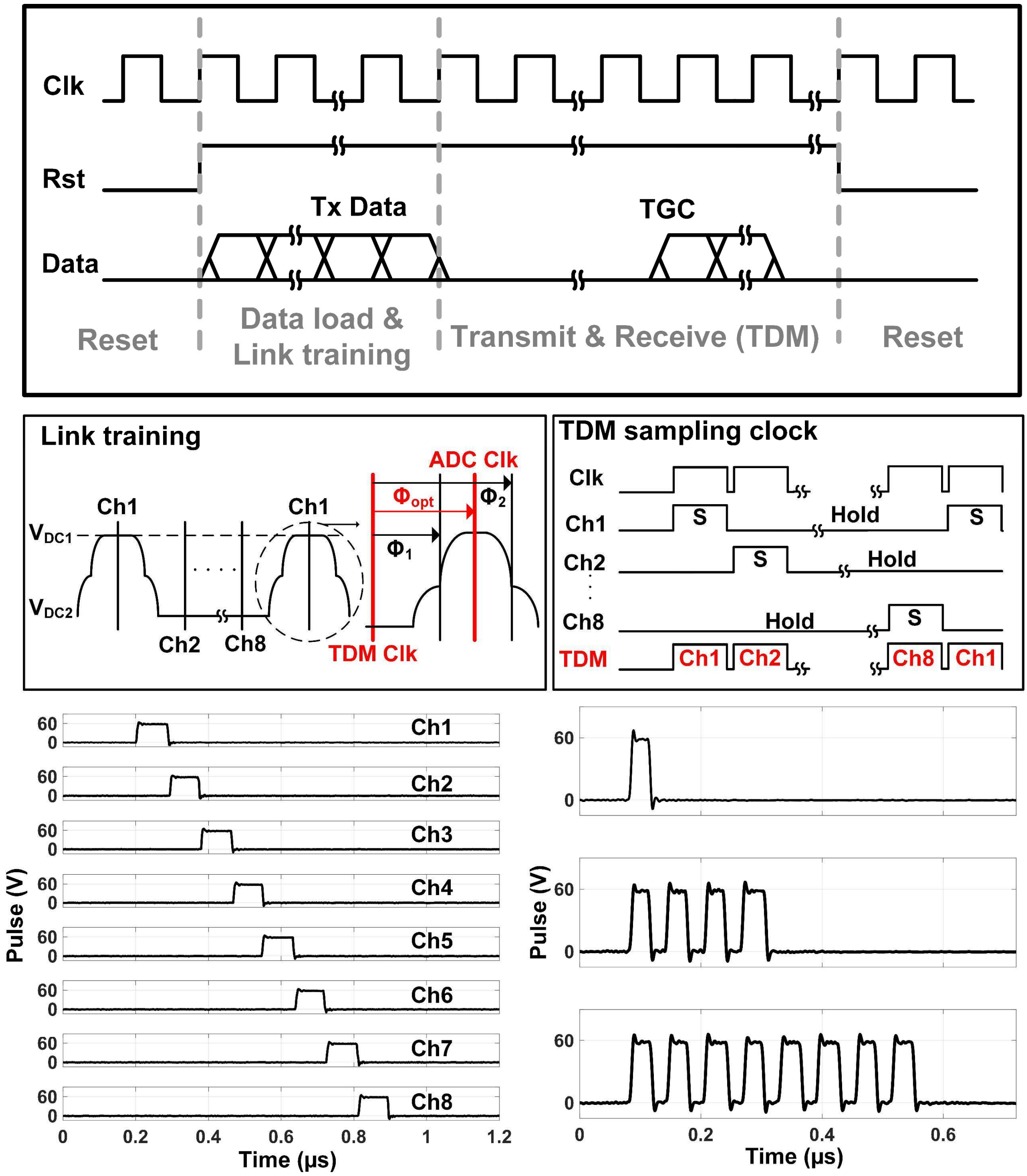

Fig. 3. Timing diagram of the system, TDM sampling clock diagram through the link training process, and measured each 90ns delayed output pulses with multiple pulse operation for Doppler imaging.

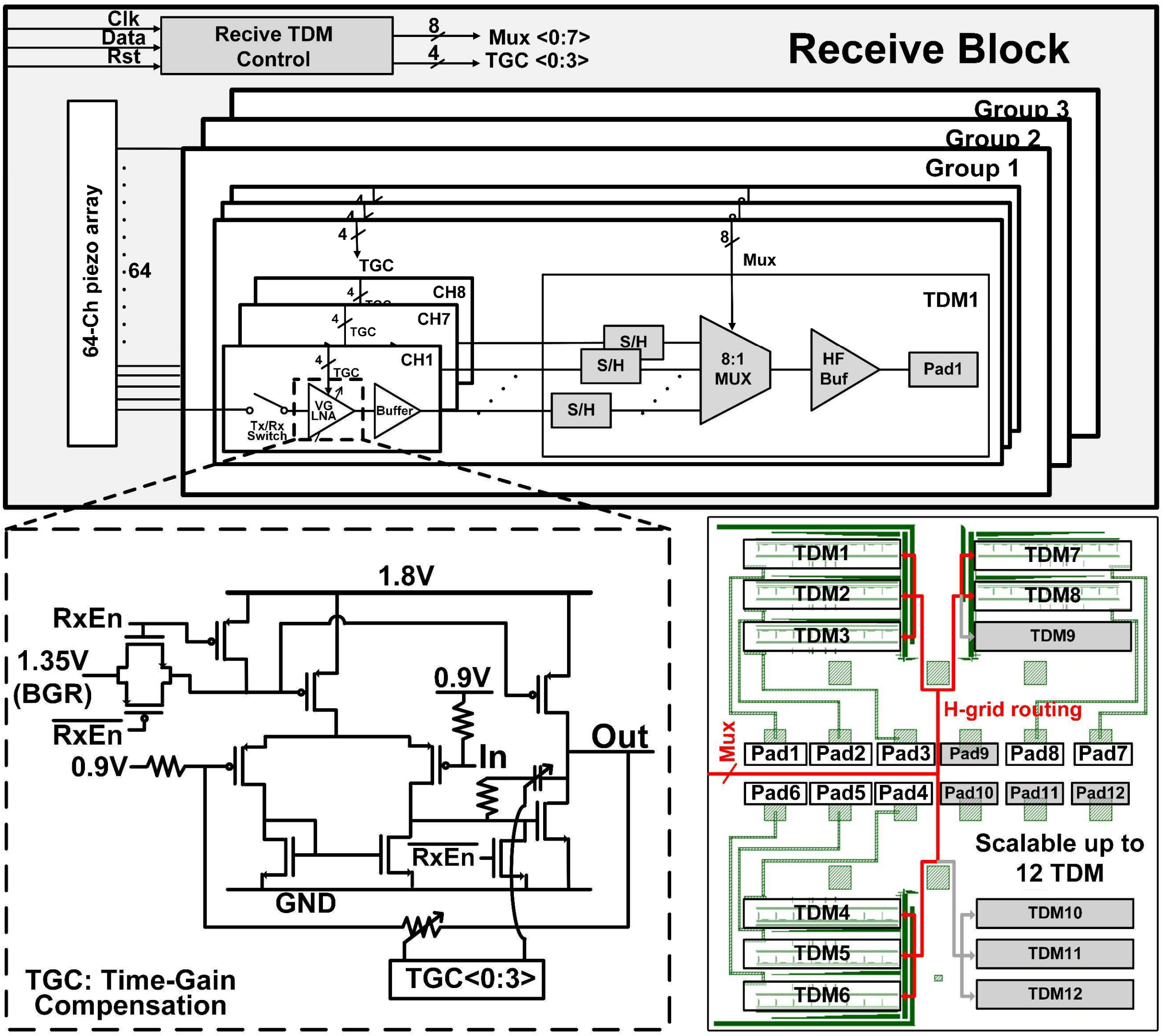

Fig. 4. Block diagram of the receiver section of the ASIC, schematic of LNA including symmetrical layout of the TDM block.

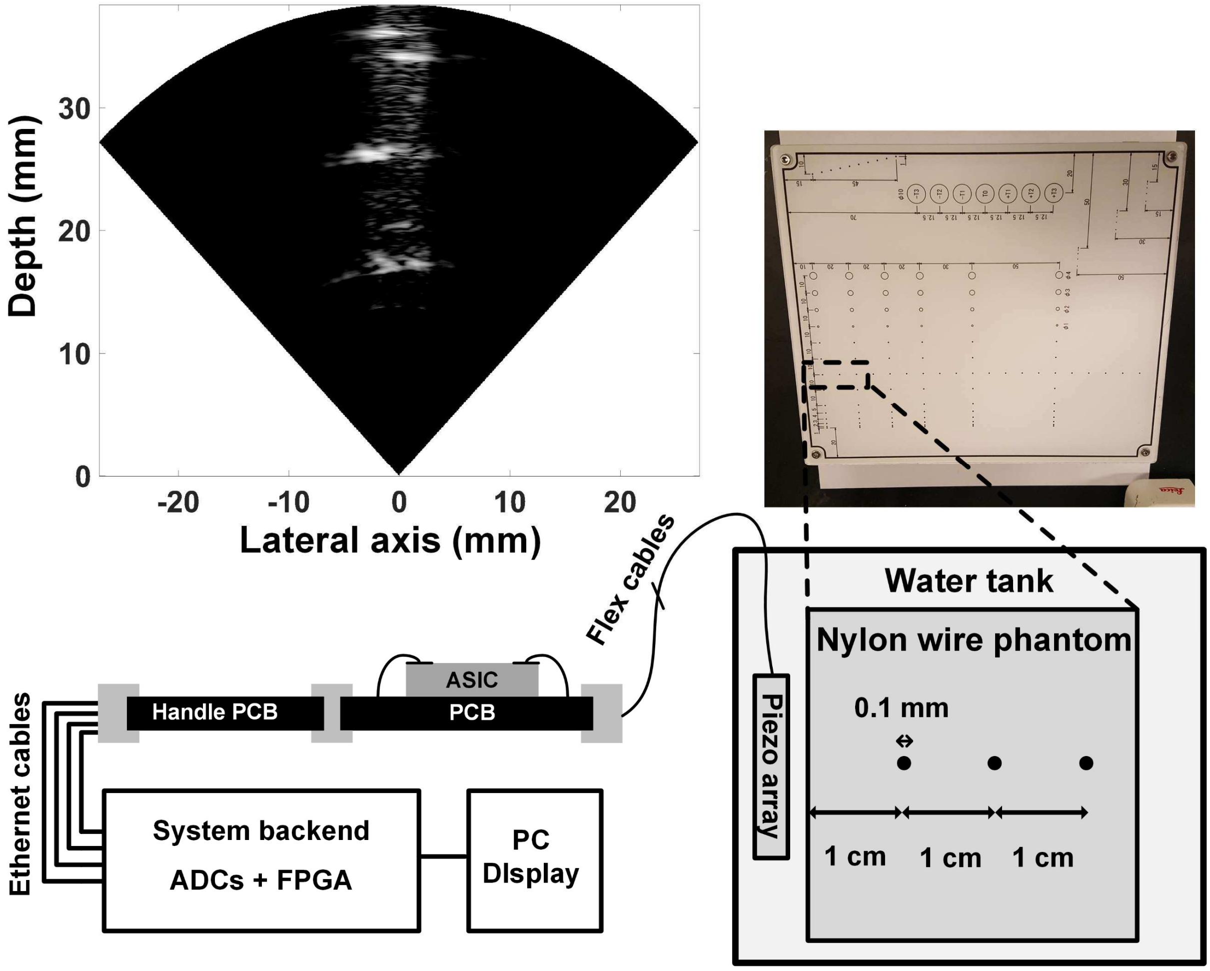

Fig. 5. Imaging setup diagram with phantom, and B-mode image of 3 nylon wires.

	This Work	[1] ISSCC'17	[2] JSSC'17	[3] ISSCC'17	[5] TBCAS'12	[6] ISSCC'14
Integrated Tx-BF	**Yes**	Yes	No	No	No	No
Rx wire reduction	**TDM**	S/H analog	S/H analog	ADC + FIFO	Analog filter	S/H + Digital
Rx raw data accessibility	**Yes**	No	No	Yes	No	No
Delay min (ns)	**5**	25	30.3	8.33	1.75 ~2.5	6.25
Delay max (us)	**10.235**	0.750	0.272	1.067	0.035	8
Die area (mm^2)	**28.6**	416.64	37.21	9.37	0.36	19.35
Die dimension(mm^2)	**2.6×11**	22.4×18.6	6.1×6.1	2.93×3.2	1.2×0.3	4.5×4.3
Power consumption / channel	**6.26mW**	0.7mW	0.27mW	17.5mW	4.62mW	17.81mW
# of channels	**64 Tx / 64 Rx**	128 Tx / 3072 Rx	1024 Rx	16 Rx	8 Rx	64 Rx
# of wires	**22**	> 128	> 160	-	-	-
Tx amplitude	**60 V**	136 V	-	-	-	-
Transducer	**PZT / CMUT**	2D PZT	2D PZT	2D CMUT	Annular CMUT	2D CMUT
Process	**0.18μm HV**	0.18μm HV SOI	0.18μm	28nm	0.35μm	0.13μm

Fig. 6. Benchmarking table of state-of-the-art ultrasound array ASICs.

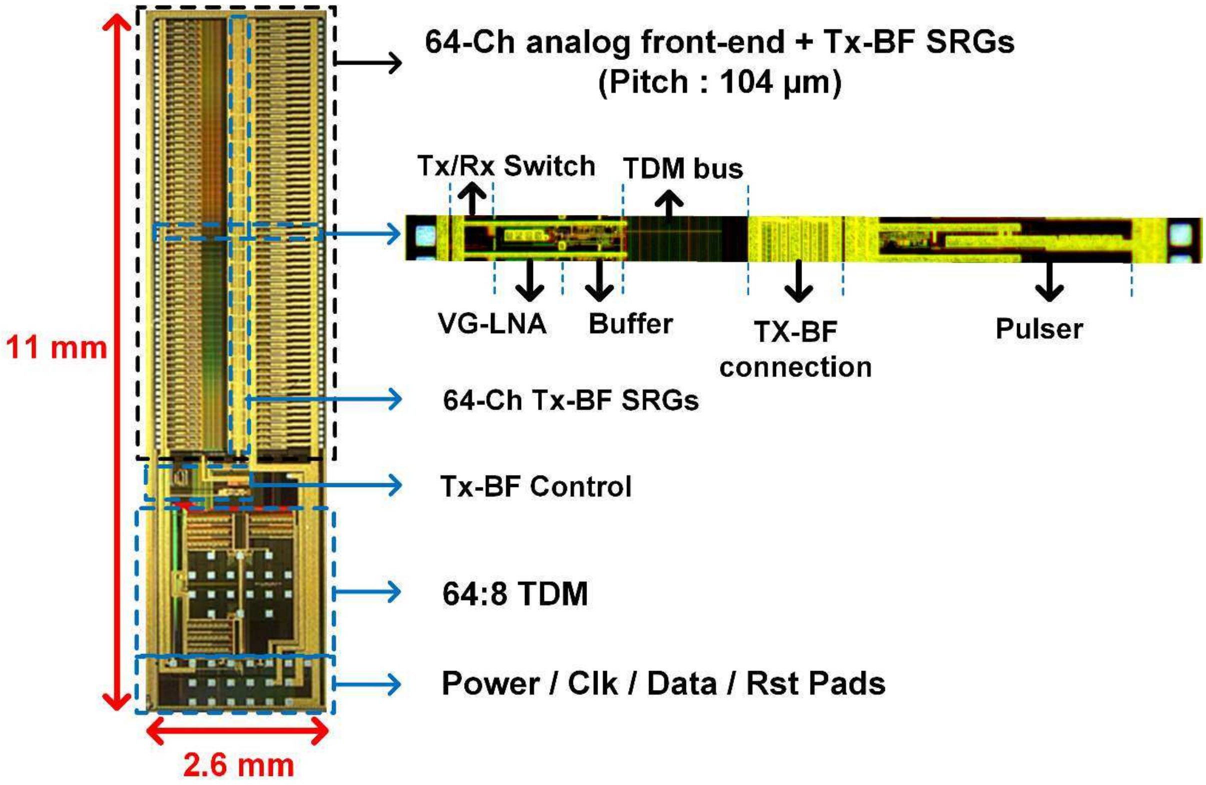

Fig. 7. Microphotograph of the 64-ch 1-D transducer interface ASIC implemented in 60V 0.18-μm HV-BCD technology.

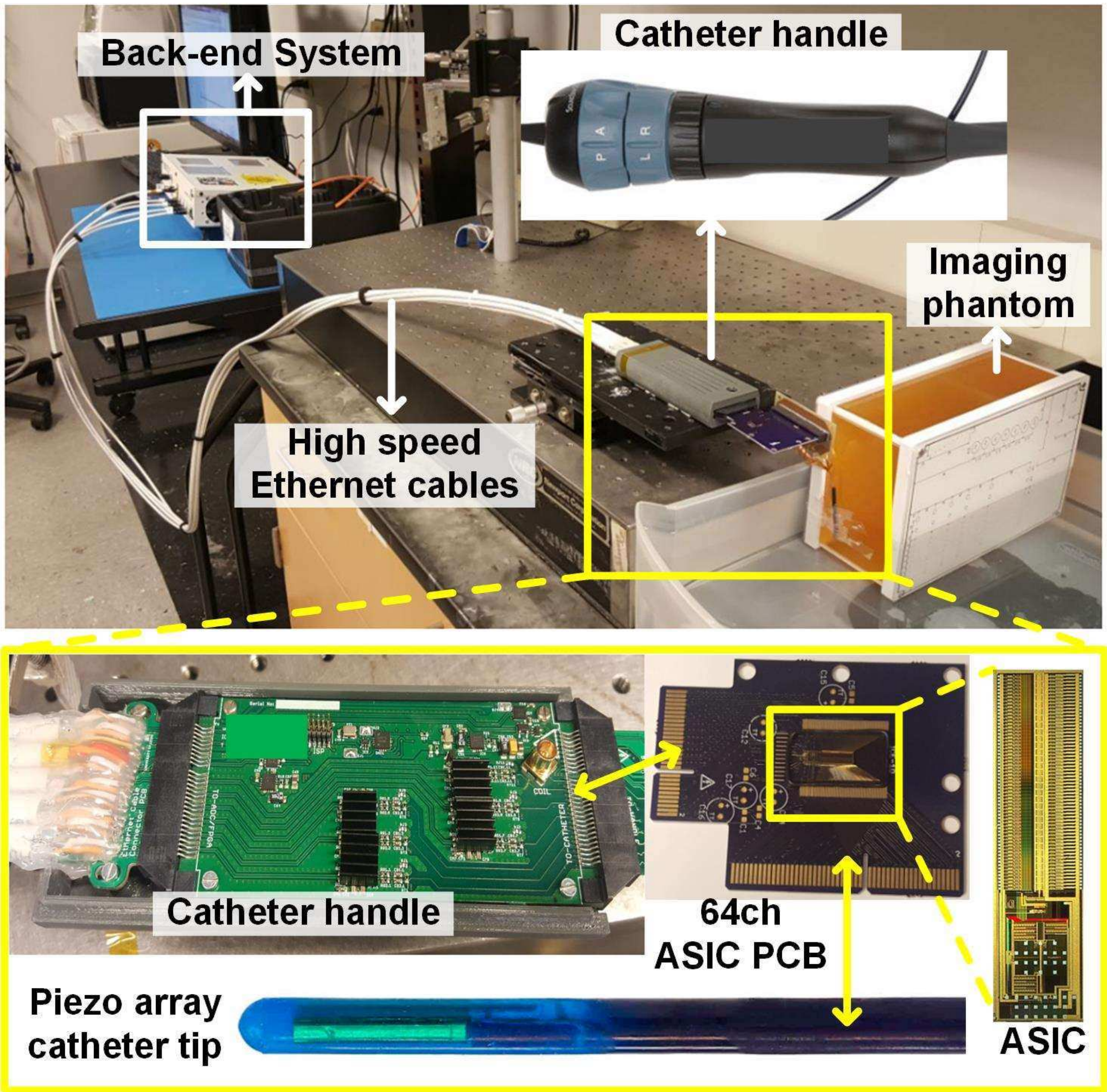

Fig. S. 1. Top: Ultrasound imaging measurement setup with various interconnects between key components of the ultrasound imaging system. Bottom: The 64-Ch piezoelectric array is connected to the Tx/Rx block of the ASIC, which is wirebonded directly on a 4 layer PCB, with 8 flex cables. The PCB that supports the ASIC, connects its 22 interconnects through a high speed connector to catheter handle, which is in turn connected to the system backend through four Ethernet cables.

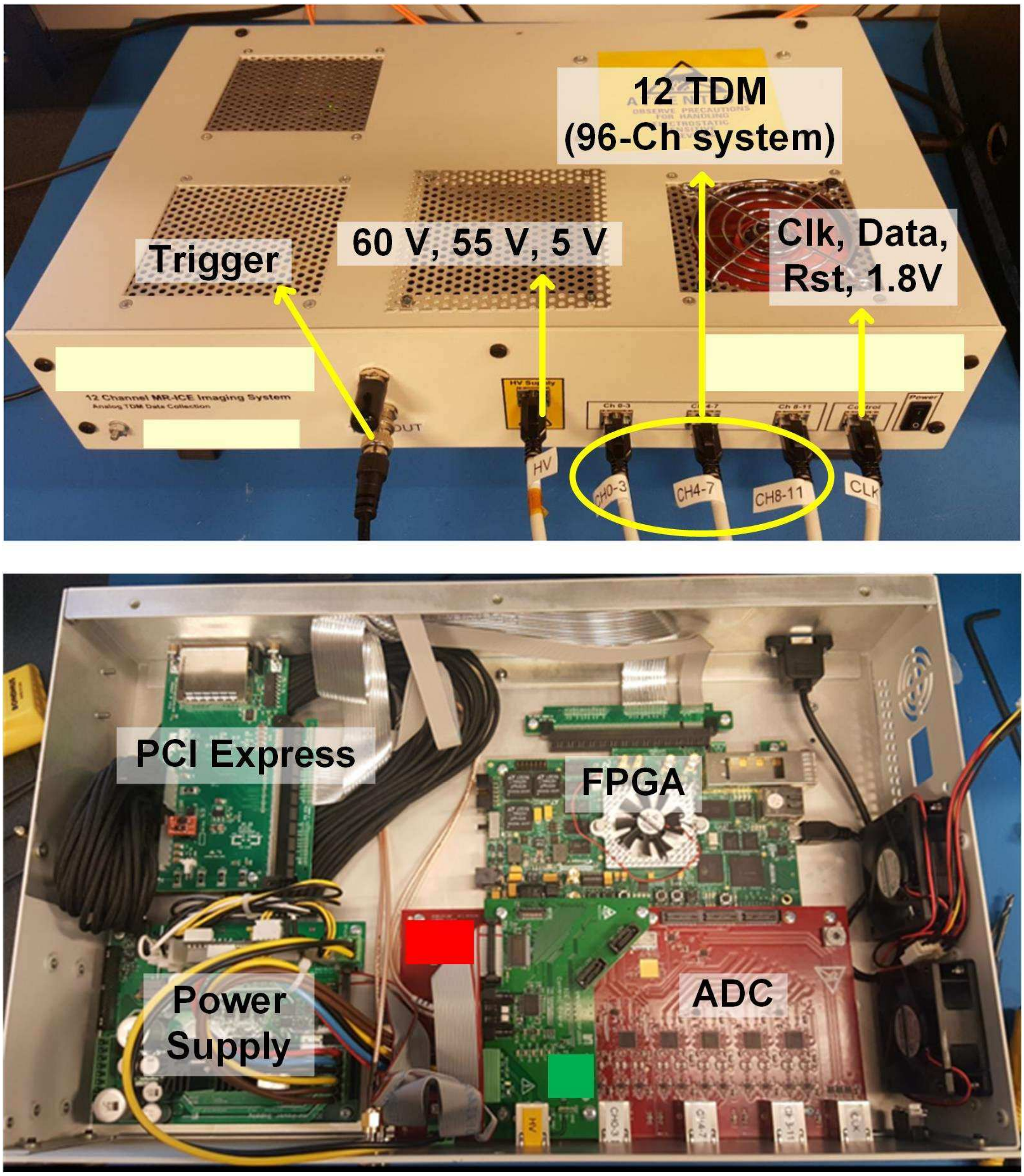

Fig. S. 2. ICE system backend consisting of 12 200 MSPS ADCs (ADC16DX370 from TI) embedded in a PCB to support up to 12 TDM signals, a FPGA board (5SGSMD5K2F40C2N from Altera), power supply module, and a PCI express card, which delivers data from FPGA to PC via optical cable.

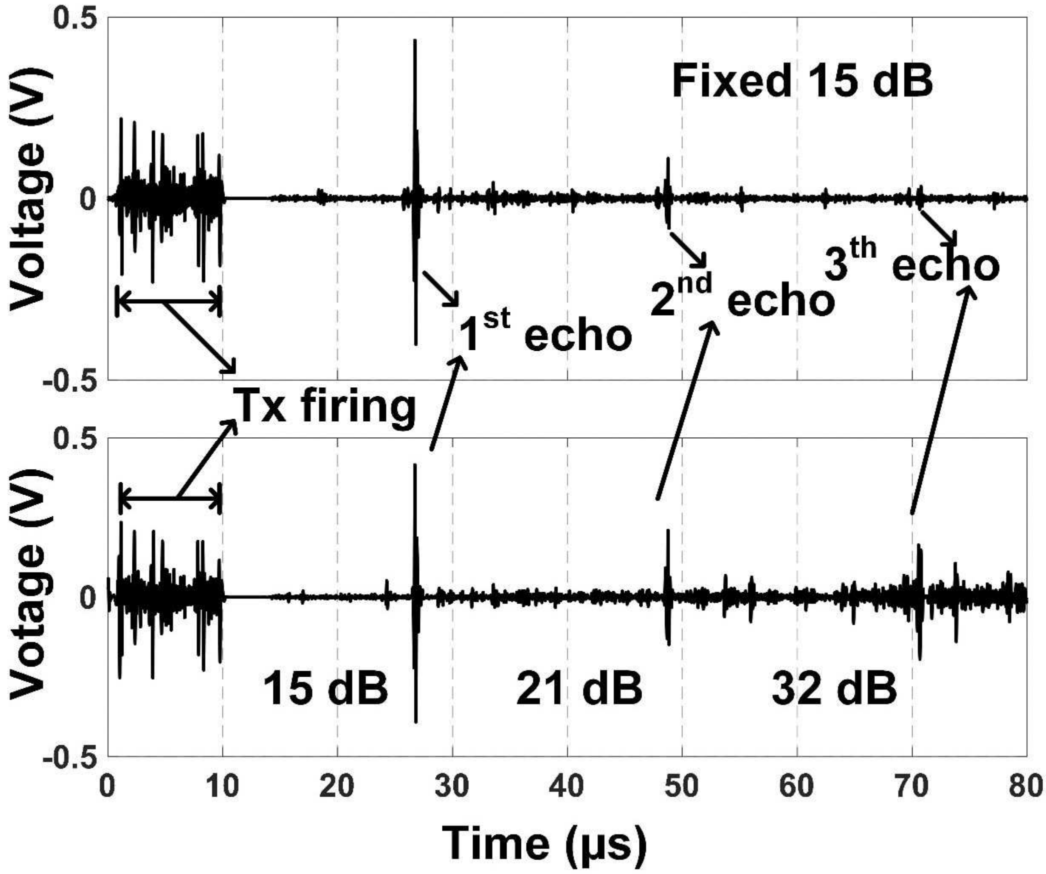

Fig. S.3. Top graph: 3 measured echoes reflected from a metal reflector at 1.6cm without TGC after TDM and DDD. Bottom graph: Same pulse-echo signal measured with TGC enabled, gain increases over time from 15 dB to 21 dB, and 32 dB to compensate for attenuation in the further echoes.