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Proceedings Paper:
Jung, G, Rashid, MW, Carpenter, TM et al. (2018) Single-Chip Reduced-Wire Active Catheter System with Programmable Transmit Beamforming and Receive Time-Division Multiplexing for Intracardiac Echocardiography. In: Digest Of Technical Papers. 2018 IEEE International Solid-State Circuits Conference (ISSCC), 11-15 Feb 2018, San Francisco, CA, USA. IEEE, pp. 188-190. ISBN: 978-1-5090-4940-0. ISSN: 2376-8606.

https://doi.org/10.1109/ISSCC.2018.8310247

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Single-Chip Reduced-Wire Active Catheter System with Programmable Transmit Beamforming and Receive Time-Division Multiplexing for Intracardiac Echocardiography

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Intracardiac echocardiography (ICE) provides real-time ultrasound imaging of the heart anatomy from inside, guiding interventions like valve repair, closure of atrial septal defects (ASD) and catheter based ablation to treat atrial fibrillation. With its better image quality and ease of use, ICE is becoming the preferred imaging modality over transesophageal echography (TEE) for structural heart interventions. The existing commercial ICE catheters, however, offer a limited 2-D or 3-D field of view despite catheters utilizing large number of wires. In these catheters, each element in the ICE array is connected to the backend data acquisition channel with a separate wire, which is a critical barrier for improving image quality and widening the field of view. In order to use ICE catheters under MRI instead of the ionizing X-ray radiation based angiography, the number of interconnect wires in the catheter should be minimized to reduce RF-induced heating. Furthermore, reducing the number of wires improves the flexibility and lowers the cost of the single-use ICE catheters.

To reduce the number of interconnects in ultrasound systems, recent literature show subarray beamforming with switched-capacitor delay [1], [2], digital subarray beamforming with ΔΣ modulator [3], and time-division multiplexing (TDM) with direct digital demultiplexing (DDD) [4]. The switched-capacitor approach is preferred in 2-D arrays, however, a large number of capacitors and switches are needed for each channel for reasonable delay, which introduce mismatch, and makes it difficult to fit in the ICE catheter. It is also not compatible with applications that need access to the raw echo data of every channel for improved image processing. The ΔΣ modulator approach has shown compact integration. However, it requires high frequency

clock (960MHz), which is difficult to feed into long catheters, limiting the integration of high voltage (HV) Transmit (Tx) circuits with thick gate oxide on a single chip.

This paper presents a single-chip reduced-wire active catheter system for driving a 64-Ch piezo-transducer array, which adopts 8:1 TDM analog receiver (Rx) with DDD, and Tx-beamformer (Tx-BF), which can be programmed with a single low voltage differential signaling (LVDS) data line for wire reduction. Fig. 1 shows the ICE system block diagram focusing on the front-end ASIC, which reduces the number of wires from more than 64 to 22. The 64-Ch received raw echo signals are reduced to 8 through TDM, and sent to ADCs in the backend system, where DDD is performed in FPGA for real-time image processing in the digital domain.

Fig. 2 shows detailed block diagram of the Tx-BF and 64-Ch pulser array of the ASIC. It can create a maximum delay of 10.235μs with a resolution of 5ns, using an 11-bit global counter (GC). The 6-bit coarse counter (CC) part of GC starts to count down from 63 to find the coarse delay of each channel, while the 5-bit mod counter (MC) part of GC is programmed to find the exact start time and the width of a pulse for each channel. Each channel of the 16-bit serial-in parallel-out (SIPO) shift register (SR) stores Tx delay and pulse width values for each pulser, which can enable Tx pulse-width apodization for side-lobe suppression. A 6-bit SR is used to check proper data loading, a 2-bit SR is used for Rx configuration, and a 3-bit SR stores the number of firing pulses for Doppler operation. To program firing delays for all 64 Ch, each programming cycle requires a 1040-bit data packet (64×16+2+3+5+6). Before programming the Tx-BF, all registers are reset, following which the data packet is sent from an FPGA according to the timing diagram in Fig. 3. The 60V pulser can drive 15pF of capacitive loading at 7MHz, which is suitable for comparably-sized 1-D ICE piezo transducer array. The pulser is designed to limit the peak level-shifter current to 5mA from 60V supply by adding a 55V supply and a 5V buffer chain, avoiding voltage drop across the 6.7mm on-chip 60V powerline. Fig. 3 also shows measured results indicating functionality of the Tx-BF and 60V pulser.

The Rx block in Fig. 4 operates at 1.8V and consists of Tx/Rx switches, variable gain (VG) LNAs, buffer, and TDM circuitry with a symmetric layout, which reduces mismatch. Tx/Rx switches protect the Rx blocks from 60V pulses. Time-gain compensation (TGC) can be applied via data line to set the 2-stage LNA gain to one of 4 fixed levels (15, 21, 27, and 32dB), which on average shows 4.6nV/√Hz of the input referred noise at 7MHz. The buffer delivers the amplified echo signal into a TDM circuit, which consists of an analog multiplexer and sample and hold (S/H) capacitors. TDM is controlled by a block that generates sample clocks for each of the 8 channel by gating the corresponding clock. The ADC timing, generated by the backend system, is accurately synchronized with the TDM clock to make sure each ADC sample corresponds to a channel in the multiplexed data, following transients. Since properties of the catheter change depending on its surrounding environment, link training is performed (Fig. 3), as described in [4]. In this work, TDM operates at 200MHz, yielding 25MSPS for each channel, suitable for the echo signal that is centered at 7MHz with 80% bandwidth. The sampled TDM signals are sent out from the catheter handle to backend ADCs through 3m-long Ethernet cables.

The prototype ASIC is fabricated in 60V 0.18-μm HV-BCD process. Fig. 7 shows a microphotograph of the entire ASIC, which consists of 64-Ch analog front-end (Pulser, Tx/Rx switch, LNA, and buffer), Tx-BF, and TDM, which occupies 2.6×11mm^2, and consumes 401mW average power during B-mode imaging. Each of Tx/Rx AFE channels occupies 0.26mm^2, which is matched to the size of each ICE array element. Successful proof-of-concept imaging experiments are performed by connecting the ASIC, wire-bonded on a PCB, to a 64-Ch piezo transducer array at the tip of an ICE catheter using flex cables. Fig. 5 shows the early B-mode images obtained on a standard imaging phantom (N-365, Kyoto kagaku) of 3 nylon wires with 30dB of dynamic range. Fig. 6 benchmarks the state-of-the-art ultrasound ASIC designs. This work has integrated both Tx beamforming and Rx cable reduction in a single chip, reducing the number of wires down to 22, with 5ns of delay resolution within a span of 10.235μs, while providing the backend image processing engine with

access to the entire raw echo data from every channel. The complete backend system is designed with the capacity to handle up to 12 TDM signals from a 2-D transducer array, which will occupy the same footprint on the ASIC, as shown in Fig. 4 layout, while supporting a 96-Ch system. Since the size of pulser often limits the minimum size Tx/Rx elements on the ASIC, the reduced capacitive loading helps with matching the transducer unit area. This architecture is also compatible with subarray beamforming with switched-capacitor delay, which will pave the way to further reduction in the number of wires in ICE catheters, while supporting higher resolution 3D images.

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