A Reduced-Wire ICE Catheter ASIC with Tx Beamforming and Rx Time-Division Multiplexing

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Abstract—This paper presents a single chip reduced-wire active catheter application-specific integrated circuit (ASIC), equipped with programmable transmit (Tx) beamforming and receive (Rx) time-division multiplexing (TDM). The proposed front-end ASIC is designed for driving a 64-channel 1D transducer array in intracardiac echocardiography (ICE) ultrasound catheters. The ASIC is implemented in 60 V 0.18-μm HV-BCD technology, integrating Tx beamformers with high voltage (HV) pulsers and Rx front-end in the same chip, which occupies 2.6×11 mm^2 that can fit in the catheter size of 9 F (<3 mm). The proposed system reduces the number of wires from >64 to only 22 by integrating Tx beamformer which is programmable using a single low-voltage differential signaling (LVDS) data line. In Rx mode, the system uses 8:1 TDM with direct digital demultiplexing (DDD) providing raw channel data which enables dynamic Rx beamforming using individual array elements. This system has been successfully used for B-mode imaging on standard ultrasound phantom with 401 mW of average power consumption. The ASIC has a compact element pitch-matched layout, which is also compatible with capacitive micromachined ultrasound transducer (CMUT)-on-CMOS application. This system addresses cable number and dimensional restrictions in catheters to enable ICE imaging under magnetic resonance imaging (MRI) by reducing radio frequency (RF) induced heating.

Index Terms—Medical ultrasound imaging, time division multiplexing, capacitive micromachined ultrasound transducers (CMUT), intracardiac echocardiography (ICE).

I. INTRODUCTION

INTRACARDIAC echocardiography (ICE) has become an important clinical modality in interventional ultrasound imaging [1], [2]. It requires a minimally invasive procedure with local anesthesia to place a catheter in the right side of the heart to guide interventions like valve repair, placement of stents, closure of atrial septal defects (ASD), and catheter-based ablation to treat atrial fibrillation [3].

Current commercial ICE catheters offer a 2D or limited 3D field of view in spite of large number of interconnections, which are mainly determined by the number of array elements and ground connections. Each element in the ICE array is connected to the analog-front-end (AFE) residing in an external ultrasound system with a separate long flexible wire, which is a significant limitation for improving image quality and increasing the number of elements. Also, in order to use ICE catheters under MRI instead of the ionizing X-ray radiation-based angiography, the number of interconnect wires in the catheter should be decreased to reduce RF-induced heating of the conducting lines to acceptable levels and the catheter tip should be visible [4], [5]. Reducing the number of connections by integrating electronics at the catheter tip would improve the overall system performance by capturing the receiver signals with higher fidelity, and transmitting them to the backend using higher quality cables which reduce the spurious interference present in the catheterization labs. Cable reduction would also improve the mechanical flexibility of these single use catheters, and possibly lower the cost. Therefore, integrating electronics at the catheter tip would have a significant impact in the catheter-based ultrasound imaging applications.

When designing the integrated systems on a chip for imaging application, ideally the quality of the resulting images should not be compromised while improving other aspects such as the cable count. In the application considered here, 64 element 2D imaging ICE catheter, to preserve the image quality, the raw data from each channel (without pre-combining signals from multiple array elements) should be available in the backend as in the current ICE catheters. That enables dynamic receive (Rx) beamforming techniques to be applied without limitations. The transmit (Tx) and Rx aperture size should be maximized making use of the full width of the catheter so that the image resolution and penetration depth are not compromised [6]. This requires Tx beamformer be integrated along with the Rx circuitry on the chip using a high voltage (HV) process and connected to the backend system with small number of cables

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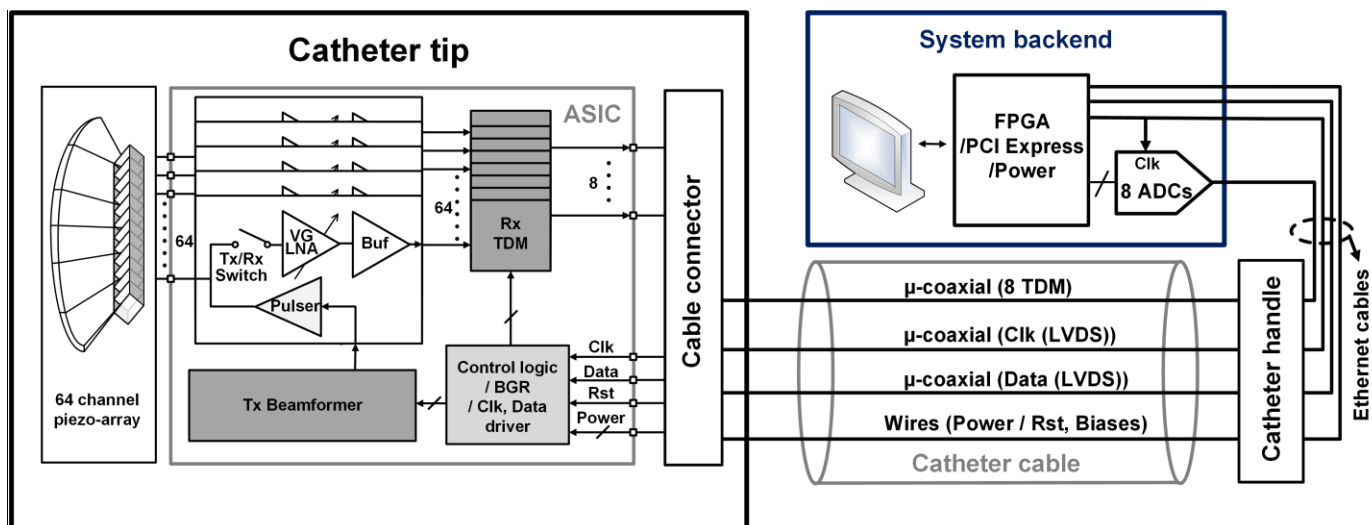
Fig. 1. Simplified block diagram of the proposed ICE catheter system which includes backend system.

and use the same maximum array area. Furthermore, the layout of the chip should be such that it is suitable for cable interconnect within the size limitations of the catheter tip. This paper demonstrates the first implementation of such an integrated system that combines a single cable programmable Tx beamformer and provides raw Rx data with 8:1 time division multiplexed receiver frontend for cable reduction.

On the Rx side, time division multiplexing (TDM) with direct digital demodulation (DDD) is used in this work as it provides -35 dB or below electrical crosstalk between channels with μ-coax cables suitable for ICE imaging [7]. This figure can be further reduced by digital signal processing techniques [8]. Noting that in current miniature ultrasound systems, electrical crosstalk below -25 dB is acceptable [9], TDM emerges as a viable and simple option as compared to more robust but more complex and power consuming digital data transmission. Frequency division multiplexing (FDM) also has been shown to be feasible to provide raw channel data for ICE application [10]. However, this approach requires multiple analog filters and mixers that are vulnerable to process variations, which will increase the mismatch and complexity of the system. Another common method to reduce the number of wires in ultrasound systems on the receiver side is subarray beamforming (μ-beamforming) [11]. Recent implementations of this method include a switched-capacitor-based delay and addition of an on chip digitizer and digital line driver [12]. Another digital subarray beamformer uses ΔΣ modulator [13]. However, this system requires high frequency operation (960 MHz), which is difficult to feed into long interconnects in catheter-based applications, and limits integration of HV Tx circuits with thick gate oxide on a single chip. Note that these systems do not utilize the full aperture for Tx and Rx or do not integrate the Tx beamformer electronics which can be challenging to integrate with low voltage digital electronics. Furthermore, subarray beamforming methods inevitably compromise imaging performance as compared to a fully sampled array targeted here due to limited steering angles and

angular directivity of the subarrays, which does not provide raw data information [14].

As mentioned above, the more critical aspect of cable reduction is single chip integration of the Tx beamformer at the catheter tip. Without Tx beamformer integration, only Rx cable reduction does not result in a practical imaging system. Single chip integration is essential to have a system size suitable for a catheter with a short rigid section at the tip. Single chip integration avoids complex through wafer vias for stacking chips and simplifies acoustic design. There are few examples of fully integrated Tx beamformer/Rx frontend systems. A system with more than 3000 transducer elements has been realized with Tx/Rx capability using subarray beamforming [15]. However, this system is developed for hand held probes to be used outside of the body. Other systems suitable in size for catheter implementation utilize subarray beamformers resulting in compromise in image quality and system complexity as noted by others [3] [12]. Other approaches to Tx beamformer implementation either require the number of cables proportional to the number of elements [16] with an external counter, or the beamformer has limited operation ability by only firing one pulse for each channel [17]-[19]. Another on-chip beamformer with integrated counter was presented in [20], however, it still requires multiple control signals to generate pulse for each channel.

In this paper, we describe a single chip solution for 2D imaging ICE catheter system, which limits the ASIC design to 9 F (<3 mm width) in size, and less than 0.5 W of power as the main constraints. The proposed ASIC adopts 8:1 TDM with DDD and Tx beamforming circuit requiring a single low voltage differential signaling (LVDS) data line for cable reduction. This paper is organized as follows. Section II describes the proposed system architecture including brief explanation of backend system. The details of the Tx ASIC level operation is provided in Section III, and the Rx operation is described in Section IV. The electrical measurements and acoustic experiments are presented in Section V. Further
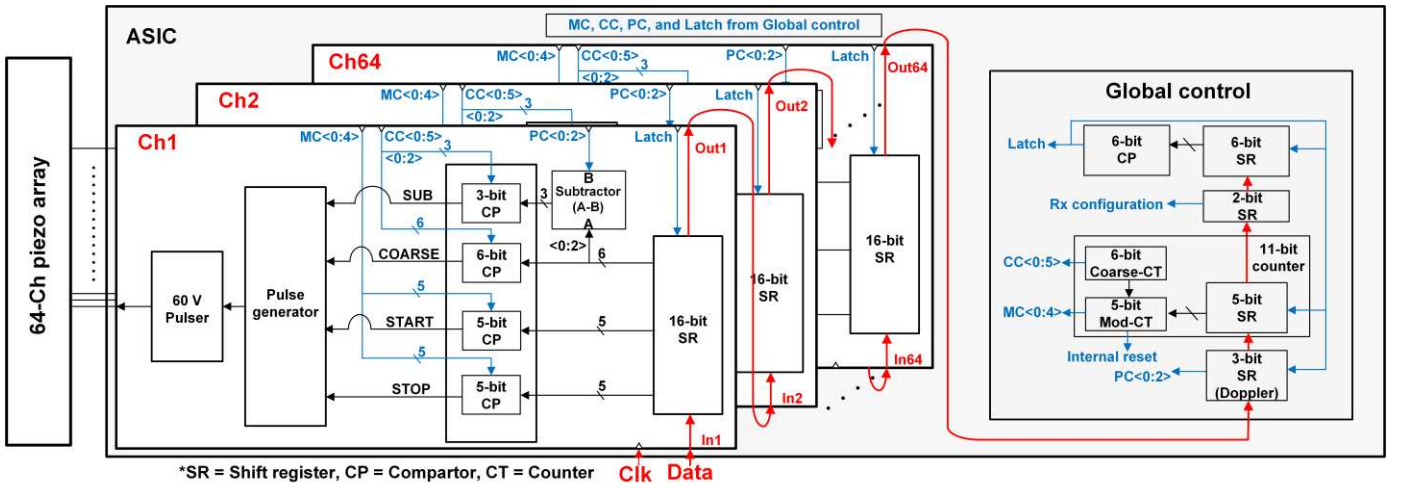
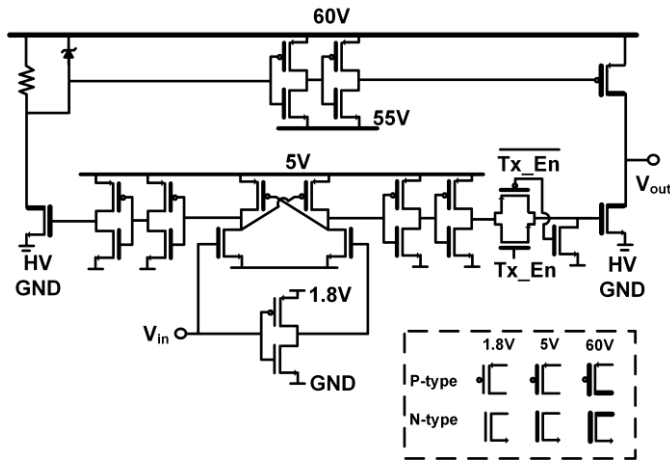Fig. 2. Detailed block diagram of the Tx-beamformer.

Fig. 3. Schematic diagram of the proposed 60 V pulser.

discussion is presented in Section VI with comparison with the recent state-of-art before concluding in Section VII.

II. SYSTEM ARCHITECTURE

In a conventional ICE catheter system, each of the piezo-array elements at the catheter tip is connected to the AFE system of the mainframe using a long conducting line. To reduce the number of wires, the proposed system uses an ASIC at the catheter tip to implement the Tx beamformer and Rx TDM circuits in a single chip. Fig. 1 shows the simplified block diagram of the proposed ICE catheter system. Each 1D piezo-transducer array element is driven by a HV pulser, which can generate up to 60 V unipolar pulse, appropriately delayed based on the beamforming profile by the integrated beamformer. A Tx/Rx switch is located between pulser and Rx circuits to protect low voltage (LV) devices during Tx operation. Variable gain low noise amplifier (LNA) compensates for the attenuation of reflected echo signal by adjusting its gain to implement time gain compensation (TGC).

Eight sets of 8:1 TDM circuitry reduce the number of output signals from 64 to 8, and the high frequency (HF) buffers drive the TDM signals via Ethernet cables to the backend system.

The ADC in the backend system samples the corresponding channel at the right time. A key feature of the TDM in this system is the clock synchronization between the external ADC and multiplexer in the ASIC, details of which will be described in the next section. In this system, 64 channels of piezo-array elements are used to interface with the ASIC in this proof-of-concept implementation. This array can be directly mounted on top of the front-end ASIC using flip-chip bonding or PZT-on-CMOS integration for future implementation [3], [12]. The proposed ASIC is also designed to be compatible with capacitive micromachined ultrasound transducer (CMUT)-on-CMOS application, where the array is fabricated directly over the CMOS wafer using a low temperature process [21].

The catheter cable consists of a mixture of μ-coax cables (200 MHz of clock, data, TDM output signals) and single wires to deliver power lines, biases and control signals. After the catheter cable, the TDM signals are amplified via catheter handle to be sent across the long Ethernet cables to ADCs in backend system, where DDD is performed in the FPGA for advanced imaging processing in the digital domain [7].

The backend system consists of a custom ADC board to support 8 TDM signals, FPGA board, and power supply module. It also employs filters, AC-DC converters, DC-DC converters, and a PCI express card, which delivers data from the FPGA to a personal computer via optical fiber.

III. TX BEAMFORMER AND PULSER DESIGN

A. Design and Operation of Tx Beamformer

The proposed Tx beamformer uses a single LVDS data line to load the beamforming profile for 64 channels. It creates a maximum delay of 10.235 μs with a resolution of 5 ns, using an 11-bit global counter. This maximum delay enables steering the ultrasound beam over the desired ±45° field of view. The beamformer is designed to generate different pulse-width for each channel to control the Tx bandwidth and enable pulse-width apodization, which improves ultrasound image quality by suppressing the side lobe effects [22]. Also, it can generate multiple pulses up to 8, for narrow band higher SNR operation in pulsed Doppler mode. It also can change the pulse repetition
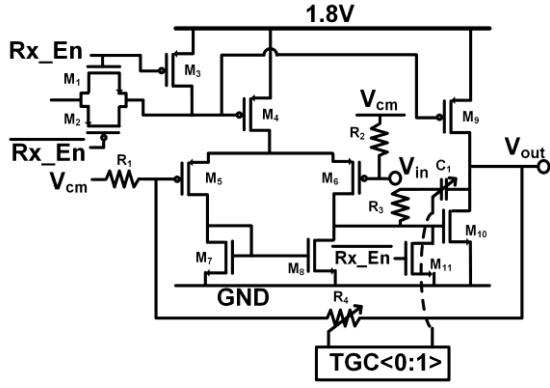
Fig. 4. Schematics of variable gain LNA.

(a)

(b)

Fig. 5. (a) Simplified block diagram of TDM block for 8 channels, and (b) TDM sampling clock diagram.

frequency during Doppler mode operation.

Fig. 2 shows the detailed block diagram of Tx beamformer. In global control logic block, there is an 11-bit global counter that consists of 6-bit course counter (CC) and 5-bit mod counter (MC). During the data loading sequence, the initial value of 6-bit CC is fixed to 111111_2, and the counter starts counting down to 000000_2 to find the coarse delay of each channel, while the 5-bit MC can be programmed to set the exact start time, width of a pulse, and number of pulses for each channel. Each of 64 channels has 16-bit serial-in parallel-out (SIPO) shift register that stores delay and pulse width information, respectively. Top 6-bit shift register is used to check proper data loading by comparing the value with 111111_2. Once the data is loaded properly, the latch signal locks the shift registers and the counters start to count for pulse generation. A 2-bit shift register is used for Rx gain control configuration, and the last 3 bits of the shift register store the number of pulses for Doppler operation. Each channel has a 3-bit subtractor, which is used to keep track of how many pulses are fired during each transmitting cycle. Each channel has a 19-bit comparator that can calculate the exact beamforming profile to deliver LV pulses to the input of pulser.

To program the delay profile for all of the 64 channels, each programming cycle requires a 1040-bit data packet (64×16+2 +3+5+6), which corresponds to 5.2 μs. Before programming the Tx beamformer, all shift registers are reset to set initial values, following which the data packet is generated and sent from the FPGA in the backend system through the high speed Ethernet cables.

B. Design and Operation of HV Pulser

Ultrasound pulse generator, aka pulser, is one of the key building blocks of any ultrasound imaging system, which drives ultrasound transducers, such as piezoelectric transducer or CMUT with HV output swing to create a pressure pulse. Recent literature shows several pulse-level shifting techniques to overcome limited supply voltage such as voltage doubler or multi-level pulse generator in ultrasound application [23], [24]. However, these approaches require multiple control signals and occupy significant area, such that integrating them in the ICE catheter becomes challenging.

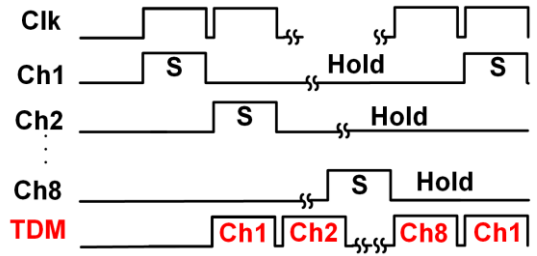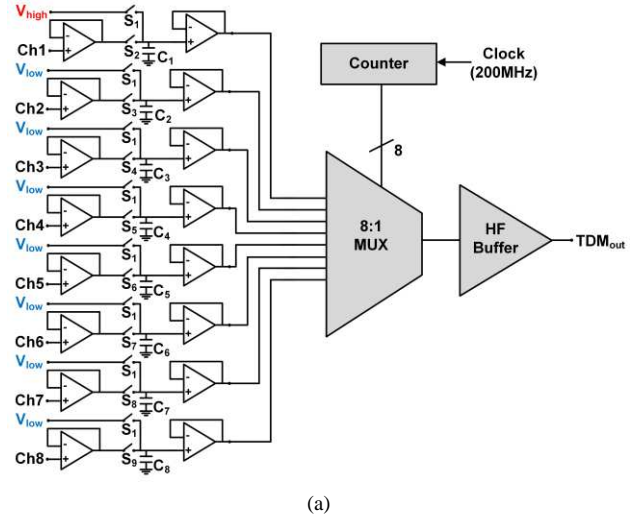In this system, a digital pulser is implemented using 60 V

double-diffused metal oxide semiconductor (DMOS) transistors, as shown in Fig. 3. The input of pulser is generated from Tx beamformer with 1.8 V supply. The pulser shifts this signal to 5 V_{pp} to have enough input swing for DMOS transistors, and finally drives the output node with 60 V pulse. It is crucial to ensure that all devices in the circuit are operated in their safe operating conditions throughout the pulse cycle, considering the fact that in this process, the drain-source junction breakdown and gate-oxide breakdown voltages are 60 V and 5 V, respectively. Considering that P-type DMOS transistor occupies larger area compared to the N-type DMOS transistor due to additional guard rings, a 1.3 kΩ resistor is used in level-shifter stage with protection Zener diode which has 5 V of breakdown voltage. This level shifter is designed to limit the peak current to 5 mA from 60 V supply by adding an external 55 V supply and 5 V buffer chain, avoiding voltage drop across 6.7 mm on-chip power routing. The pulser is designed to drive 15 pF of capacitive load at 7 MHz with 60 V pulses, which is the equivalent capacitance of comparably large sized piezoelectric 1D ICE array.

IV. Rx Circuitry Design For Cable Reduction

Simplified schematic of the AFE is shown in Fig. 1. 64 channels of Rx circuitry consists of Tx/Rx switch, variable gain LNA, buffer and TDM circuitry. The LNA design assumes an input echo signal dynamic range of 76 dB, and the gain of Rx

circuitry is set to compensate the attenuation by 4 stages (15 dB, 21 dB, 27 dB, and 32 dB) to meet the dynamic range of ADC in the backend system. During the Tx mode, Tx/Rx switch protects LV circuits from HV pulses. Variable gain LNA amplifies the echo signal based on the traveling depth for compensation, the buffer drives the amplified signal to TDM circuitry, and finally TDM circuitry samples and combines the output signals with 8:1 ratio to the backend system. The key blocks are described in detail below.

A. Design and Operation of Variable Gain LNA

Rx front-end topology in ultrasound system usually depends on the electrical impedance of ultrasound transducer type. The transimpedance amplifier (TIA) is a commonly used topology in CMUT application because the equivalent electrical model of CMUT has comparably high impedance [12]. For implementing the AFE for piezoelectric array, LNA structure is preferred because of relatively low impedance of piezoelectric elements [25]. Considering the area efficiency, and the fact that in this process capacitors occupy larger area than resistors, and for minimizing the shift of pulse-echo response to lower-frequencies, a resistive feedback LNA structure was selected for this system [26]. Also, instead of implementing LNA and time gain control (TGC) circuit separately, we adopted a variable gain LNA structure.

Fig. 4 shows the schematic diagram of variable gain LNA structure. The gain is controlled by 2-bit TGC control bits through data line, which is generated by the external FPGA. The Miller compensation capacitor, C_1, is also controlled by TGC signal to push the second pole of this 2-stage op-amp well beyond the closed-loop bandwidth to keep phase margin above 60° in every gain stage of LNA. Rx_EN signal and switch transistors (M_1, M_2, and M_{11}) are required for power saving mode during Tx data loading period.

B. Design and Operation of TDM Circuitry

The TDM technique has been frequently used in communication systems to reduce the number of outputs [27], [28]. This approach allows multiple channels to share the same cable by assigning a corresponding time slot to each channel. Analog TDM requires a relatively simple design and less power because it needs an analog multiplexer and digital counting logic in addition to sample and hold circuits, which is suitable for compact ICE application. Also in this proposed system, by using DDD technique, the ADC can sample TDM output signals using the same frequency as the TDM circuitry in the ASIC. This results in less data processing to increase efficiency in the backend system [7].

The Tx target center frequency of this system is around 7 MHz, and the 3 dB fractional bandwidth is assumed as 80%, especially in the case of CMUT array, which usually has broader bandwidth than a piezoelectric array. This bandwidth requires a sampling rate more than 20 MS/s considering the Nyquist requirement. In this system, the clock frequency is chosen as 200 MHz, resulting in 25 MS/s for each channel of 8:1 TDM circuitry. To minimize the TDM cross-talk level due to inter symbol interference, the HF buffer is designed to have more than 400 MHz bandwidth. The TDM circuitry consists of 8 sets of TDM blocks, and each TDM block consists of 8 channels of sample and hold switches, link training switches,
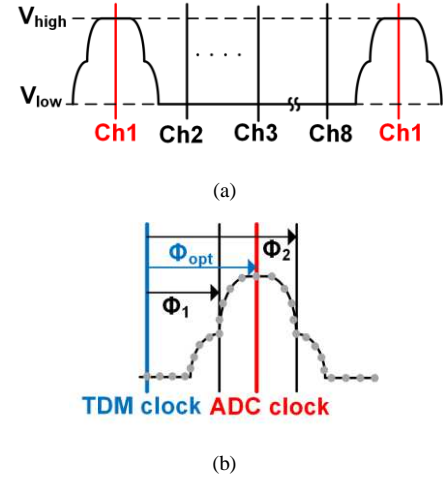

(a)

(b)

Fig. 6. Link training waveform of (a) channel number synchronization, and (b) phase synchronization.

analog 8:1 multiplexer, and high frequency buffer, as shown in Fig. 5(a). The TDM block is designed and placed symmetrically using H-grid clock distribution to reduce the mismatch. The counter logic generates sampling clocks and the analog multiplexer selects signals for corresponding channel after 1 period of clock, which keeps track of which channel is to be connected, as shown in Fig. 5(b).

A critical part of the DDD is the clock synchronization between the TDM analog multiplexer in the ASIC and the ADC in the backend system with the same frequency. For this reason, the system requires two training sequences before TDM block starts working. One is channel number synchronization, and another is clock phase synchronization. These training sequences are called "link training" to ensure that the samples are correctly digitized in the backend system. During the link training process, first channel is connected to a fixed voltage level, V_{high}, while other channels are connected to another lower fixed voltage, V_{low}, by adding another switch in parallel with the sample and hold switch for each channel, as shown in Fig. 5(a). During this operation, S_1 is connected and all the other switches from S_2 to S_9 are open that the corresponding timing of channel 1 can be detected during demultiplexing in the backend system. By performing this step, the timing of the first channel of each TDM block can be ensured so that the order of channel timing is determined, as shown in Fig. 6(a).

The clock phase synchronization is used to ensure that the ADC and TDM multiplexer clocks are correctly phase synchronized to compensate for the propagation delays in the cabling. This is important as one needs to make sure that the ADC takes the samples when the signal through the interconnection has stabilized rather than during the switching transients. The TDM clock phase can be adjusted using a phase-locked loop (PLL) in the FPGA to determine the optimum phase shift, as shown in Fig. 6(b). The phase of TDM clock is changed with 78 ps steps until channel 1's half maximum points are found, such as Φ_1 and Φ_2. These two points show when the switching transients are occurring, so optimal phase shift is estimated to be in the middle of these two points, which is marked as Φ_{opt}. The HF buffer is designed using current feedback source degenerated push-pull type buffers with ~400
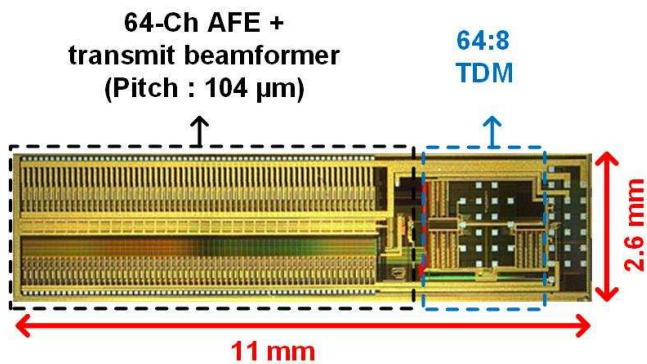
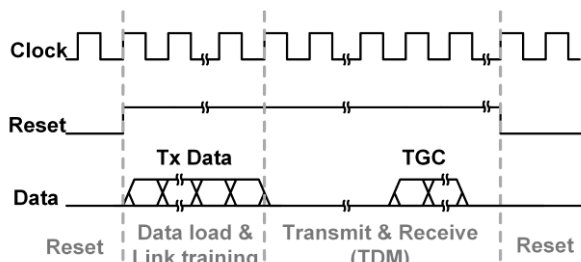Fig. 7. Microphotograph of the 64-channel ICE ASIC, implemented in a 60 V, 0.18-μm HV-BCD CMOS process.

Fig. 8. Timing diagram of the proposed system.
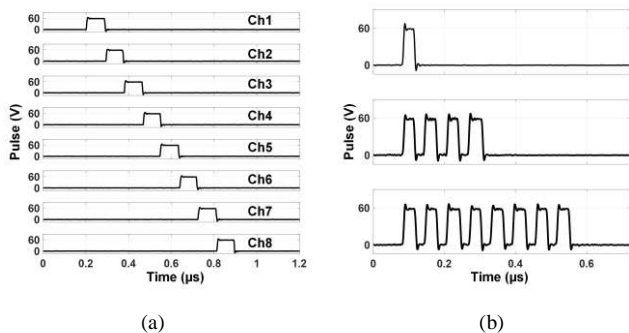

(a)　　　　　　　　　　　　(b)

Fig. 9. (a) Measured pulser output from adjacent 8 channels. (b) Multiple consecutive pulse generation for Doppler imaging.

MHz bandwidth, tuned for 75 Ω cable termination [29].

V. Experimental Results

The ASIC is fabricated in a 0.18-μm 60 V power management 4M1P HV-BCD CMOS process. It consists of 64 channel AFE (pulser, Tx/Rx switch, LNA, and buffer), Tx beamformer, and symmetrically designed TDM, which occupies 2.6×11 mm^2, as shown in Fig. 7. The pads for supplies, control signals and TDM outputs are located on the right side of ASIC, which are designed to be compatible with flip-chip interconnect based catheter cable connection. The chip consumes 401 mW of power on average for B-mode imaging using phased-array beamforming, 42% of which is used for TDM and drivers. Fig. 8 shows the timing diagram of the proposed system. The ASIC requires clock, reset, and data inputs. Once the Tx data is loaded properly after link training from the TDM side, the Tx beamformer triggers pulsers to fire
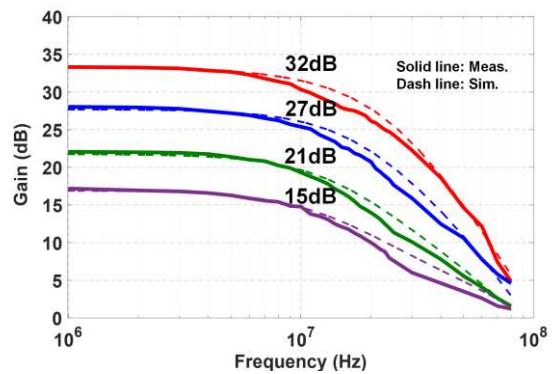

Fig. 10. Measured and simulated frequency response of variable gain LNA with different 4 gains.
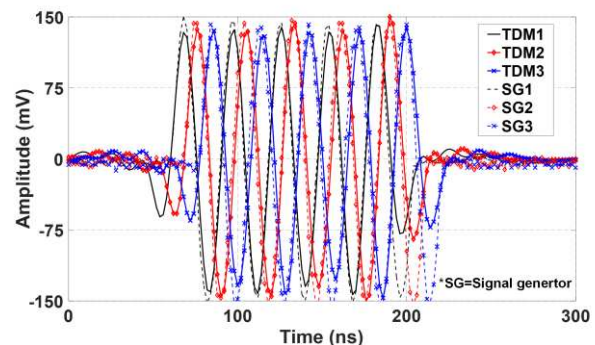

Fig. 11. Comparison between the signal generator and TDM output signals after digital signal processing.

HV pulses based on the beamforming profile, and Rx circuits are receiving at the same time. TGC signal can be loaded through data line to control the Rx gain at specific times. To eliminate the dead time during the Tx data loading, another set of Tx beamforming data can be loaded during receive period after Tx firing is done. After receiving the echo signals, reset signal returns the entire system back to the initial state. The link training always needs to be done before loading beamforming data, that compensates any change of the delay of the cable due to temperature change or bending.

A. Electrical Characterization for Tx Circuitry

The ASIC was wire-bonded to a custom printed circuit board (PCB) to probe the output of the pulsers with the effective loading of ~15 pF, which is the equivalent capacitance of 1D piezo-array with 80 membranes (each membrane occupies 46×46 μm^2). The FPGA generates beamforming profile where each channel has the pulse width of 80 ns, and is delayed by 80 ns relative to the previous channel. Fig. 9(a) shows the measured pulse output from channel 1 to channel 8. The pulsers successfully generate 60 V pulses with rise and fall time of 6 ns, which is suitable for driving a center frequency of 7 MHz pulse. Fig. 9(b) shows that the proposed Tx beamformer can generate up to 8 pulses for Doppler operation.

B. Electrical Characterization for LNA and Rx TDM

Fig. 10 compares the measured and simulated frequency response of variable gain LNA with different gain settings, which shows 15 dB, 21 dB, 27 dB, and 32 dB at center
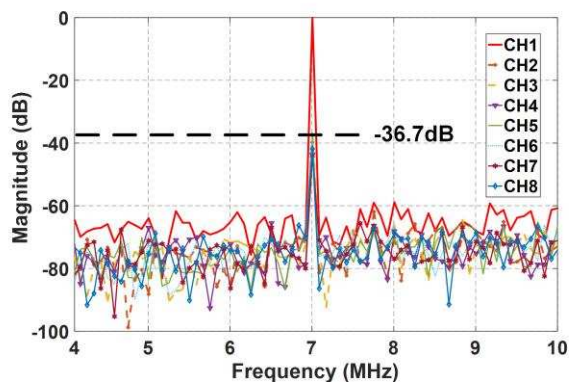
Fig. 12. Crosstalk measurement of 8 channels of TDM circuitry.

frequency of 7 MHz with 3 dB bandwidth of 11 MHz. The measured input referred noise at 7 MHz for different gain levels show less than 4.1 nV/√Hz on average, close to the design target value of 5 nV/√Hz, which is calculated from the assumed LNA input dynamic range.

The proposed Rx TDM was separately characterized with a test chip to evaluate the performance of TDM circuitry. The test chip included a subset of blocks in the main ASIC, the ones needed to evaluate a block of 8 channels of TDM, as shown in Fig. 5(a), with an additional control block for link training. A custom PCB was designed to connect 8 input signals from external signal generators, and TDM output signal was connected to one of the backend TDM input terminals. The ADC samples the corresponding channel signals, then the FPGA performs DDD and further digital processing for interpolation, decimation, phase correction, and filtering to recover the original input data [7]. To test this signal chain, channel 1, 2, and 3 were connected to signal generators, which generated 7 MHz sine waves with 50 ns delay. Fig. 11 shows the comparison between digitized signal generator output and recovered TDM output signals after signal processing, which shows good agreement. The mismatch between the TDM outputs and signal generator outputs in the first and the last bursts is the result of band pass filtering. The mismatch between the channels is measured to be less than 0.6 dB in amplitude.

The level of crosstalk was also characterized in the TDM test chip. A 7 MHz sine wave was applied to channel 1, while inputs to other channels were grounded. The TDM signal was recovered for all 8 channels and analyzed using fast Fourier transform (FFT). Fig. 12 shows that the maximum crosstalk level is -36.7 dB when compared to channel 1, which is suitable for ICE application [9]. It is noteworthy that this measurement of the crosstalk is between the signals of the same TDM block over the same cable as a result of the multiplexing scheme, which represent the worst case scenario. The crosstalk level between separate TDM blocks on different cables was measured to be below -60 dB.

C. Ultrasound Imaging with the Entire System

The proof-of-concept imaging experiments were performed by connecting the ASIC wire-bonded on a PCB, to a 64 channel piezoelectric transducer array at the tip of an ICE catheter using cables as shown in Fig. 13. The ASIC PCB is directly

Fig. 13. Ultrasound imaging measurement setup with piezo-array immersed in the water facing standard phantom.

(a)

(b)

Fig. 14. (a) B-mode image of 10 nylon wires, and (b) 2 cysts image in a standard phantom.

connected to catheter handle, which the TDM signals are amplified prior to passing through to the ADCs in the backend system via 3 m of Ethernet (Cat7A) cable to allow the system to be placed away from the MRI bore or the ultrasound mainframe in practice. In the future, the piezoelectric array will be either flip-chip bonded to the ASIC or the CMUT-on-CMOS technique will be applied for compact assembly, both of which are expected to reduce the parasitics and improve the resulting image.

TABLE I
BENCHMARKING OF THE REDUCED-WIRE ULTRASOUND ASIC SYSTEMS

Parameter	This work	[12]	[13]	[25]	[32]	[33]
Single chip integrated Tx-Rx system	Yes	No	No	No	No	No
Shared Tx-Rx array aperture with pitch match	Yes	No	N/A	No	No	No
Rx wire reduction	TDM	ADC + S/H analog	ADC + FIFO	S/H analog	Analog filter	S/H + Digital
Tx Wire reduction	Yes	No	No	No	No	No
Rx raw data accessibility	Yes	No	Yes	No	No	No
Center frequency (MHz)	7	5	5	5	40	3
Tx delay min (ns)/max(μs)	5/10.235	-	-	-	-	-
Die size (mm^2)	2.6×11	2.5×4.8	2.93×3.2	6.1×6.1	1.2×0.3	4.5×4.3
Power/ Rx channel (mW)	6.26	0.91	17.5	0.27	4.62	17.81
Active area/ channel (mm^2)	0.27	0.026	0.088	0.026	0.045	0.303
Power/ Rx active area (mW/ mm^2)	23.18	35	198.96	10.38	102.66	58.77
# of channels	64Tx/64Rx	144Rx	16Rx	1024Rx	8Rx	64Rx
# of wires / Rx channels	8/64	4/144	1/16	96/1024	1/8	1/64
# of wires/ Tx channels	0.0625 (4/64)	1	1	1	1	1
Tx amplitude	60V	-	-	-	-	-
Transducer	1D PZT/CMUT	2D PZT	2D CMUT	2D PZT	Annular CMUT	2D CMUT
Process	0.18 μm HV	0.18 μm	28 nm	0.18 μm	0.35 μm	0.13 μm

The piezoelectric transducer array is immersed in a water tank, facing a multi-purpose standardized tissue mimicking imaging phantom (N-365, Kyoto Kagaku, Japan). To form a cross-sectional B-scan image of the phantom, in Tx mode, the Tx beamformer is programmed to generate 123 focused and steered beams using suitable delay schemes to scan the ±45° sector image. In Rx mode, the echo signals captured by the ASIC front-end are transferred to the back-end system where the signals are post-processed and dynamic Rx beamforming is performed to reconstruct B-scan images [6]. Two different imaging targets inside the imaging phantom were used to test the performance of the system. First, a set of 10 nylon wire targets of 100 μm diameter were imaged. Fig. 14(a) shows the image of the 10 wire target, in which each wire is located 1 cm apart from others up to a depth ~5 cm, as shown in the diagram on the right. The second target was 2 gray scale cyst phantoms at a depth of 3 cm, as shown in Fig. 14(b). Both images are presented with a dynamic range (DR) of 40 dB. The contrast-to-noise-ratio (CNR) was also calculated for the cyst target to quantify the system performance. The CNR is defined as [30],

$$CNR = \frac{|\mu_C - \mu_B|}{\sqrt{\sigma_C^2 + \sigma_B^2}}, \qquad (1)$$

where μ_C and μ_B are the mean intensities of the regions inside the cyst and outside the cyst, respectively, and σ_C^2 and σ_B^2 are the corresponding variances. The CNR values for T_1 and T_2 cyst (Fig. 14(b)) were calculated as 1.55 and 1.23 with a relative contrast difference of 2 dB, which is in reasonable agreement with specs of the phantom [31].

VI. DISCUSSION

Overall, these results demonstrate the full functionality of the ASIC and backend system with a performance suitable for the targeted ICE application. Since the size of the pulser often limits the minimum size of Tx/Rx elements on the ASIC, the reduced capacitive loading with smaller 2D array elements will help to pitch-match the ASIC with a 2D ICE array implementation.

Table I benchmarks this work against the state-of-the-art ultrasound ASIC designs, where detailed information is available. As seen in the overall system comparison, this ASIC is the only system that integrates Tx/Rx without compromising imaging aperture and access to raw Rx data. This ASIC generates Tx delays from 5 ns to 10.235 μs to steer the ultrasound beam over the ±45° field of view, and has effectively 0 to 11 MHz pulse-echo system bandwidth. The die size is determined by the ICE application to fit in a 9 F catheter as shown in the ASIC micrograph (Fig. 7). Note that the power consumption per active chip area compares favorably with most other Rx cable reduction systems. AFE of each channel occupies 0.27 mm^2, which is designed to match the pitch for future CMUT-on-CMOS design (element size: 2.6×0.104 mm^2). Number of Rx cables is reduced by 8:1 TDM. Note that in case of a 2D array when TDM is used in conjunction with 3x3 subarray beamforming with switched-capacitor delay, this ratio can increase to 72:1.

The number of wires per Tx channel is reported as 4/64, including the data and clock wires, which is a significant advantage of this particular ASIC. It should be noted that this figure will further improve by increasing number of Tx channels for a system with larger number of elements as the required number of wires will remain the same. The size and power can be further optimized as the proposed ASIC is the first prototype for proof-of-concept for catheter-based ICE application, however even with non-ideal PCB based interconnect and partly operational PZT array, overall this novel system provides high dynamic range images of tissue mimicking phantoms.

VII. CONCLUSIONS

This work integrates both Tx beamformer and TDM based Rx in a single chip to reduce the number of interconnect wires

in a 64 element 2D imaging ICE catheter. The Tx beamformer is capable of steering and focusing the Tx beams in a wide angular range and can be programmed in every firing using a single data line. The crosstalk levels and overall SNR of the resulting images indicate suitable performance for 2D imaging with 1D ICE arrays. The number of wires has been reduced from more than 64 down to 22 for this application, while maintaining full access to the raw data from each channel. More significant reduction is expected for 2D array-based systems with a larger number of elements. The reduction in cable count will not only create the potential for operation under MRI and reduce catheter cost, but it will also increase the mechanical flexibility and possibility of additional functionality in ICE catheters.

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