This is a repository copy of *On-chip hybrid superconducting-semiconducting quantum circuit*.

White Rose Research Online URL for this paper:
http://eprints.whiterose.ac.uk/137721/

Version: Accepted Version

Article:
Delfanazari, K., Puddy, R.K., Ma, P. et al. (8 more authors) (2018) On-chip hybrid superconducting-semiconducting quantum circuit. IEEE Transactions on Applied Superconductivity, 28 (4). 1100304. ISSN 1051-8223

https://doi.org/10.1109/TASC.2018.2812817

© 2018 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other users, including reprinting/ republishing this material for advertising or promotional purposes, creating new collective works for resale or redistribution to servers or lists, or reuse of any copyrighted components of this work in other works. Reproduced in accordance with the publisher's self-archiving policy.

Reuse
Items deposited in White Rose Research Online are protected by copyright, with all rights reserved unless indicated otherwise. They may be downloaded and/or printed for private study, or other acts as permitted by national copyright laws. The publisher or other rights holders may allow further reproduction and re-use of the full text version. This is indicated by the licence information on the White Rose Research Online record for the item.

Takedown
If you consider content in White Rose Research Online to be in breach of UK law, please notify us by emailing eprints@whiterose.ac.uk including the URL of the record and the reason for the withdrawal request.

eprints@whiterose.ac.uk
https://eprints.whiterose.ac.uk/

On-chip hybrid Superconducting-Semiconducting Circuit for Scalable Quantum Computing

K. Delfanazari, Member, IEEE, R. K. Puddy, P. Ma, T. Yi, M. Cao, C. Richardson, I. Farrer, D. A. Ritchie, H. J. Joyce, M. J. Kelly, Senior Member, IEEE, and C. G. Smith

Abstract— In this paper, we experimentally demonstrate a hybrid superconducting-semiconducting (S-Sm) circuit consisting of eight planar and ballistic Nb-$In_{0.75}Ga_{0.25}As$-Nb Josephson junctions. E-beam lithography was used to fabricate the Josephson junctions on an InGaAs chip. In contrast to our previous studies on long junctions that were fabricated by photolithography, in this study, we observe the induced superconductivity in an $In_{0.75}Ga_{0.25}As$ quantum well at higher temperatures, between T= 0.3 and 1.4 K (^{3}He cryostat temperature range). The induced superconducting gap of Δ_{ind}= 0.65 meV was measured at lowest base temperature T= 300 mK. The effect of temperature and magnetic fields B on the induced superconductivity are presented. Our results suggest that our $In_{0.75}Ga_{0.25}As$ heterojunctions is a promising scalable material system for quantum processing and computing applications.

Index Terms—Josephson junctions, quantum computing, hybrid superconductor-semiconductor junction, on-chip quantum circuits.

I. Introduction

THE hybrid superconductor-semiconductor-superconductor (S-Sm-S) structures have been proposed to be the building blocks of the next generation of quantum computers, after the purported detection of exotic Majorana particles with zero electrical charges at the interface of S-Sm junctions [1-3]. However, there still is a fundamental technological problem in the (i) fabrication of highly transparent interfaces between superconductors and semiconductors and (ii) scaling the number of junctions up in a single chip to realize a quantum device applicable for quantum technology [4-7]. In this regard, we have recently demonstrated hybrid Josephson junctions with highly transparent interfaces between the superconducting Niobium (Nb) and semiconducting $In_{0.75}Ga_{0.25}As$ two-dimensional electron gas (2DEG) contacts. The circuit and Josephson junctions were fabricated by photolithography [4,5]. The devices were measured in a dilution fridge and the induced superconductivity was observed at temperatures T ≤ 400 mK. In this paper, we report on a different approach to fabricate the hybrid Nb-$In_{0.75}Ga_{0.25}As$-Nb Josephson junctions. E-beam and photo-lithography and wet-etching were used to fabricate the hybrid quantum circuits. To form the Josephson junctions, two irregular pentagons of length L= 550 nm (at shortest path) and width w= 3 μm were patterned facing each other. We found that it is possible to observe the induced superconductivity in $In_{0.75}Ga_{0.25}As$ quantum well at higher temperature ranges, between T = 3 mK and 1 K.

Manuscript received September 19, 2017. This work was supported in part by EPSRC Grant Nos. EP/M009505/1 and EP/J017671/1.

K. Delfanazari, R. K. Puddy, P. Ma, T. Yi, M. Cao, D. A. Ritchie, M. J. Kelly, and C. G. Smith are with the Department of Physics, Cavendish Laboratory, University of Cambridge, Cambridge CB3 0HE, UK. (corresponding author; K. Delfanazari, e-mail: kd398@cam.ac.uk).

K. Delfanazari, H. J. Joyce and M. J. Kelly are with the Centre for Advanced Photonics and Electronics, Engineering Department, University of Cambridge, Cambridge CB3 0FA, UK.

C. Richardson is with Department of Materials Science and Metallurgy, University of Cambridge, Cambridge, CB3 0FS, UK.

I. Farrer is with the Department of Electronics and Electrical Engineering, University of Sheffield, Sheffield S1 3JD, UK.

II. Hybrid S-Sm-S Josephson junction Fabrication

A. Semiconducting Heterojunction Fabrication

Fig. 1: The schematic view of the $In_{0.75}Ga_{0.25}As/In_{0.75}Al_{0.25}As/GaAs$ heterostructure. The $In_{0.75}Ga_{0.25}As$ quantum well 2DEG with 30 nm thickness is formed 120 nm below the wafer surface. Niobium (Nb) was used as the superconducting contacts (shown in black) to form a hybrid and ballistic Nb–$In_{0.75}Ga_{0.25}As$ 2DEG–Nb Josephson junction.

The $In_{0.75}Ga_{0.25}As/In_{0.75}Al_{0.25}As/GaAs$ quantum wells used in this study were grown by molecular beam epitaxy (MBE)

mount on 500 μm semi-insulating (001) indium free GaAs substrates [8]. The layer thickness and the sequence of distinct layers are shown in Fig. 1. Arsenic dimers (As_2) are used to reduce antisite defects at the low growth temperatures. To improve the electron mobility in this structure, three growth parameters, substrate temperature (T_s), arsenic over pressure (P_{As2}) and Si modulation doping level (N_{Si}) were set. At the start of the graded buffer layer growth, T_s was adjusted. Following oxide elimination, the GaAs/AlAs/GaAs (50/75/250 nm) buffer layer was grown at T= 580˚C.

Before growing the step-graded buffer (SGB) layer (a 1300 nm InAlAs), the substrate temperature was ramped down for 20 min. The SGB layer then was grown at starting substrate temperatures of T= 416, 390, 360, 341, 331 and 337˚C [8].

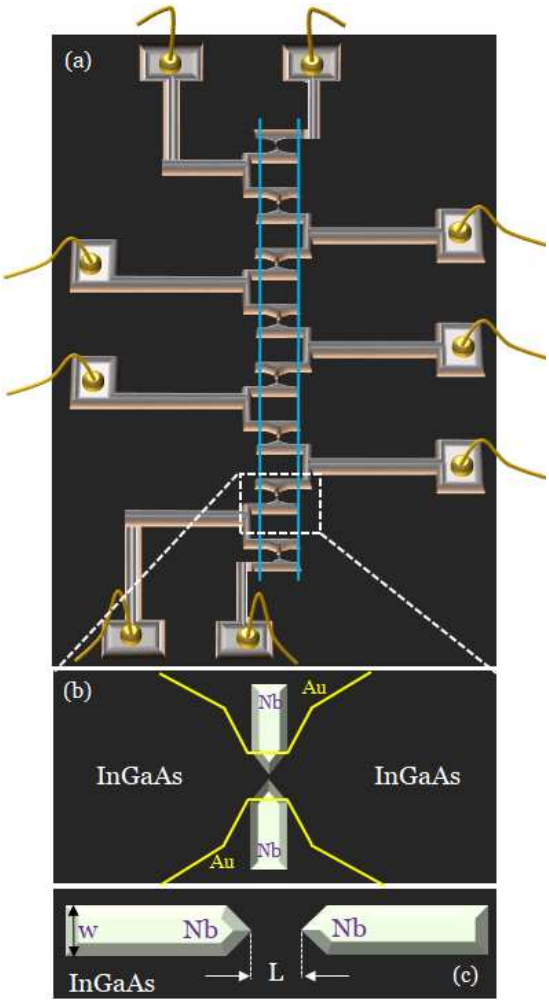

Fig. 2: The on-chip hybrid superconducting-semiconducting quantum circuit: (a) A schematic view of the hybrid quantum circuit consisting of eight symmetric and planar Nb-$In_{0.75}Ga_{0.25}As$-Nb Josephson junction on a chip. The superconducting parts are Niobium (Nb). The mesa (active area) is shown by blue lines. The area shown in yellow is covered by gold (Au) for electrical measurements. (b) An enlargement of the area indicated by the square showing the junction formation on the active region. (c) The detail of one planar Nb-$In_{0.75}Ga_{0.25}As$-Nb Josephson junction. The gap between two Nb electrodes has a length L= 550 nm at the shortest path.

Since the substrate becomes more absorbing during growth, the quantum wells (a 30 nm thick $In_{0.75}Ga_{0.25}As$ 2DEG) were grown at slightly higher substrate temperatures. To change the indium composition in the structure, at the start of each layer in the SGB sequence, the temperature of aluminum cell was reduced while the temperature of indium cell was increased [8].

Throughout the structure, the nominal growth rate was kept uniform. Before growing the 75% InAlAs buffer, growth was interrupted (to stabilise the indium cell). To avoid impurity accumulation, because of growth interruption, a further 250 nm InAlAs layer was grown. This separates the impurities from the conduction channel. The 2DEG quantum well was covered by a 60 nm $In_{0.75}Al_{0.25}As$ spacer.

To ensure conductance in the dark, the wafers were modulation doped (15 nm of n-type $In_{0.75}Al_{0.25}As$). The modulation doping concentration was controlled by altering the silicon cell temperature. Finally, a 40 nm $In_{0.75}Al_{0.25}As$ layer was grown followed by a 2 nm InGaAs cap layer.

Shubnikov–de Haas oscillations and Hall effect measurements were performed at 1.5 K to obtain electron density $n_s=2.24\times10^{11}$ (cm^{-2}) and mobility $\mu_e=2.5\times10^5$ (cm^2/Vs) in the dark and $n_s=2.28\times10^{11}$ (cm^{-2}) and $\mu_e=2.58\times10^5$ (cm^2/Vs) after illumination.

B. On-chip Hybrid Circuits Fabrication

Eight planar and symmetric Josephson junctions were patterned and fabricated on a single $In_{0.75}Ga_{0.25}As/In_{0.75}Al_{0.25}As/GaAs$ chip by wet etching and e-beam processing. In this study we report the experimental results of one junction. Results for other devices, including the statistics and quantum yield will be discussed elsewhere.

Figure 2(a) shows the schematic view of the on-chip hybrid superconductor-semiconductor circuit consisting of eight symmetric and planar Nb-$In_{0.75}Ga_{0.25}As$-Nb Josephson junctions.

To make the hybrid junctions, first a mesa structure (the area between two blue lines shown in Fig. 2) was fabricated by wet-etch, to make the active region. The acid solution was made of H_2SO_4: H_2O_2: H_2O to get an etch depth of □150 nm. H_2O_2 was used to oxidise the exposed InGaAs surface and H_2SO_4 was used to dissolve the oxide (InGaAs cannot be etched solely in H_2O_2 or H_2SO_4 solutions).

The DEKTAK surface profiler was used to measure the mesa depth of □150 nm. AuGeNi alloy was then used to make ohmic contacts which were placed 100 μm away from the junctions to prevent the influence of the normal electrons on the Nb- $In_{0.75}Ga_{0.25}As$ quantum well interfaces.

Nb superconducting contacts to 2DEG were made by creation of a □140 nm deep trench on the active region by wet-etch. A □130 nm thick Nb was deposited by DC magnetron sputtering in Ar plasma to form Nb-$In_{0.75}Ga_{0.25}As$-Nb Josephson junctions. The junction has a width of w= 3 μm and length of L= 550 nm (at the shortest path).

The schematic view of one junction consisting of two irregular pentagonal shape superconducting leads is shown in

Fig. 2b. At the last stage, 10/50 nm thick Ti/Au layers was evaporated on top of the junctions for electrical measurement purposes. Figure 2c is the computer aided design (CAD) design, showing that Nb electrodes on each side of the junction were covered by thin layers of Ti/Au. The sample was diced and glued by using the GE varnish or silver epoxy onto a standard leaded chip carrier (LCC). To bond the ohmic contacts to the carrier pads, the gold-ball thermosonic bonder with a gold thread was used.

III. Experimental Results

A. Electrical Circuit for Josephson Junction Measurements

The quantum transport measurements were carried out in a ^{3}He cryostat with a base temperature of 290 mK and magnetic field up to 10 T. The junctions were measured using a two-terminal lock-in method by superimposing a small ac- signal at the frequency 70 Hz and amplitude 5 μV (from a lock-in amplifier) to the junction dc- bias voltage (from National Instrument isolated analog output modules).

A current pre-amplifier with a gain of 10^6 A/V was used to convert the measured current into a voltage which was read by a Stanford SR830 DSP lock-in amplifier.

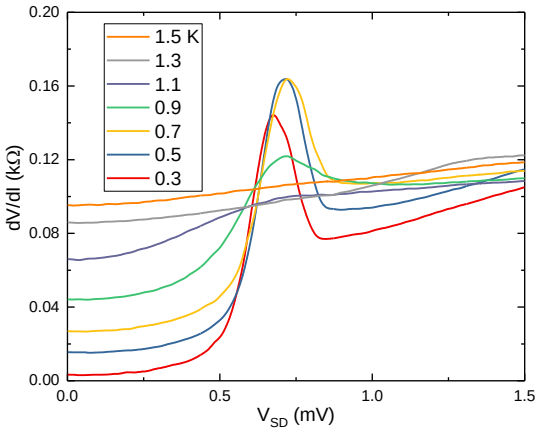

Fig. 3: The dV/dI curves versus source-drain voltage V_{SD} at temperatures between T =300 mK and 1.5 K. The induced superconducting gap in $In_{0.75}Ga_{0.25}As$ quantum well was observed for temperatures between T =300 mK and 900 mK.

To block the dc offset voltage of the pre-amplifier, and to eliminate the noise, a capacitor and a low path filter were used, respectively.

B. Effect of Temperature on Induced Superconductivity

The differential resistance dV/dI versus source-drain voltage V_{SD} bias curves of the Josephson junction at temperature ranges between T= 0.3 and 1.5 K are plotted in Fig. 3. At low enough temperatures, an excess current I_{exc} flows through the junctions because of electron- and hole-like quasiparticles correlations (Andreev reflections [9]) and reflection-less tunneling below the junction's T_c and for voltage biases within the Nb superconducting gap.

The dV/dI (V_{SD}) value is reduced in the gap region and a U-shape dip (a hard-induced superconducting gap was observed [4,5].

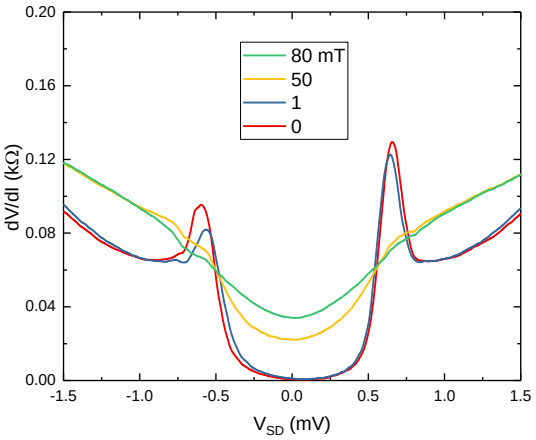

Fig. 4: The dV/dI plots versus V_{SD} at 0 < B (mT) < 80 and at base temperature T= 300 mK. The applied magnetic field B was perpendicular to the junction plane. The induced superconducting gap was suppressed as the applied field is increased.

The junction is ballistic and the distance (shortest path) between the two Nb electrodes is 550 nm which is an order of magnitude shorter than the corresponding elastic mean free path $\ell_e = e^{-1}\hbar\mu_e\sqrt{2\pi n_s} \approx 2$ μm. Here, n_s and μ_e are electron density and mobility of 2DEG, respectively.

In this experiment, the induced superconducting gap in $In_{0.75}Ga_{0.25}As$ quantum well was observed at magnetic field B= 0 and at temperatures between T= 300 mK and 900 mK. This indicates that, due to higher critical temperature of Nb based devices (~9 K) than commonly used Al based junctions [3], the induced superconductivity in Nb-$In_{0.75}Ga_{0.25}As$ devices can even be observed at temperatures above the dilution fridge temperature limits, by improving the fabrication techniques and/or by shortening the junction length to less than 0.5 μm.

The subharmonic gap structures, because of multiple Andreev reflections at the Nb-$In_{0.75}Ga_{0.25}As$ interfaces, observed in our previous studies [4,5] on long Nb-$In_{0.75}Ga_{0.25}As$-Nb Josephson junctions, were not observed in this experiment. The reason could be the difference in the design and fabrication processes of the junctions. Further studies are required to fully understand this.

C. Effect of Magnetic Field on Induced Superconductivity

The plot of the dV/dI as a function of applied perpendicular magnetic field B at T= 300 mK is shown in Fig. 4. Two symmetric peaks in the dV/dI vs. source-drain voltage V_{SD} bias

are observed at B= 0 T and T= 300 mK. From these peaks at B= 0 T and T= 300 mK, we estimate the induced gap Δ_{ind} =0.65 meV using the relation $\Delta = eV_{SD}$. The Δ_{ind} obtained here is about half of the value of high quality bulk Nb [10]. The separation of the peaks of induced superconducting gap, suppresses by increasing the magnetic field B, the position of the peaks shifts toward zero bias with further increasing the applied magnetic field B and the peaks disappear near B≈ 50 mT. However, a dip in the dV/dI curve (V-shape) is still seen at higher magnetic fields B up to 1 T. This peak is attributed to coherent multiple Andreev and normal reflections at the $In_{0.75}Ga_{0.25}As$-Nb interfaces.

D. Evolution of the Induced Superconductivity as a function of Temperature and Magnetic field

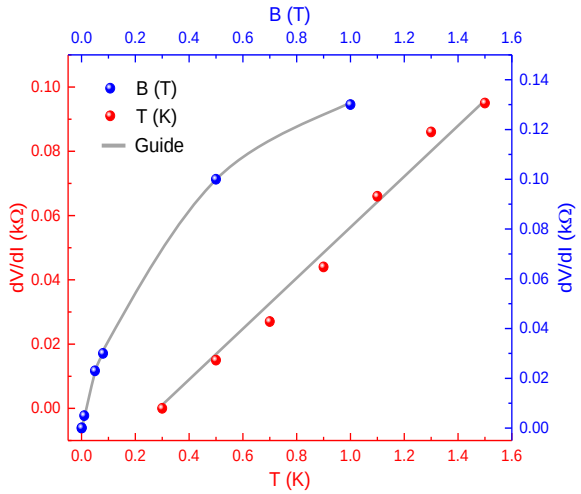

Fig. 5: Temperature and magnetic field B dependence of induced superconductivity. Red circles are dV/dI at temperatures between T= 300 mK and 1.5 K. Blue circles show dV/dI at magnetic field B between B= 0 and 1 T.

Figure 5 shows the dV/dI as a function of temperature (red graph/circles) and magnetic fields B (blue graph/circles). The gray lines are for guide. It can be inferred that the dV/dI increases with increasing the temperature and magnetic fields B. Nb is a type II superconductor with higher critical filed of H_{c2} (4.2) ~ 0.9 T [11,12]. The increase of the dV/dI stops when applied magnetic fields B is larger than H_{c2}.

IV. Conclusion

We have experimentally demonstrated a superconducting-semiconducting hybrid circuit consisting of eight planar and ballistic Nb- $In_{0.75}Ga_{0.25}As$-Nb Josephson junctions. The e-beam and photo-lithography processes were used to fabricate the hybrid circuit and scale up the number of Josephson junctions on the InGaAs chip. The temperature and magnetic field B dependencies of the induced superconducting gap were studied experimentally. In contrast to the long hybrid junctions made by photolithography process, here, we could observe the induced superconductivity in $In_{0.75}Ga_{0.25}As$ quantum wells at higher temperature ranges, between temperatures T= 0.3 and 1 K (^{3}He cryostat temperature range). Our results suggest that hybrid circuits based on Nb and $In_{0.75}Ga_{0.25}As$ are promising platform for scalable quantum processing and computing.

Acknowledgment

Authors acknowledge financial support from EPSRC grant numbers EP/M009505/1 and EP/J017671/1.

The data presented in this paper can be accessed at https://doi.org/10.17863/CAM.20606.

References

[1] V. Mourik et al., Signatures of Majorana fermions in hybrid superconductor-semiconductor nanowire devices. Science 336, 1003–1007 (2012).

[2] L. P. Rokhinson, X. Liu, J. K. Furdyna, The fractional a.c. Josephson effect in a semiconductor-superconductor nanowire as a signature of Majorana particles. Nat. Phys. 8, 795–799 (2012).

[3] M. T. Deng, et al., Majorana bound state in a coupled quantum-dot hybrid-nanowire system. Science, 354, 1557-1562 (2016).

[4] K. Delfanazari, R. K. Puddy, P. Ma, T. Yi, M. Cao, Y. Gul, I. Farrer, D. A. Ritchie, H. J. Joyce, M. J. Kelly, C. G. Smith, On Chip Andreev Devices: hard Gap and Quantum Transport in Ballistic Nb-$In_{0.75}Ga_{0.25}As$ quantum well-Nb Josephson junctions, Adv. Mater. 2017, 1701836.

[5] K. Delfanazari, R. K. Puddy, P. Ma, T. Yi, M. Cao, Y. Gul, I. Farrer, D. A. Ritchie, H. J. Joyce, M. J. Kelly, C. G. Smith, Proximity induced superconductivity in indium gallium arsenide quantum wells, J. Magnetism and Magnetic Materials, 2017, http://doi.org/10.1016/j.jmmm.2017.10.057.

[6] Ö. Gül, H. Zhang, F. K. de Vries, J. van Veen, K. Zuo, V. Mourik, S. Conesa-Boj, M. P. Nowak, D. J. van Woerkom, M. Quintero-Pérez, M. C. Cassidy, A. Geresdi, S. Koelling, D. Car, S. R. Plissard, E. P. A. M. Bakkers, L. P. Kouwenhoven, Hard Superconducting Gap in InSb Nanowires Nano Lett., 2017, 17 (4), pp 2690–2696.

[7] H. J. Suominen, M. Kjaergaard, A. R. Hamilton, J. Shabani, C. J. Palmstrøm, C. M Marcus, F. Nichele, Scalable Majorana Devices, arXiv:1703.03699

[8] C. Chen, I. Farrer, S. N. Holmes, F. Sfigakis, M. P. Fletcher, H. E. Beere, D. A. Ritchie, Growth variations and scattering mechanisms in metamorphic $In_{0.75}Ga_{0.25}As/In_{0.75}Al_{0.25}As$ quantum wells grown by molecular beam epitaxy. J. Crystal Growth **425**, 70–75 (2015).

[9] A. F. Andreev, Thermal conductivity of the intermediate state of superconductors. Sov. Phys. JETP. 19: 1228 (1964).

[10] H. Irie, Y. Harada, H. Sugiyama, T. Akazaki, Josephson coupling through one-dimensional ballistic channel in semiconductor-superconductor hybrid quantum point contacts, Phys. Rev. B 89, 165415 (2014).

[11] W. R. Hudson and R. J. Jirberg, Superconducting properties of niobium thin films, Nasa technical note, (1971).

[12] D. K. Finnemore, T. F. Stromberg, and C. A. Swenson, Superconducting properties of high-purity niobium, Phys. Rev. **149**, 231 (1966).