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Configuration of readout electronics and data acquisition for the HiPERCAM instrument

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ABSTRACT

HiPERCAM is a five channel fast photometer to study high temporal variability of the universe, covering from 0.3 to 1.0 microns in five wavebands. HiPERCAM uses custom-made 2Kx1K split-frame transfer CCDs mounted in separate compact camera heads and cooled by thermoelectric coolers to 180K. The demands on the readout system are very unique to this instrument in that all five CCDs are operated in a pseudo drift window mode along with the normal windowing, binning and full-frame modes. The pseudo drift mode involves reading out small window regions from 2 quadrants of each CCD, with the possibility to exceed 1 kHz window rates per output channel. The CCDs are custom manufactured by Teledyne e2v to allow independent serial clock controls for each output. The devices are manufactured in standard and deep-depletion processes with appropriate anti-reflection coatings to achieve high quantum efficiencies in each of the five wavebands. An ESO NGC controller has been configured to control and readout all five CCDs. The data acquisition software has been modified to provide GPS timestamping of the data and access to the acquired data in real time for the data reduction software. The instrument has had its first light and first science observations on the 4.2m William Herschel Telescope, La Palma during a commissioning run in October 2017 and subsequently on the 10.4m Gran Telescopio Canarias in February 2018 and science observations in April 2018. This paper will present the details of the preamplifier electronics, configuration of the readout electronics and the data acquisition software to support the unique readout modes along with the overall performance of the instrument.

Keywords: HiPERCAM, Frame transfer CCDs, TEC CCD heads, fast window readout, differential signal path for CCDs, amplifiers, NGC sequencer scripts

1. INTRODUCTION

Following the continued success of the ULTRACAM[1] instrument on sky for over 15 years, the European Research Council has funded the Universities of Sheffield, Warwick and Durham to build its successor, HiPERCAM, a five channel high-speed camera to study rapid variability in the universe covering the entire optical spectrum, taking advantages of the latest technologies. The scientific goals and the instrument design concepts have been presented earlier at the SPIE 2016 conference[2] in Edinburgh. HiPERCAM extends the performance envelope of ULTRACAM by observing simultaneously in five wavelength channels from 0.3 to 1.0 microns, with double the field of view and number of pixels in each band. A complex optical design has been achieved within a space envelope which is not much larger than the original ULTRACAM design. HiPERCAM uses custom-made 2Kx1K split-frame transfer CCDs manufactured by Teledyne-e2v, Chelmsford, UK, each of which is mounted in a separate small camera head and cooled to below 180K by thermoelectric coolers. An electronics readout system has been configured to readout all five CCDs using ESO's NGC controller and implemented necessary modifications to ESO's acquisition software to support various readout modes of the instrument.

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This paper presents a brief description of the optical and mechanical designs of the instrument followed by the details of the configuration of the readout electronics and the data acquisition software for the instrument. The paper also presents the test results obtained in the lab as well as on-sky performance of the instrument.

2. HIPERCAM INSTRUMENT

2.1 Optical design

HiPERCAM operates over a wavelength range of 300-1000nm, covering the u', g', r', i' and z' wavebands simultaneously. The optical design comprises a four element collimator lens, a series of four dichroic beam splitters (which split the light into the required wavebands) and a set of five, 6 element double Gauss-type camera lenses. HiPERCAM is a visiting instrument and is required to operate on a variety of telescopes. The table below shows the performance on two of the telescopes: the 4.2m William Herschel Telescope (WHT) and the 10.4m Gran Telescopio Canarias (GTC).

Table 1: HiPERCAM optical performance on WHT and GTC.

Parameter	WHT	GTC
Pixel scale ("/pixel)	0.3	0.081
Field of view (arcmin)	10.24 x 5.12	2.76 x 1.38
Image quality (FWHM)	<0.3" across FOV	<0.4" across FOV

2.2 Mechanical structure design

The HiPERCAM design is based on the successful double octopod concept used in ULTRACAM, although HiPERCAM comprises four Aluminium platforms instead of three. It incorporates different material types to provide extremely high stiffness irrespective of its tilt and orientation on the telescope. Electrical isolation is achieved by a Glass composite flange. The structure's central platform houses the hull containing all of the optics. The platforms are interconnected by a set of carbon fibre struts having concave alignment spigots connected at both ends, which in turn abutt onto aluminium hemispheres bolted onto the respective platforms. This self-aligning modular construction allows deconstruction to be conducted if required. The instrument is mounted onto the telescope via a dedicated Interface Collar, allowing optimum positioning of the instrument. Currently, two Collars exist: one for the WHT and one for the GTC.

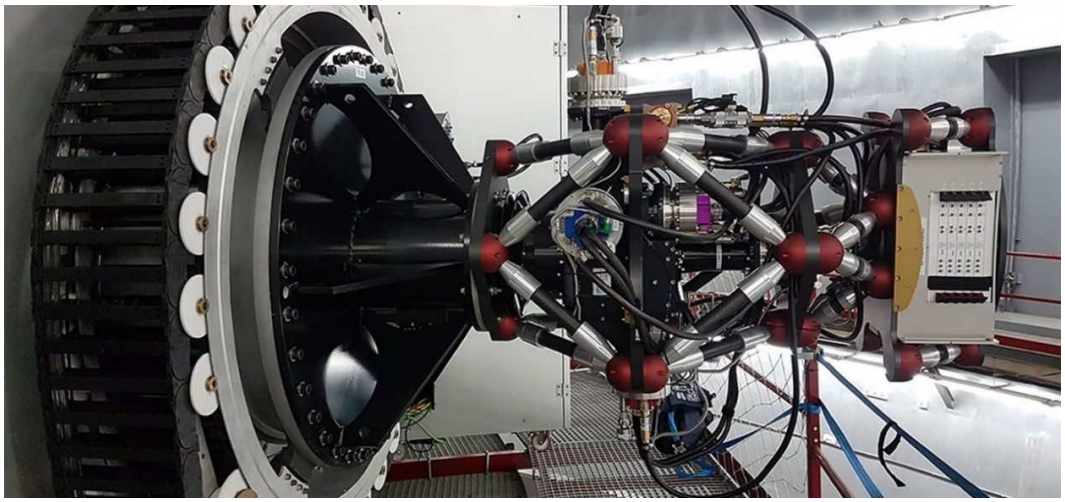

Figure 1: HiPERCAM mounted on one of the folded Cassegrain focus of the GTC. The octopod provides extremely high stiffness. The hull in the middle houses all of the optics and CCD heads. The instrument collar interface to the telescope (on the left) and the NGC controller (on the right) can also be seen in the picture.

2.3 Detector system

The HIPERCAM detector system block diagram is shown in Figure 2. A brief description of the individual units is given below:

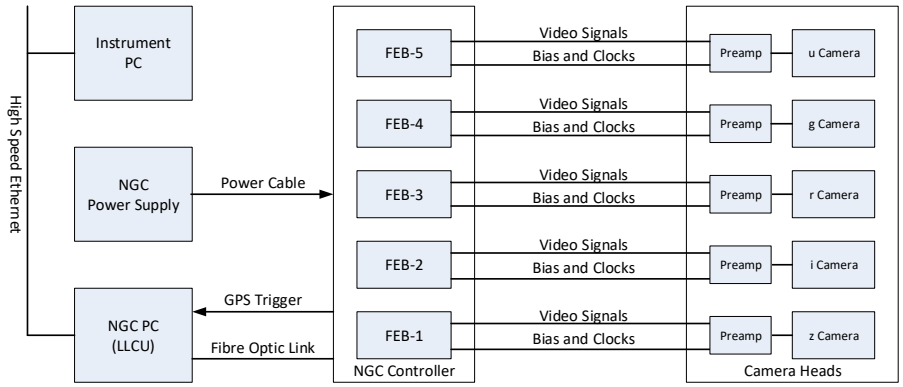

Figure 2: Block diagram of the HiPERCAM detector control system

HiPERCAM uses five Teledyne e2v CCD231-42s for five channels of the instrument. The CCD231-42 is a back illuminated, 2K x2K, 15um pixel device operating in a 2Kx1K (columns x rows) split-frame transfer mode with 4 readout ports. Two types of devices have been produced; standard silicon with blue optimised AR coatings for UV to blue wavelengths and deep-depleted devices with AR coatings optimised for visible to near infrared wavelengths. The CCD has a 2Kx1K image area in the middle and masked areas of 2048x520 at the top and bottom. Each half of the image area is frame transferred to the respective masked areas in frame transfer mode and read out through the serial registers, one at the top and one at the bottom of the device. Each serial register has two readout ports which can be independently clocked from each other. That is, all four outputs on the CCD can be clocked independently of each other. The parallel clocks for the top and the bottom sections of the CCD are made common. In order to achieve fast frame-transfer times, the parallel registers are operated in a 2-phase mode. In HiPERCAM, the top and bottom parallel sections are clocked synchronously. Hence the entire image and the storage area can be clocked using only 4 parallel clocks (2 for image sections and 2 for storage sections). The devices are capable of fast line transfers of 8us. The deep-depletion variant devices have fringe-suppressing anti-etalon structures and high quantum efficiencies in the red part of the spectrum.

Universal Cryogenics in Tucson, Arizona co-designed, manufactured and supplied the Peltier cooled camera heads for HiPERCAM. The camera heads have been manufactured from stainless steel and use a pair of 5-stage Peltier elements (thermo electric coolers) to cool the CCDs. The heat exchange block mounted inside the camera head uses cold liquid circulation to remove the heat from the hot side of the Peltier elements. The camera heads achieved operating temperatures below -90C with a circulating water temperature at 5C. A CCD preamplifier electronics PCB is mounted at the back of the camera head within 10cm of the CCD to amplify and drive the CCD output signals to the controller.

The CCDs are operated using ESO's NGC controller[3], which is equipped with 5 front-end basic (FEB) boards and their transition modules. An FEB board has 4 differential video processing chains each with 1MHz, 16-bit A/D converters. The controller is connected to an NGC workstation (also called a Local Linux Control Unit or LLCU) via a duplex fibre link through a PCIe host interface board. A separate power supply rack provides the required DC power supplies to the controller. The LLCU is also equipped with GPS time processing hardware to time stamp the acquired data. As the CCDs are operated in a frame-transfer mode, no mechanical shutter is required to define the exposures. The exposure time resolution is set to 0.01ms which is the time required to generate a trigger pulse (also for no-trigger) for the GPS timestamp hardware and is included in the given exposure time. The minimum exposure time that can be specified is dependent on the CCD clear option. If the clear CCD option is set, an exposure time starting from 0.01ms to several hours can be specified. If the option is not set, then the CCD is not cleared between the reads and the minimum expose time is the frame readout time.

2.4 Data acquisition software

The CCD control and the data acquisition are provided in a real-time Scientific Linux environment. The host computer is an industry standard 19" rack mountable PC with ample storage space. The acquisition and control software allows complete control of the camera controller, including the selection of readout speeds and readout modes (full frame, quad (one window in each CCD quadrant), two quads (2 windows in each quadrant), drift window and related options). See section 4 and 5 for the details of the configuration of the acquisition software for different readout modes.

3. PREAMPLIFIER DESIGN

CCD signals from the top and bottom pairs of outputs are brought outside the camera head by two custom flex cables through two hermetic micro-d connectors (SRI hermitic back-to-back 37 way micro-d connectors). A preamplifier board that plugs onto these two micro-d connectors has been designed which implements ac coupled differential pre-amplifier circuits, passive filters on bias lines, over-voltage and ESD protections on the input bias lines of the CCD. Passive filters and over-voltage protection are provided on each bias line by resistors, capacitors and zener diodes. Protection against ESD is provided by fast switching protection circuits, SP720s from Little fuse. The bias and clock inputs are protected from both positive and negative transients above the respective threshold voltages. The low input capacitance of the protecting structures of the SP720 have negligible effects on the clock rise / fall times.

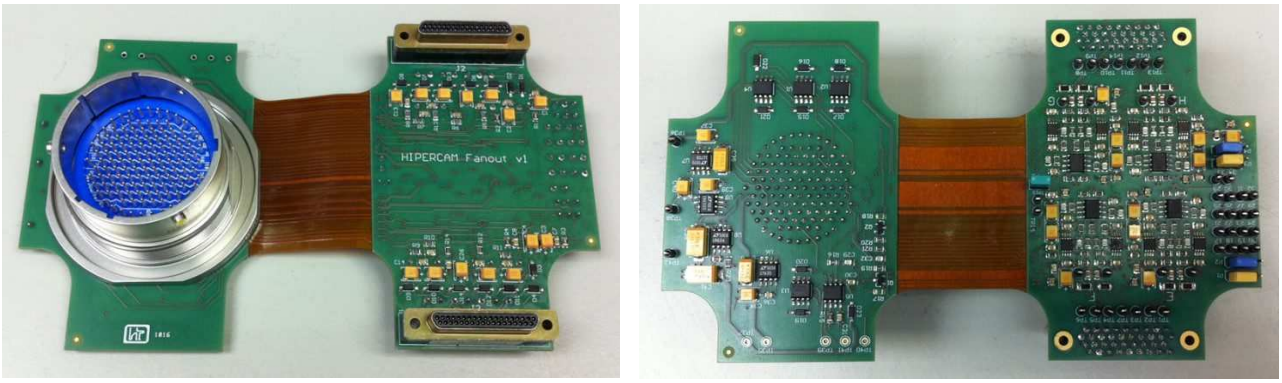

Figure 3: HiPERCAM CCD preamplifier – top and bottom sides of the rigid-flex-rigid boards.

The preamplifier board comprises two rigid PCBs connected by a flex cable. One of the two rigid PCBs (PCB-1) implements the CCD protective and preamplifier circuits and has two 37 micro-d connectors which plug onto the two corresponding SRI hermitic connectors on the back of the camera head. The other rigid board (PCB-2) which is folded back onto the PCB-1 implements power supply regulators for preamps, circuits to generate an extra clock required (see section 3.1), and has a 128-pin circular connector for interfacing to the CCD controller. The PCB-2 is attached to the metal lid of an aluminum box enclosing the preamp boards which provides a full EMI shield.

Figure 4: Preamplifier in an enclosure on the back of the camera head.

3.1 Generation of an extra clock

Each FEB board of the controller is capable of supplying up to 20 bias supplies and up to 18 clocks. However, the CCD231-42 requires at least 19 clocks for independent clocking of all four outputs, even after optimally sharing the parallel and other serial clocks. An extra clock (identified as Dump Gate) is generated from a General Purpose I/O line (GPIO) available on the FEB board. The circuitry needed to translate the 3.3V level GPIO clock to the required CCD dump gate level is implemented in the preamplifier board (PCB-2). The Dump Gate clock high level is supplied from the Reset Gate clock high rail and hence the high level of the Reset Gate and the Dump Gate are same. This works well as the Reset Gate is

normally held at high level during the serial register dump operation. The low level of the Dump Gate clock is fixed at substrate voltage and is within the nominal clock low level for the CCD dump gate.

3.2 Differential preamplifier

The preamp is designed to take the advantage of the dummy outputs available from the CCD to form a true differential preamplifier which can effectively reduce the common mode noise such as EMI, input offset drifts or pickup noise at the telescope. The CCD active and dummy MOSFET source outputs are loaded with suitable resistive loads on the fan-out board to provide the required operating drain currents. The output signals are then ac coupled to a differential pre-amplifier. The differential outputs are connected to the differential inputs of the signal processing chain in the FEB board through a 1.6m length multi-screened cable.

As there is no gain in the signal processing chain of the FEB board, the required signal gain is provided at the pre-amplifier. The output sensitivity of the CCD is about 7.4μV/e^-. The ADC on the FEB board is configured for the +/-2.5V input voltage range. The gain of the preamplifier is set at about 9.0 to match the dynamic range of the CCD full well capacity to the input range of the ADC. This gain setting results in a conversion gain of about 1.2e^-/ADU and hence the ADC saturates at about 80ke, slightly below the full well capacity of the CCD whilst the read noise (4 to 5e) is adequately sampled.

The NGC FEB implements two methods of signal processing: Correlated Double Sample (CDS) and an Analog Clamp Sample (ACS) method. The signal processing method is configured in the hardware by a number of solder jumpers, and hence this is not programmable. The FEB boards for the HiPERCAM are configured for the ACS method which is implemented by clamping the video chain during the reset phase and sampling the signal after the charge dump during the pixel readout cycle.

The design of the preamplifier is based on the preamp design for ZTF mosaic camera[4]. This is a conventional differential amplifier (a two op-amp configuration commonly used in infrared applications at cryogenic temperatures) and uses analog switches to establish black levels before the preamp. Figure 5 shows a simplified circuit schematic of the preamplifier design. The preamp makes use of the dummy outputs from the CCD to form a true differential signal path from the CCD to the controller. The FEB board accepts differential input signals and presents the inputs to the ADC as differential inputs. Hence the complete chain from the CCD to the ADC is truly a differential signal path and benefits from rejecting any common mode or pickup noise. However due to the use of two outputs, the resultant noise is √2 times higher compared to a single output.

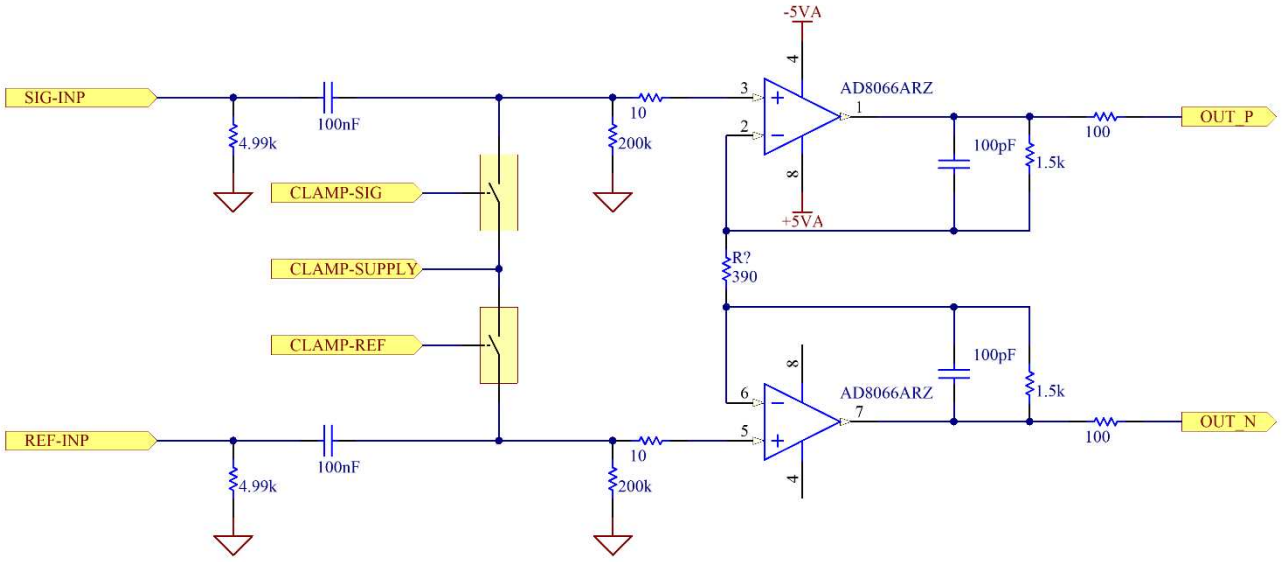

Figure 5: A simplified circuit schematic of the differential preamplifier.

The preamp can also be configured to use in a single ended mode where the dummy output is still powered, but the reference input of the preamp is permanently clamped to a reference clamp supply via an analog switch through software configuration that selects a different clock pattern. In this configuration, the noise contribution to the total noise from the

dummy output should be negligible. However, if it is preferred to depower the dummy outputs (e.g. to reduce the power dissipation within the CCD), then this can be done by selecting corresponding jumper links on the fan-out board.

3.3 Bandwidth and noise

The -3dB bandwidth on the preamp board was initially set to 2.25MHz, using appropriate resistor and capacitor values in the feedback paths of the differential preamplifier. The measured read noise with an engineering CCD was around 6.5e^- at 263kHz pixel rate. As there were no extra clocks available (at the time of the preamp design) the bandwidth is not programmable on the preamp board. The -3dB bandwidth was then reduced to about 1.06MHz which resulted in a slightly lower read noise of about 5.1e^- rms at the same pixel rate. The bandwidth of 1.06MHz is achieved by changing the feedback capacitor. Reducing the bandwidth reduced the read noise by about 1.4e^- at slow speed.

The -3dB bandwidth limit is set according to:

$$\text{-3dB bandwidth} = 1/(2\pi\tau), \text{ where } \tau = \text{Pixel Period} / (-2 \times \ln(1 - \text{Vout}/\text{Vin}))$$

The current bandwidth limit (1.06MHz) is a bit high for the slow readout speed (263kHz) which allows the signal to reach more than 99.999% of its final value, whereas for the fast speed, it allows the signal to reach 99.9% of the final value. Hence it is more optimally set for the fast speed. This could be a reason for the slightly better readout noise ~4.5e^- is achieved in the fast speed (523kHz). The read noise in the slow speed later was improved to ~4.0e^- by taking multiple samples (4 samples per pixel) of the signal level.

3.4 Gain and non-linearity

The gain of the preamplifier including the FEB signal processing chain is measured by injecting a pulsed signal at the inputs of the preamp board. The pulsed inputs (active OS and dummy OS) are generated from an arbitrary function generator and triggered to synchronise with the readout using the summing well clock to synchronise with the ACS sampling of the FEB board. The dummy output is pulsed from 0V to 700mV whilst the active output is pulsed from 0V to the desired voltage below 700mV. The high amplitude of the active output is varied from 675mV to 400mV in steps of 25mV and the data is acquired at each step. Figure 6 below shows the measured gain as 8.45 from the preamplifier to the ADC (the set value of the gain at the preamp is 8.70). The FEB signal transfer function is separately measured by injecting a pulsed input signal swept over the ADC input range and synchronised with the clamp sample readout. The FEB transfer function is measured as 79.25µV/ADU.

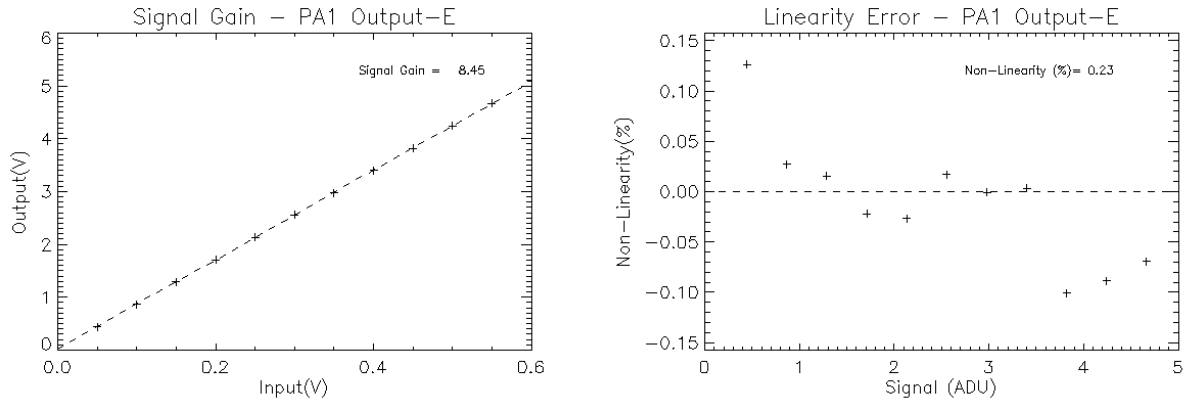

Figure 6: Gain and linearity of the HiPERCAM signal processing chain (preamplifier plus the FEB signal processing). The set gain at the preamp is 8.70 at the preamplifier.

The ADC on the FEB (AD7677ASTZ, 16 bit, 1MHz full speed) is configured for a +/-2.5V input range, with a maximum input signal limit of +/-3.0V. At a conversion gain of 7.4µV/e^-, the ADC saturated full well (80ke) corresponds to about 0.59V signal swing from the reset level. With a differential gain of 8.7 in the preamplifier, the corresponding output swing is 5.03V, which matches well with the dynamic range of the CCD.

4. HIPERCAM READOUT MODES

The HiPERCAM CCDs are required to operate in four different readout modes: full frame, one window per quadrant, two windows per quadrant and drift window readout modes. Usual options such as clearing the CCD before an exposure (except in drift mode where the CCD is not cleared), include pre-scan, over-scan pixels, binning pixels, control LED exposures are included in each mode. In addition, the readout needs to take care of reflected images in some channels due to the optical layout of instrument. This is especially important in the windowed readout modes, where individual windows (rows) in different quadrants are aligned before reading them out in parallel. There is also a requirement to skip a defined number of readout cycles in any of the cameras and synchronise their readout from the following readout cycles.

The hardware architecture of the CCD allows independent clocking of each serial register. That is, one half of the serial register can be shifted towards its nearest output amplifier without shifting charges on the other half of the register. This architecture allows full control of the serial clocking in each of the 4 outputs of the CCD. However, the sharing of the parallel clocks results in synchronous parallel clocking in the upper and lower sections of the CCD. That is, the row shifts happen in parallel in both upper and lower sections. Every time a row transfer (transfer from active area into the storage area) or row shift (row shift from the storage area into the serial readout register) is performed, row transfer or row shifts happen simultaneously in both upper and lower sections. The CCD has four readout ports namely E, F, G and H, which are connected to the respective video processing channels 1 to 4 on the FEB board. For each ADC conversion, four pixels from each FEB board (one pixel from each video chain) are transmitted to the host interface board in the order from FEB1 to FEB5.

4.1 NGC IR software

The NGC infrared detector control software (DCS) has been used as it is more suited to the HiPERCAM data acquisition needs. Several detector sub parameters, such as window co-ordinates and other camera specific options, have been defined in an input sub-parameter file. The values of these parameters can be changed from within the NGC GUI or can be set using commands sent to the NGC DCS server. The required clock patterns are created using ESO's graphical editor tool called 'BlueWave'. Evaluation of various control parameters and the sequencer program flow is scripted in TCL/TK. All five FEB boards run the same sequencer script for a given readout modes in an infinite loop. Typically, a base sequencer script is created for a given readout mode and copied to individual sequencer scripts to run on different FEB boards. The individual sequencer script file is then edited to change a couple of camera specific options in the script such as the NSKIPS and REFLECT parameters. This way, all of the sequencer scripts and the timing remains the same for all FEBs and keeps them all synchronised with each other for a given readout mode.

4.2 Full frame mode

Full frame readout mode is the simplest mode in which the top half of the central active area is transferred into the upper storage area, while the other half is transferred down into the lower storage area. Charge is then shifted and digitized through all four outputs in parallel. Options to skip readout cycles, clear CCD, include pre-scan pixels, over-scan rows and binning pixels are supported. There is no reflect option required in this readout mode as the entire CCD is read out through all 4 outputs in parallel.

4.3 Window mode

A set of one window or two windows (non-overlapping in rows) per quadrant from each CCD are read out from all 5 CCDs. The windows in each quadrant have the same row start, but can have different column starts. The size and start locations of the windows are the same on all five CCDs. The size of each set of windows can be different. Figure 7 illustrates the requirements for different windows to be read out.

After the frame transfer, all rows are dumped until the start row of the first window set. A row at a time is then shifted into the serial register and the columns starts are then aligned by skipping the minimum number of pixels in each output individually (i.e. the column starts are set to be the same distance from their respective output amplifiers). Once aligned, the required pixels are read out in parallel from all four outputs. The row shift, column alignments and readouts are then repeated for all rows of the window region. Options to clear the CCD, skip readout cycles, include pre-scan pixels and binned read out are all supported. In addition, the reflect option takes into account the reflected images on some channels during window alignment in different outputs. The two window readout mode is exactly same as the one window readout except that two non-over lapping (in rows) windows are readout from each quadrant of a CCD. The readout methodology and options supported are the same as with the one window readout mode.

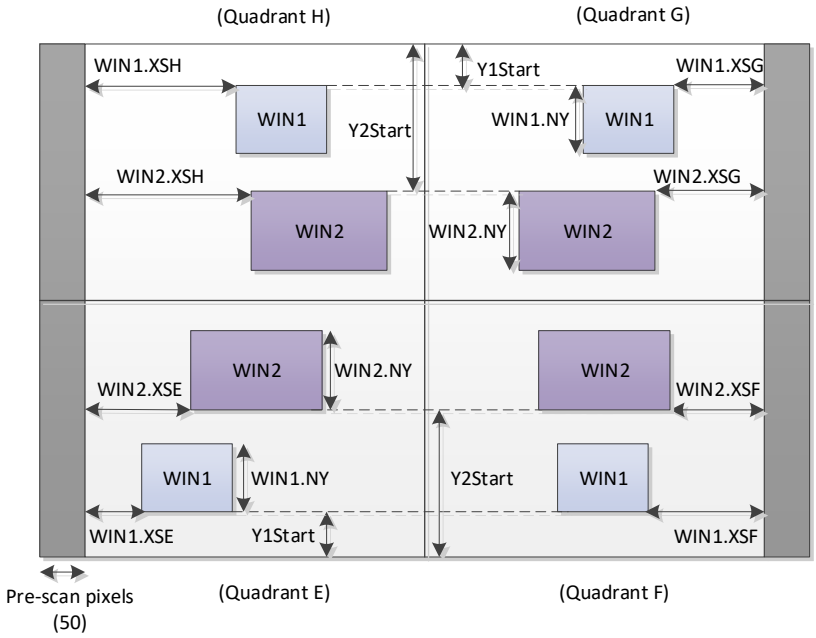

Figure 7: Window readout modes in HiPERCAM. Four quadrants of a CCD with two sets of windows are shown with pre-scan pixels in each readout port.

4.4 Drift window mode

In the drift readout mode, a focal plane mask is employed in the telescope focal plane such that only a few rows above the lower storage area are exposed. The exposed rows after a desired integration time are quickly transferred into the top of the storage area section. Every time a new set of rows (windows) are exposed and shifted into the storage area, the previously exposed rows under the storage area are drifted down towards the readout register where they are readout, whilst new exposures are taking place in the active area. As the windows are read out, gaps form between the windows in the storage area. Depending on the window size (in rows), it may not be possible to fit windows with equal gaps between them. In order to ensure the same exposure time for every window, the exposure times for the windows with equal gaps have to be increased by a small pipeline delay equal to the time required to dump the extra rows for the window with a larger gap. The number of extra rows to dump will vary depending on the window height (WIN.NY) and the bin factors used.

In CCD231-42, the storage section on either side of the central active area has 520 rows. The number of windows that can be fit within this area is calculated from:

$$\text{NWINS} = \text{INT}((520.0 / \text{WIN.NY} + 1) / 2).$$

The number of extra rows to dump (for the window with a larger gap) is calculated from:

$$\text{NROWS} = 520 - (2*\text{NWINS} - 1)*\text{WIN.NY}.$$

A delay equal to the time required to dump NROWS is added to the given exposure time for NWINS-1 windows, and no delay is added to the window with a larger gap when the extra NROWS are dumped instead.

4.5 Skip readout cycle

Normally, all five CCDs are read out in parallel. However, any of the 5 CCDs can be skipped a number of readout cycles set by the NSKIPS parameter (e.g. to integrate sufficient signal before reading out). If a CCD is set to skip a readout cycle, the corresponding sequencer runs exactly the same timing as the other CCDs that are read out normally, but without shifting the charges from the active area on that CCD. However, the signal processing still clocks and outputs a digital value for each pixel. Hence, irrespective of the NSKIPS parameters, the data generated by the readout has the same size. As the timing is exactly same, including dummy clocking to skip readout cycles, they always remain synchronous with each

other. This SKIP option is available in full frame, 1 window and 2 window readout modes. This option is currently not available in the drift mode due to complications arising with the pipeline delays.

As an example, consider NSKIPS1=2 for CCD1 whilst all other CCDs are set to skip 0 reads (NSKIPS2=0, NSKIP3=0 and so on). The main sequencer that executes the wipe (W), expose (E), read (R), dummy wipe (DW), dummy expose (DE) and dummy read (DR) routines in an infinite loop are shown below:

LOOP INFINITE JSR WIPE JSR EXPOSE LOOP NSKIPS1 JSR DUMMY_READ JSR DUMMY_WIPE JSR DUMMY_EXPOSE END JSR READ END	LOOP INFINITE JSR WIPE JSR EXPOSE LOOP NSKIPS2 JSR DUMMY_READ JSR DUMMY_WIPE JSR DUMMY_EXPOSE END JSR READ END
Sequencer loop on FEB1	Sequencer loop on FEB2,3,4,5

The sequencer1 execute the following sequence of routines:

W	E	DR	DW	DE	DR	DW	DE	R	W	E	DR	DW	DE	DR	DW	DE	R	.	.

The sequencer2 (and the rest of sequencers) execute the following sequence of routines:

W	E	R	W	E	R	W	E	R	W	E	R	W	E	R	W	E	R	.	.

Figure 8: Example of read out cycle skips.

As all the sequencers execute either the actual or the dummy routines of the same function at any given time, and both the actual and the dummy routines have exactly the same timing (but the dummy routines do not shift the charges from the CCD), they always run in synchronous with each other, irrespective of the number of readout skips on any one or multiple CCDs.

4.6 Reflected images

Due to multiple reflections of the light in the optical path of the HiPERCAM instrument, some of the cameras have reflected images at their focal planes which require the serial clocks swap between E and H outputs and between F and G outputs. The REFLECT option is used to specify which of the cameras have reflected images. For the CCDs with the REFLECT option set true, the serial clocking is swapped between the E and H outputs and similarly between F and G outputs. As individual sequencer scripts are running on different FEBs, it is possible to swap clocking on selected CCDs. This switch in the sequencer script makes it possible to use the same set of external cables for all cameras. This option is available in 1 quad, 2 quad and drift modes. The option is not required for full frame as the entire frame is readout.

5. ACQUISITION SOFTWARE

The system architecture of HiPERCAM for software and configuration is illustrated in Figure 9 below. The control/data acquisition server (ngcircon) is the entry point for the NGC Infrared software, through which all system communication is done. The control server communicates with the NGC electronics through driver interface process (ngcb2Drv). The data acquisition process (used for data acquisition and pre-processing) is also launched and controlled by the control server.

5.1 Modifications to NGC IR software

The modification of NGC IR software for HiPERCAM is made in the data acquisition process task called hiperCamCCD. It operates on different HiPERCAM readout modes, creating the correct FITS header information. Once the hiperCamCCD task is launched with option parameters, it receives data from the NGC-PCIe card. When the exposure of a frame is complete, it reads the timestamp from the GPS driver and then adds it to the end of the frame before passing the frame data to the FITS Files task for writing FITS files to the hard disk. The GPS timestamp is synchronized with the start of exposure by an external trigger from the NGC controller. The hiperCamCCD task runs continuously until either the required number of frames have been obtained or a “STOP" command has been issued. Depending on the mode and option parameters, the hiperCamCCD task can also perform the software N-sample average technique for noise reduction.

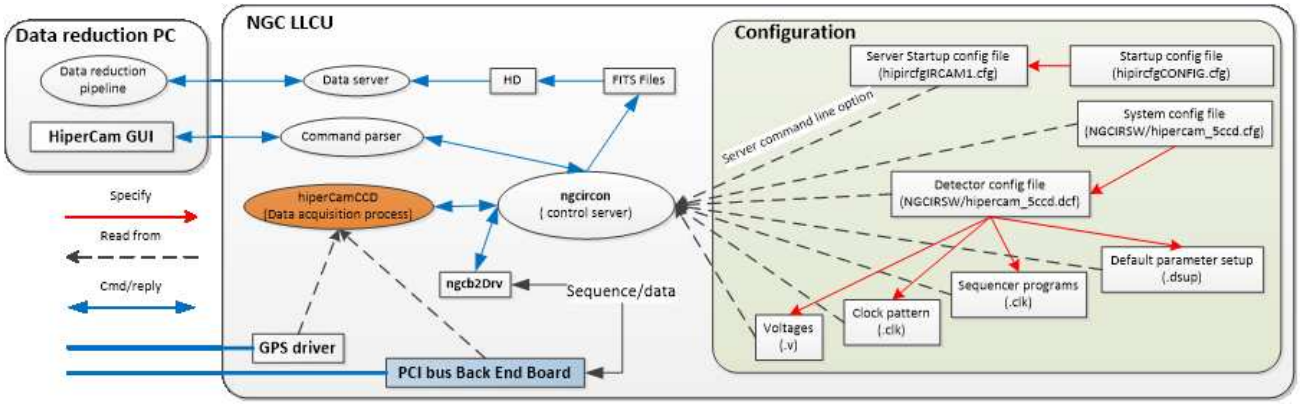

Figure 9: System architecture of HiPERCAM software and configuration.

5.2 interfaces to higher level software

HiPERCAM can be controlled by low level commands sent to the NGC DCS. These commands allow changing the readout mode and altering parameters within the sequencer scripts, as well as the stopping/starting of data acquisition. To allow control of HiPERCAM over the network, a HTTP server with a RESTful interface has been written in Python. This server runs on the Scientific Linux PC and issues low-level DCS commands. For the end-user, HiPERCAM is controlled via a GUI, written in Python/Tk, that sends requests to the HTTP server. For real-time viewing of the data and data-reduction, a Python WebSocket server runs on the Scientific Linux PC. Connections to this WebSocket allow clients to retrieve individual frames from the FITS files that contain an exposure sequence. A Python-based data reduction pipeline is used to view the data in real time at the telescope.

6. CAMERA PERFORMANCE

The standard FEB board can set bias voltages up to a maximum of 28V. Depending on the current flow, the actual voltage applied to the CCD can be less than this. For example, the output drain bias draws about 5mA current for each output. For the differential configuration, the same bias is used for both the active output and dummy output drain supply, which doubles the current on that bias line. The bias lines have 100 ohms series resistors in the FEB for telemetry of set and applied voltages. This reduces the actual applied voltage to the drains of the output MOSFETs to about 26.5V. This reduced supply had a pronounced effect on the linearity and to some extent the system gain.

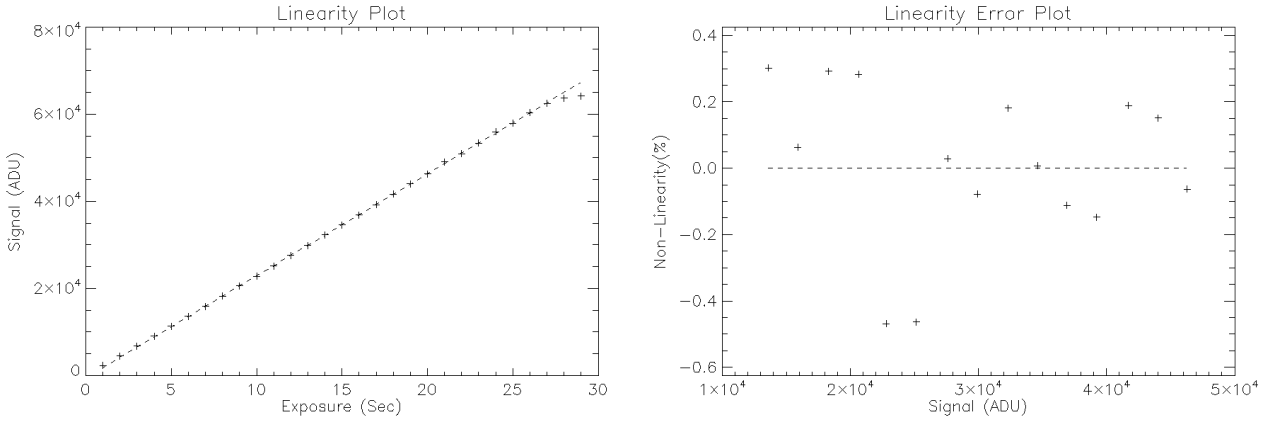

Figure 10: Linearity of one of the channels of a HiPERCAM camera (20 to 80% of full well). Similar linearity was measured form all cameras after the increase in the VOD supply.

In order to improve the linearity, the FEB boards have been modified to generate up to 32V output drain supply, by changing the voltage setting resistors around the voltage regulators and increasing the DC power supply. This allowed us to apply drain voltages up to 30V as recommended by e2v for these devices. This improved the linearity significantly

(reduced the non-linearity from about 6% to less than 1% p-v). Figure 10 below shows the non-linearity measured from one of the readout channel from 20% to 80% of the full well.

Similarly, increasing the high level voltage of the parallel clocks from the typical recommended levels by about 1V resulted in a better full well capacity and a more linear photon transfer function (Figure 11).

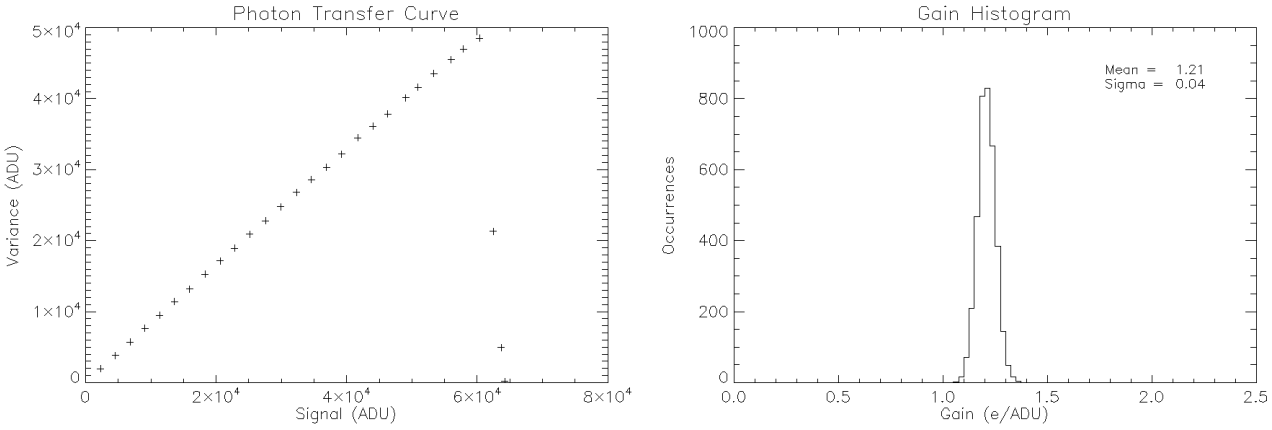

Figure 11: Linear photon transfer and gain histogram of a readout channel of a HiPERCAM camera. The linearity in the photon transfer curve and higher full well capacity have been obtained after increasing the high level of the image and storage clocks.

The bias signal in the pre-scan pixels stays firmly at the same level irrespective of the signal level in the imaging area. Both active and reference inputs before the preamplifier are clamped to the clamp reference supply at the beginning of each line readout.

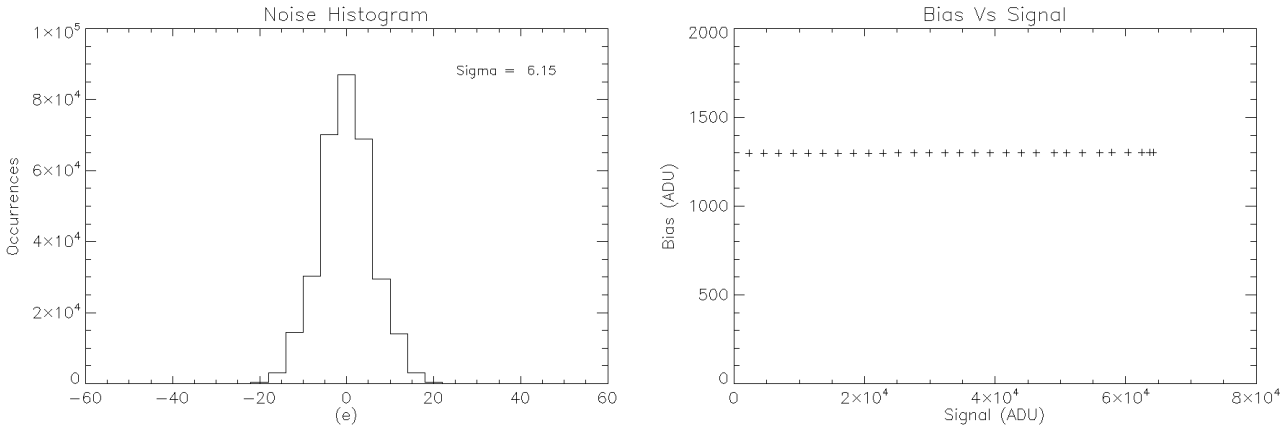

Figure 12: Noise histogram of a readout channel of a HiPERCAM camera at 263kHz pixel rate. Better read noise (~4.5e to 5e) is measured at the 526kHz pixel rate. Read noise in the slow speed was improved to 4e to 4.5e with multiple samples per pixel.

The instrument had its first commissioning run at the 4.2m William Herschel Telescope on La Palma during October 2017 and further commissioning and science observations took place during February, March and May 2018 on the 10.4m Gran Telescopio Canarias, also on La Palma. Please refer to the paper[5] (at this conference) for further details on the design and performance of the instrument and results from the commissioning and science observation runs. There was no noticeable pick up or interference seen in the data in the differential mode configuration. However, in the single-ended mode (when the reference input to the differential amplifier is permanently clamped to a quiet supply), quite a bit of interference is seen and the noise was generally higher than in the differential configuration.

The measured dark current at the operating temperature (-90C) was about 200e/hour. The QE of the devices were not measured in our laboratory, but the e2v measured values were well above the requirements.

Figure 13: A first light picture from the commissioning run at the William Herschel Telescope, La Palma. Image of NGC7331 produced from 20 minute exposures from 4 cameras.

7. ACKNOWLEDGEMENTS

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