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Switching Loss Optimisation of Cascaded H-Bridge Converters for Bidirectional Grid-Tie Battery Energy Storage Systems

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Abstract— **Multilevel converters are an emerging industrial technology and are the subject of a substantial amount of research. However, they are yet to find their way into many mainstream engineering applications. This paper presents a method of quantifying the benefits and disadvantages of multilevel converters of increasing order. The analysis focuses on the cascaded H-bride topology for grid-tie battery inverter applications. The analysis includes both semiconductors losses and semiconductor driver losses. It is shown that multilevel converters can have significant benefits over their conventional counterparts, but that more levels is not necessarily better. This paper's important result is to create a quantitative measure of the pros and cons of multilevel architecture.**

Keywords—multilevel, switching loss, grid-tie, optimisation

I. Introduction

The electrical generation and distribution industry is undergoing rapid change, moving away from fixed generation at large, centralised generation, together with uncontrolled demand, towards the much discussed 'smart grid'. The smart grid is a necessary progression that all developed nations will be increasingly moving towards in the coming years. One of the key aspects of any smart grid will be energy storage. [1] This will likely come in various forms and on a range of scales, but one area of active development is domestic level electrical energy storage in batteries. This could primarily serve to address the issues of grid stability and varying demand; and even enable households with domestic generation (e.g. solar) that are currently, in principle, energy independent to become fully power independent of their local electrical grid.

An exciting converter topology for this application is the multilevel converter. These offer the opportunity to integrate the battery management into the converter, with smaller battery packs utilised at each level of a cascaded H-bridge which can be dynamically utilised. Multilevel converters that can also manage balancing of cell strings within the converter topology are an area of active research. Papers can be found referring to it dating from 2009 [2, 4], covering the hardware and algorithms utilised and the results attained, with many common, or at least similar, approaches. This has been demonstrated to be able to very effectively balance between strings even with very different capacities and initial state of charge [5, 6].

Thus it has also been demonstrated that multilevel converters can not only perform essential string balancing operations, but also adapt to battery strings as they degrade, reducing the barriers to use of already degraded batteries such as second life electric vehicle batteries.

An aspect consistent across papers published in the field, is the lack of justification for the number of levels chosen in their analyses [2, 3, 6, 7]. While this is not a criticism of the research, and certainly does not invalidate their efforts, some sort of analytical method for evaluating multilevel converters of increasing order would be of use in moving this technology from research into industrial application. This is the goal of the research here.

II. Proposed Analytical Method

While there are a number of factors that can be considered in the optimisation of a power electronic converter, this paper will exclusively consider semiconductor losses and the losses in the associated drivers. While this is not a complete analysis by any means, the results are useful indicators and, being largely independent of miscellaneous system configuration (e.g. thermal management, filtering configuration, etc.), it forms the foundation of further analysis.

For the purposes of this paper, a specific application will be considered. This will help focus the scope of the work, but it is worth noting that none of the methods discussed are exclusively applicable to the chosen scenario. As previously discussed, this paper focusses on converters for domestic energy storage, so this guided the specification. Some key parameters are stated below:

- A 50Hz 230V mains interface (UK standard).
- Maximum RMS power capacity of 6kW.
- Nominal 500V DC link.

Switching frequency is not initially specified, as the effect of switching frequency on the analyses is to be examined. This paper will focus on a single phase, cascaded H-bridge converter, figure 1. This topology is ideal for battery-based inverters as it requires an isolated dc voltage for each level, something which can easily be supplied by a battery pack, B1...B3 in figure 1.

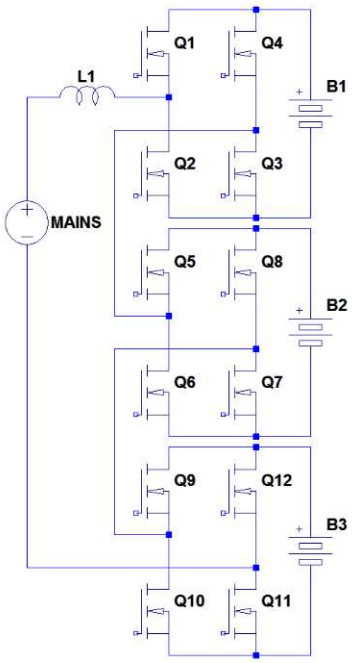

Fig. 1 A simplified schematic of a cascaded H-bridge multilevel

In general, the losses in the converter are considered as a sum of a number of different contributing factors. These include both losses in the semiconductor devices themselves, and the gate drivers. Only MOSFET devices are considered as even in the best case scenario for its rivals (a single bridge at low frequency) modern MOSFETs outperform their BJT and IGBT counterparts in this power and voltage range. However, the same techniques could be expanded and applied to a range of devices and topologies. The specific losses calculated individually here are:

- Power dissipated due to the on-state resistance of the MOSFET.
- Transient power dissipation into the gate of the MOSFET.
- Transient power dissipation through charging and discharging of the 'output capacitance' (the capacitance from drain to source) of the MOSFET, hereafter referred to as output loss.
- Transient power dissipation in the MOSFET gate drive.
- Quiescent power dissipation in the MOSFET gate driver.

A. *On-State Resistance Derivation*

The on-state resistance is a relatively straightforward expression to derive. MOSFET on-state resistance is readily available on the device datasheet, but does vary with temperature (often by a great deal). Instead of using the best case value often stated prominently at the top of datasheets, a more realistic figure was used by finding the on-state resistance when the device is at 80°C. This gives an expression for converter power dissipation due to on-state resistance of:

$$P_{R,ON} = 2NI_{RMS,MAX}{}^{2}R_{DS,ON(@80°C)} \quad (1)$$

Where $I_{RMS,MAX}$ is the maximum RMS system current and N is the number of cascaded H-bridges in the converter. Please note that N should not be confused with the number of levels that the converter can achieve, which is actually characterised by the expression 2N+1.
The factor of two is due to the fact that at any time exactly two devices are conducting in each bridge.

B. *Transient Gate Dissipation*

To calculate the energy dissipation in the gate over one switching cycle, the integral of the gate charge-voltage curve must be calculated. Figure 2 shows the gate charge-voltage curve for a MOSFET.
The first element to be calculated is the Miller charge. This is responsible for the plateau that can be seen in the centre of the graph in (2). The Miller charge can be expressed as the following integral:

$$Q_{MILLER} = \int_{0}^{V_{DS,MAX}} C_{rss}(V_{DS})dV_{DS} \quad (2)$$

Where C_{rss} is the capacitance between the gate and the drain of the MOSFET, also known as the feedback capacitance, and V_{DS} is the drain-source voltage applied to the MOSFET.
This may seem trivial, but in practice is not entirely straightforward as an inspection of the datasheet for any device shows that the feedback capacitance varies significantly and non-linearly with respect to the drain-source voltage, V_{DS}. A linearising approximation is made for C_{rss} and C_{oss} (which is used later). This approximation was experimentally and analytically challenged and was found to be a reasonable approximation of the information quoted on the datasheets of multiple devices when compared with real world performance.
$V_{DS,MAX}$ is defined by the number of cascaded bridges in the converter and the DC link voltage, as the total required DC link voltage is divided over the number of bridges in the converter.

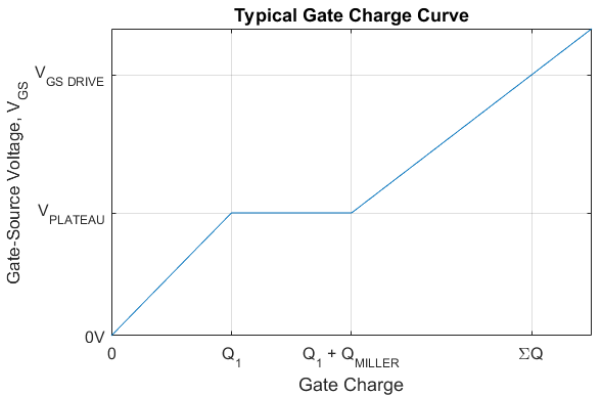

Fig. 2 A Typical MOSFET gate charge-voltage curve, with some key values annotated.

The previous expression (2) can be modified to account for sinusoidal variation of $V_{DS,MAX}$ due to the utility mains supply using the expression:

$$Q_{AV}(V_{DS}) = \frac{\int_0^{\pi/2} Q\left(V_{DS,MAX}\sin(t)\right)dt}{\pi/2} \quad (3)$$

The gradient of the sloped elements in figure 2 are determined by C_{iss}, also known as the input capacitance. This is a combination of the capacitances between the gate and drain and the gate and source. This too varies with respect to the drain-source voltage, but the variation is small and it has been approximated to a representative constant value for the purpose of this estimation. This has, too been shown to be a reasonable approximation. $V_{PLATEAU}$ can be found on the datasheet for the device, and the maximum gate-source voltage, labelled in figure 2 as $V_{GS,DRIVE}$, is the choice of the designer but is nominally twelve volts for MOSFET drives, and this is the value used.

The transient power dissipation can therefore be modelled by the expression:

$$P_{GATE} = 8E_{GATE} \times f_{SWITCHING}$$

$$E_{GATE} = {}^1/_2\, C_{iss}{V_{GS,DRIVE}}^2 + Q_{MILLER} * V_{PLATEAU} \quad (4)$$

C. Transient Output Loss

This source of this loss is due to there being a voltage current product between the source and the drain of the transistor(s) owing to the finite switching time of the device. This can be characterised as the double integral of the output capacitance with respect to the drain source voltage, V_{DS}.

$$E_{OUT}(V_{DS}) = \iint_0^{V_{DS,MAX}} C(V_{DS})d^2{V_{DS}}^2 \quad (5)$$

This method can then be extended to account for variation in $V_{DS,MAX}$ due to variation in the mains voltage. This is achieved in the same manner as for miller charge calculation, namely:

$$E_{AV}(V_{DS}) = \frac{\int_0^{\pi/2} E\left(V_{DS,MAX}\sin(t)\right)dt}{\pi/2} \quad (6)$$

This expression provides this output loss per switching event, so this loss occurs twice for each device per cycle, with four devices in a single bridge, providing the total output loss per bridge:.

$$P_{OUT} = 8E_{OUT,AV} \times f_{SWITCHING} \quad (7)$$

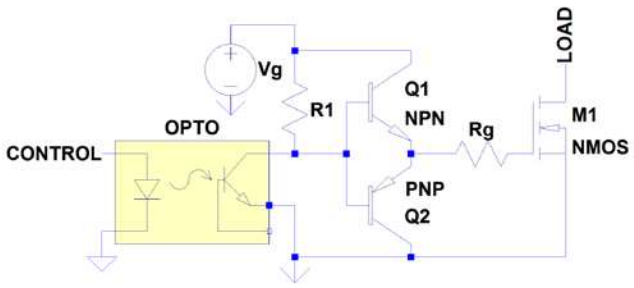

Fig. 3 The gate drive considered for the purposes of these estimations.

D. Transient Gate Drive Dissipation

While gate drives can be configured in a variety of ways, as an analytical tool the relatively simple gate drive circuit shown in figure 3 is to be used as a reference.

The transient loss of the gate drive is actually quite trivial to calculate. Figure 2 shows the gate charge-voltage curve for a MOSFET, where the area under the curve is the power dissipated in the gate. The area above the curve (bounded by $V_{GS,DRIVE}$ and $\sum Q$) indicates the energy lost in the gate drive during a switch on event. As such, the transient gate drive losses can be evaluated as:

$$E_{DRIVE,T} = \left(C_{iss}V_{GS,DRIVE} + Q_{MILLER,AV}\right) \times V_{GS,DRIVE} - E_{GATE}$$

$$P_{DRIVE,T} = 8E_{DRIVE,T} \times f_{SWITCHING}/\eta \quad (8)$$

Where η is the efficiency of the isolated DC-DC converter required to supply each gate drive, which nominally achieve 80% efficiency near maximum load.

E. Quiescent Gate Drive Dissipation

In order to evaluate the quiescent loss of the gate drive, the component values must be specified, for which a maximum switching time must be specified. The minimum time resolution of the PWM control signal utilised gives a figure for maximum switching time, but this is very conservative. In reality, a compromise can be made that will allow for slightly slower switching times at the cost of increasing output distortion. Methods used here for finding this relationship were derived from [8] and [9].

The time taken for the miller shelf to elapse was calculated, and is largely independent of the current capacity of the gate drive, being primarily governed by the maximum current through the drain. With the knowledge of the charge that needs to flow into the drain, namely the sum of the miller charge and the 'output charge', and the fact that the current will increase approximately linearly from zero to the maximum value permits calculation of the 'Miller time':

$$t_{MILLER} = \frac{2(Q_{OUT} + Q_{MILLER})}{I_{MAX}} \quad (9)$$

Some devices are not capable of switching at high frequencies due to this constraint.

Assuming that the Miller time is less than the total permitted switching period, this leaves an amount of time within which

to perform the rest of the turn off and turn on operations. The gate resistor R_G forms a RC network with the input capacitance C_{iss}, therefore the gate charges and discharges exponentially. From this the absolute maximum gate resistor, and therefore minimum peak gate current, can be calculated.

The value of gate resistance along with the maximum gate-source voltage, $V_{GS,DRIVE}$ defines the peak current requirement of the gate drive circuit. This peak current will be driven by the transistors Q1 and Q2 in figure 3. If a typical large signal gain of 100 is considered for these devices, then that defines the resistor R1 as $R_G/100$. This is a source of quiescent loss in the converter, as this resistor is continuously dissipating power.

Though it is likely to be negligible, the power dissipation in the LED with the opto-isolator device in (3) is also modelled. This gives the expression:

$$P_{DRIVE,Q} = 4N\frac{V_{GS,DRIVE}{}^2}{R1} + 2NP_{LED} \tag{10}$$

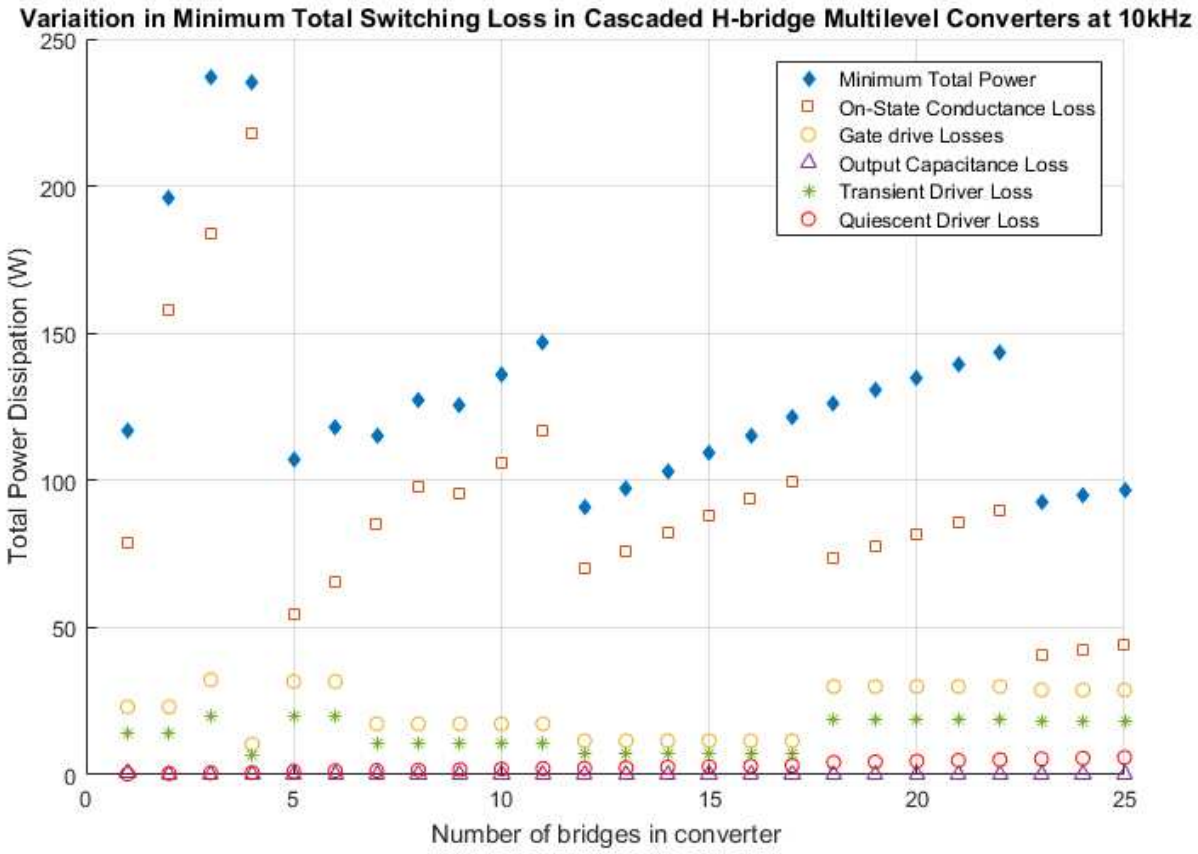

Fig. 4 Minimum losses displayed as both a total value and its component parts, with respect to increasing number of cascaded H-bridges. Evaluated at a switching frequency of 10kHz.

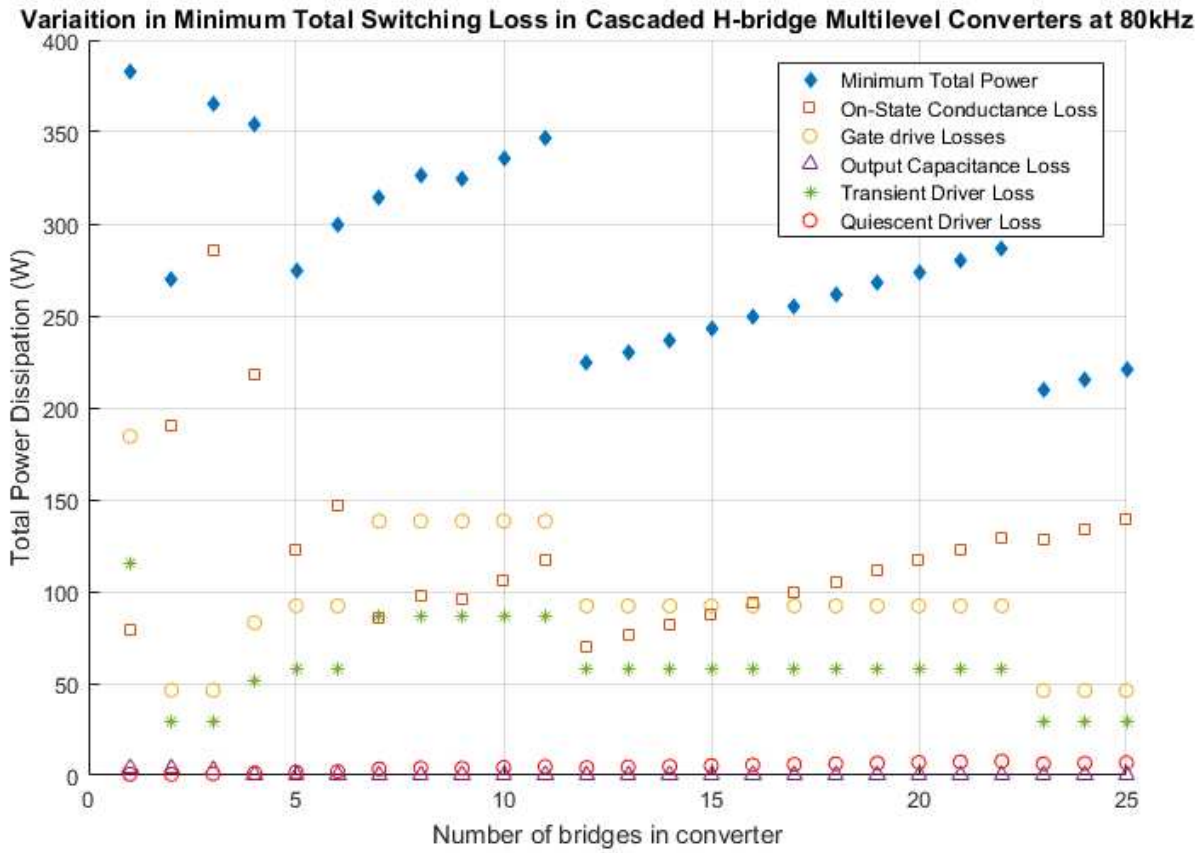

Fig. 5 Minimum losses displayed as both a total value and its component parts, with respect to increasing number of cascaded H-bridges. Evaluated at a switching frequency of 80kHz.

III. Results and Discussion

To attain the results shown in figures 4 and 5, a database of devices and device specifications was compiled. This was achieved by extracting values from datasheets for a wide range of MOSEFT devices, both at the cutting edge and otherwise. While this was not an exhaustive catalogue, more than one hundred devices representing a broad cross section were considered.

To calculate the dataset that figures 4 and 5 partially represent, the losses total losses due from all considered sources were calculated and summed for every device considered under the full range of conditions for which it was suitable (e.g. sufficiently high voltage rating). The optimal device for that case was then the device with the least power loss. The 'range of conditions' was both increasing number of cascaded bridges in the converter and increasing switching frequency.

Figures 4 and 5 are only a cross-section of the whole dataset, showing total loss for the optimal device and how it is subdivided, with respect to increasing converter order for a specific switching frequency. Figure 4 shows the results at ten kilohertz, while figure 5 shows the results at eighty kilohertz.

The first thing to notice when comparing the two datasets is that the total loss is significantly higher at higher switching frequency (i.e. figure 5), as one might expect.

There are some further interesting results shown in these figures. One of the key points being that total loss can decrease with increasing number of levels. This is due to lower voltage rated devices having greatly reduced on-state resistance, more than making up for the larger number of devices in series through the current path.

For example, there is a significant drop in total loss moving from twenty two to twenty three cascaded bridges in figure 4. This is because that crosses the threshold that enables the use of thirty volt rated MOSFETs, with an on-state resistance approaching one milliohm.

Notable in its absence is the lack of any significant output losses, this is a result of devices with large parasitics being optimised out due to the emphasis these methods place on transient dissipation. If a ZVS (zero voltage switching) solution were also considered then this would change the outcome, but a system with twenty or more cascaded ZVS full bridges seemed unlikely, and so was omitted.

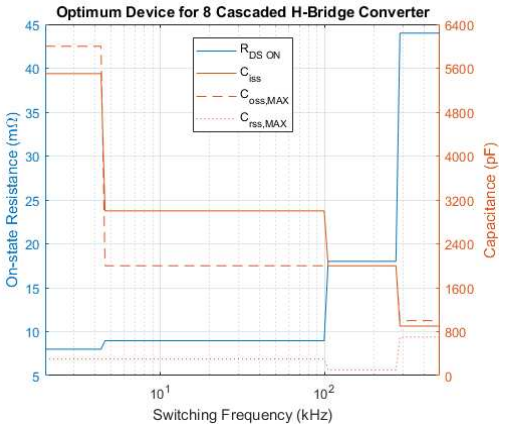

Fig. 6 Variation in optimum component properties with respect to frequency for a specific configuration.

An interesting comparison between figures 4 and 5 is the dominant source of loss. At lower frequency it is dominated by the on-state resistance, but transients dominate at higher switching frequencies.

This variation is difficult to see between figures 4 and 5 and extends over a much wider range of frequencies not shown here, but is shown in figure 6. It is clearly shown how, all else being equal, the method will tend to optimise for low on-state resistance at the expense of larger parasitics at low frequencies and vice versa at high frequencies.

IV. Conclusions

The key result, however, is that it has been shown that multilevel converters are not only a novel topology that may yield some novel benefits, such as the active cell balancing utility discussed in [2-6], but can also potentially be more efficient that their conventional counterparts. For instance, these results suggest that total loss will be lower with five cascaded H-bridges (i.e. an eleven level converter) than with a conventional single H-bridge at ten kilohertz switching frequency (see figure 4).

This is the first time that there has been a numerical comparison for a bidirectional grid-tie multilevel converter of increasing converter order. Thus enabling a transparent comparison permitting some estimation of how many levels might give the greatest benefits for a specific application.

V. Further Work

As stated at the outset, this optimisation only optimises with respect to switching loss. The design of a full system is dependent on a great many other factors such as: thermal management, EMI filtering requirements, physical footprint and not least cost.

To highlight the shortcomings of omitting cost from this analysis, for instance, the device providing extremely low loss towards the right of figure 4 costs £1 per unit, as well as its own isolated gate drive, which the converter needs nearly one hundred times over in total! Compare this with the single H-bridge requiring only four gate drives and four transistors that cost in the order of £5 each, and it becomes clear that this analysis alone is not enough to specify a real system.

While some experimental validation has already been performed to check the validity of the capacitance variation linearisation, a more extensive attempt to experimentally corroborate the predictions of this analysis would be a welcome addition.

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