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Zaidi, Z.H., Lee, K.B. orcid.org/0000-0002-5374-2767, Roberts, J.W. et al. (9 more authors) (2018) Effects of surface plasma treatment on threshold voltage hysteresis and instability in metal-insulator-semiconductor (MIS) AlGaIn/GaN heterostructure HEMTs. *Journal of Applied Physics* , 123 (18). 184503. ISSN 0021-8979

<https://doi.org/10.1063/1.5027822>

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Effects of surface plasma treatment on threshold voltage hysteresis and instability in metal-insulator-semiconductor (MIS) AlGaIn/GaN heterostructure HEMTs

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In a bid to understand the commonly observed hysteresis in the threshold voltage (V_{TH}) in AlGaIn/GaN MISHEMTs during forward gate bias stress, we have analyzed a series of measurements on devices with no surface treatment and with two different plasma treatments before the *in-situ* Al₂O₃ deposition. The observed changes between samples were quasi-equilibrium V_{TH} , forward bias related V_{TH} hysteresis and electrical response to reverse bias stress. To explain these effects a disorder induced gap state model, combined with a discrete level donor, at the dielectric/semiconductor interface was employed. TCAD modeling demonstrated the possible differences in the interface state distributions that could give a consistent explanation for the observations.

I. INTRODUCTION:

In recent years, GaN-based AlGaIn/GaN high electron mobility transistors (HEMTs) have demonstrated excellent potential for both RF and power electronics applications owing to very favorable material characteristics such as high 2DEG mobility and concentration, and a wide band gap which supports a large blocking voltage. Metal-insulator-semiconductor (MIS) structures are often preferred over Schottky gate structures in power electronics applications because of their ability to suppress the gate leakage current, engineer the threshold voltage (V_{TH}) for both depletion and enhancement mode operations, enhance the device capability to withstand larger gate voltage swing and to improve the gate-drain breakdown voltage [1-3]. There have been several successful demonstrations of various gate dielectric layers by different deposition techniques [4-11] to achieve the aforementioned objectives in AlGaIn/GaN HEMTs.

However, introducing a gate dielectric layer inserts an additional, likely non-ideal, interface in the structure which can result in charge trapping/de-trapping effects associated with the dielectric/III-nitride interface and/or the bulk dielectric itself. The dynamic charging and discharging process of these traps can affect the stability of the V_{TH} causing significant variations in switching performance. The effects can be observed through V_{TH} hysteresis in bi-directional gate transfer sweeps from below threshold to high forward bias and back again [12-17]. Previously, dynamic processes have been studied in detail using CV dispersion measurements as a function of frequency and temperature [18] and stress recovery analysis in MISHEMTs by monitoring the V_{TH} after forward gate bias [14-25]. These studies have yielded a broad distribution of stress and recovery time constants, suggesting a wide distribution of traps both at the interface and within the AlGaN barrier [16]. A very recent publication by Matys et al [26] used a disorder induced gap state (DIGS) model to explain observed V_{TH} hysteresis and reverse biased induced V_{TH} instability in MOS capacitors. However, attempts at directly comparing different surface preparations before the dielectric deposition have been limited [27]. Also, in power switching applications, GaN HEMTs are required to block large voltages in the off-state, and any V_{TH} instability in such situations can be a serious concern. There are a few reports on the influence of negative gate bias stress on the V_{TH} in recessed barrier AlGaN/GaN MISHEMTs [28] and MOS GaN FETs [29-30] but there have been no comparisons highlighting the differences between surface preparations and no attempts at consistency between forward and reverse stress models.

In terms of mitigation of these unwanted dynamic effects, using $\text{NH}_3/\text{Ar}/\text{N}_2$ or N_2 plasma to achieve surface nitridation [18-19,31-32] and oxygen plasma treatment [20] prior to dielectric deposition have been shown to be effective. In most of this past work, the focus has been on understanding the dynamic mechanisms leading to drift and/or hysteresis in V_{TH} . In practical device operation, the quasi-equilibrium value (obtained when stress-induced dynamic effects have been allowed to subside for at least 24 hours) and stability of V_{TH} , as well as its dynamical responses, are important and the effects of surface treatment prior to dielectric deposition are crucial to minimize these effects. There is no standard for stress magnitudes and times, which make it difficult to compare publications across the literature and direct comparison of different surface preparations on the same samples using a wide range of probing techniques are lacking, and consistency between all observations has still not been reported.

In this work, we have used atomic layer deposited (ALD) aluminum oxide (Al_2O_3) as a gate dielectric in AlGaN/GaN MISHEMTs because of its wide band gap (7-9eV), large conduction band offset (2.16eV), high breakdown field

(>10MV/cm) and dielectric constant (8-10) [13]. We have performed *in-situ* nitrogen (N₂) and argon (Ar) plasma treatments under the gate before deposition of the Al₂O₃ in an attempt to understand the role of both the plasma and its chemical nature. In the past, *in-situ* N₂ plasma [18-19, 31-32] and Ar plasma treatment [21] were studied separately. Here we have compared *in-situ* N₂ and Ar plasma treatments on depletion mode AlGaN/GaN MISHEMTs before the deposition of 20nm Al₂O₃ dielectric and carried out positive and negative gate bias stress measurements to evaluate the stability of the V_{TH} . We have studied the effects of high forward gate overdrive, negative gate bias stress and the shift in the quasi-equilibrium V_{TH} . We propose a model to link and explain all these observations.

II. RESULTS AND DISCUSSION

A. Experimental Details

The wafers were grown by metal organic chemical vapor deposition on 6-inch Si substrates. To facilitate the growth of Si, a nucleation layer of AlN (250nm) was used together with a series of compositionally graded carbon doped AlGaN and GaN layers. A 1nm mobility enhancement AlN layer was grown on the channel layer and an Al_{0.25}Ga_{0.75}N barrier layer of thickness 27nm grown on top of that. Finally, the wafer was capped with a 2nm undoped GaN layer. A standard device fabrication procedure was followed with mesa isolation achieved by a chlorine-based recipe in an inductively coupled plasma etching chamber. The Ohmic contacts used Ti/Al/Ni/Au metal stacks annealed at 850°C for 30 secs. After Ohmic contact formation, a 100nm SiO₂ layer was deposited using plasma enhanced chemical vapor deposition. A 1.5μm gate window was etched through the SiO₂ layer. Before the 20nm Al₂O₃ gate dielectric deposition, *in-situ* 150W N₂ plasma (referred hereafter as sample B) or 50W Ar plasma (referred hereafter as sample C) treatment for 5 minutes was performed and one sample was prepared without any treatment (referred hereafter as sample A) to serve as the reference sample. After the Al₂O₃ deposition, forming gas annealing was performed in N₂ (90%) and H₂ (10%) gas ambient at 430°C for 30 minutes. Then T-shape gates with 1μm gate field plates were defined using a Ni/Au metal stack. Finally, Ti/Au bond pads were formed on vias through the dielectric layers. Hall measurements yielded a mobility of 1909 cm²V⁻¹s⁻¹ and 2DEG density of 8.7×10¹²cm⁻².

The gate transfer characteristics of the AlGaN/GaN MISHEMTs are shown in figure 1. Starting from the virgin device, the gate transfer sweep is performed from -10V to +5V upward and then backward from +5V to -10V with V_{DS} kept at 10V. This bi-sweep is repeated two times. The V_{TH} is extracted by a linear extrapolation method. A straight line is drawn from the point of maximum transconductance along the gate transfer curve and its intercept along the x-axis defines V_{TH} . It can be seen from figure 1 (a) that in sample A (untreated) there is a positive shift in V_{TH} in the second upward sweep and a considerable hysteresis (~1.2V) in the V_{TH} . This is attributed to trapped electrons at the interface between the dielectric and III-nitride semiconductor and/or bulk dielectric traps when the gate is sufficiently positive biased to facilitate electron transfer from the

2DEG. Once the electrons are trapped, there is a delay while they emit from the traps and travel to the channel when the positive gate bias is removed. This gives rise to a time-dependent positive shift in V_{TH} or hysteresis. Regardless of the quasi-equilibrium V_{TH} , the transferred charge injected into the dielectric interface is related to the applied gate voltage above that required for real space transfer only, since the forward bias capacitance is just that due to the gate dielectric once electron transfer occurs, as indicated by the loss of gate control (figure 1). The origin of the interface traps could be due to the presence of a poor quality native oxide layer formed on the semiconductor surface, dangling bonds or interface impurities. In samples B and C, in figure 1 (b) and (c) the shift in the V_{TH} between the first and second upward sweeps and the hysteresis are both reduced compared to sample A (ΔV_{TH} from 1.2V (sample A) to 0.2V in the sample B and 0.25V in sample C). In addition, there is also a negative shift in the quasi-equilibrium V_{TH} of ~ 1.5 to 2V in both samples B and C.

B. Hysteresis

Considering the hysteresis first, the reduction in the hysteresis voltage on samples B and C compared to the sample A under the same bias sweep conditions indicates either a reduction in the number of trapped electrons and/or changes to the capture/emission dynamics. To test for a change in the number of trapped electrons, we performed hysteresis measurements as a function of forward gate bias, keeping the voltage sweep-time constant. Figure 2 shows the hysteresis increasing systematically with an incremental increase in positive gate bias above the onset voltage for real space transfer for all samples. The lack of saturation of the hysteresis voltage with increasing bias indicates the number of interface traps exceeds the electron charge resulting from the forward gate bias for the range of biases and samples considered. In other words, all electrons migrating to the interface as a result of the forward bias are trapped there. Any net reduction in the number of interfacial traps due to the plasma treatment would have little effect on the number of trapped electrons under these conditions, provided the trap numbers still dominate. Note, however, that the slopes of the curves (below $V_{GS} = 8V$) in figure 2 are different for the samples B and C compared to sample A. To explain this figure we consider two scenarios under the assumption that the occupation of the interface traps due to the forward gate bias beyond the onset voltage for real space transfer is effectively instant (justified in figure 3). If de-trapping of the induced interface electrons after relaxation of the forward gate bias to zero is slow relative to the measurement cycle then the trapped electrons at the interface are effectively fixed. A voltage redistribution occurs across the dielectric and AlGaN barrier and the measured hysteresis will be close to the forward bias above the onset voltage for real space transfer. This will result in a slope approaching unity. On the other hand, if the trapped charge relaxes quickly relative to the measurement cycle, or if there are no traps, then no hysteresis will be observed, resulting in a slope of zero in figure 2. Hence, the slopes in figure 2 ($0 < \text{slope} < 1$) confirm a decrease in the trapped electron emission times (decreased slope) as a result of the plasma treatment. This observation is reinforced by the tapering of

the hysteresis voltage observed near the end of the measurement (above $V_{GS} = 8V$) in samples B and C compared to sample A, which indicates significant emission of trapped electrons during the full forward and reverse bias measurement time (~50 sec). However, the emission and transport pathway for electrons from the interface to the 2DEG channel through, or over, the AlGaIn barrier is expected to be unchanged between the samples A, B and C. A possible reason for the decreased emission time could be that a greater proportion of trapped electrons occur near the conduction band of the AlGaIn barrier, enabling these electrons to emit more easily into the conduction band or gain an energy advantage during the hopping transport through the barrier (further explanation later). Above 8 V bias in figure 2 it can be observed that the slopes become steeper. In the case of sample A, the slope tends to unity at high bias indicating that nearly all transferred electrons are trapped for the duration of the hysteresis measurement. This could be due to electrons being forced into the slower emitting traps deeper into the gate dielectric, but it is unclear why this effect is weaker in samples B and C. Over the range of devices measured, sample B with N_2 plasma treatment showed only marginally improved hysteresis compared to sample C (Ar plasma treated), indicating perhaps that nitridation [18-19,31-32] is not important under these conditions. Both N_2 and Ar plasmas, however, can be equally effective in improving the quality of gate dielectric/semiconductor interface.

We next look at the effects of increasing forward gate bias stress time. Figure 3 (a) and (b) show the positive V_{TH} shift with forward bias stress time and the measurement sequence, respectively. The devices are de-stressed with negative gate bias to restore the initial V_{TH} and the experiment is repeated with increasing gate bias stress time. The gate transfer single sweep used to measure the shift in V_{TH} takes about 25 sec to complete, at which time some relaxation of the trapped charge will occur, resulting in a possible reduction in the measured V_{TH} shift over that immediately after the forward bias stress. Despite this, the data of figure 3 indicates two distinct charging mechanisms. The initial large shift in V_{TH} after only 20 msec forward gate stress time is followed by a more gradual shift in V_{TH} with further increase in stress duration. These observations can be explained by a rapid occupation of interfacial traps occurring initially, followed by a much slower tunneling to traps within the dielectric [14-17]. The observed (slower) timescale assigned to the tunneling of electrons into the dielectric is similar for all three samples, as expected since the plasma treatment should not affect the bulk properties of the dielectric. The data is also consistent with the notion that the plasma treatment increases the speed of relaxation of the charge from the interface back to the 2DEG (low hysteresis in figure 2) where samples B and C showed a reduced shift in V_{TH} during the hysteresis measurement compared to sample A.

To gain a better understanding of the hysteresis-related relaxation process, continuous recovery times were measured in response to forward gate bias and are shown in figure 4. The device drain current was first measured with no gate bias and $V_{DS} = 1V$ to serve as a reference. V_{DS} was limited to 1V in the measurements to avoid influence due to heating effects over a prolonged duration of time (10 hours). The devices are then subjected to a high positive gate overdrive condition ($V_{GS} = +7V$, $V_{DS} = 0V$) for 1 sec. The duration of the positive gate overdrive was chosen to limit the electron charge trapping to within the semiconductor/dielectric interface and avoid charge spillover as much as possible to the slower emitting dielectric bulk traps. After the forward gate overdrive, the devices are biased back to $V_{GS} = 0V$ and $V_{DS} = 1V$ and the drain current, which reflects the changes in the 2DEG charge due to trapping in the semiconductor/dielectric interface, is measured over a period of 10 hours with a 200 msec sampling rate. The ratio of drain current before and after the gate overdrive and experimental test sequence is shown in figure 4(a) and (b) respectively. The variations in the drain current reflect the variations in trapped charge under the gate. Due to the relatively rapid sampling of the relaxation process, this method [14] greatly reduces inaccuracies in the measured V_{TH} drift. However, significant relaxation may occur for all curves within the first measurement time period (0-200 msec) [14] and the initial relaxation characteristics, therefore, cannot be resolved. For the same gate bias, the trapped charge at the instant of the removal of the bias would be the same and hence, in this case, samples B and C appear to relax more quickly compared to sample A during this initial period, in line with the differences in hysteresis. The prolonged recovery times indicates that V_{TH} instabilities can cause difficulties over a wide range of switching conditions in practical systems.

C. Reverse bias stress

Power devices are often required to withstand large blocking voltages in the off-state and any V_{TH} shift in such situations can be problematic. There are a few reports of negative gate bias stress in recessed barrier AlGaIn/GaN MISHEMTs and GaN MOS FETs [28-30]. However, there has been no comparison between different surface preparation methods and no previous attempt at the correlation with forward bias stress results. In this work, we have performed negative gate bias stress on AlGaIn/GaN MISHEMT devices both with and without plasma treatment to evaluate the stability of V_{TH} in such scenarios and gain some further insight into the differences between the samples.

The negative shift in V_{TH} of AlGaIn/GaN MISHEMTs with negative gate bias stress time using $V_{GS} = -10V$ is shown in figure 5 (a) along with the experimental sequence (figure 5 (b)). In this experiment, virgin devices are initially swept from -10V to 0V to record the initial V_{TH} and then negative gate bias ($V_{GS} = -10V$) is applied for 0.02 sec. After that, devices are swept from -10V to 0V to record the shift in the V_{TH} . The experiment is then repeated with increased negative gate bias stress time.

Figure 5 (a) shows the shift in V_{TH} as a function of stress time, which is due to the transport of electrons from the dielectric/semiconductor interface towards the channel. The shift is considerably greater in sample A compared to samples B and C. Contrary to the results for positive gate bias stress, the charge adjustment under negative bias stress is much slower than the measurement time, giving a reduced error in sampling V_{TH} shift. The difference between sample A and samples B and C after one hour stress time is $\sim 1.7V$, which is similar to the observed quasi-equilibrium V_{TH} differences (figure 1). This is most likely due to the differences in stored charge close to the quasi-equilibrium Fermi level which also gives rise to the differences in the quasi-equilibrium V_{TH} (further explanation later).

D. Model and discussion

To date, the origin of the 2DEG charge in AlGaIn/GaN heterostructures is still a conundrum. Although it is widely accepted that the surface and interface states (in MIS structures) play a vital role, the exact nature of these interface states and their distribution within the forbidden gap is still under debate. The various models were summarized and discussed by Bakeroot et al [33]. Each model has its own limitations but may explain behavior within limited specific conditions.

The unified disorder induced gap states (DIGS) model [26, 34-35] has often been utilized to explain different V_{TH} hysteresis behaviors. This model divides the U-shaped interface state density into donor- and acceptor-like states separated by the charge neutrality level (E_{CNL}) [34] with the Fermi level (E_F) close by (figure 6(a)). Although the DIGS model can explain the formation of the 2DEG, some additional discrete donor-like interface states, particularly those which have been associated with nitrogen vacancies [36], may still be needed to explain the 2DEG variation with barrier thickness and composition, and to place E_F above E_{CNL} [33, 36]. The latter is a requirement for our model. Therefore, to help establish the charge details at the interface as a result of the plasma treatments, we used SENTAUROS TCAD to simulate a DIGS model together with discrete donor states associated with nitrogen vacancies, 0.37eV below the conduction band [36], to explain our three main experimental observations after plasma treatment. These are 1) the negative shift in the quasi-equilibrium V_{TH} ($\sim 2V$), 2) the faster emission rates (reduced hysteresis) and 3) the reduced negative shift in V_{TH} during negative gate bias stress in samples B and C compared to sample A.

Figure 6 (a) shows the distribution of interface states along with the energy levels used in the simulation to represent the plasma treated (samples B and C) and reference (sample A, higher interface state density) samples. The number of discrete

donors and the magnitude of the DIGS distribution was chosen to yield the experimental 2DEG concentrations. The discrete donors are necessary to place the Fermi level above E_{CNL} (required in the model) but should not be large enough in number to pin the Fermi level at that point. However, many concentration combinations of DIGS and discrete donor levels will give the correct value of the 2DEG. Here we are mostly interested in the relative values of the DIGS density to model the observed electrical differences between the samples, so the discrete donor number is kept constant. We excluded the 1nm thick AlN mobility enhancement layer in our model since it is unlikely to make any significant difference to our explanation. An E_{CNL} value of 1.78eV, as calculated by Mönch [37], was used. Due to the presence of the discrete donor states, the Fermi level position is slightly above the E_{CNL} level and donor-like states below the E_{CNL} level are considered frozen or fixed, i.e. they remained neutral (occupied) throughout, under all bias conditions considered [35]. The rationale for this assumption is that the emission time constants associated with states below mid-band gap in AlGaN can be very large ($10^{12} - 10^{20}$ sec) [35] and therefore are unlikely to change charge state in the gate transfer measurements. This is also borne out by the medium-term stability of the reverse gate biased pinch-off condition in normal HEMT operation.

From charge neutrality under zero gate bias, the 2DEG charge per unit area, n_s , formed as a result of this model is given by

$$n_s = N_D^+ - N_A^- \quad (1)$$

where N_D^+ the ionized donor density per unit area (here assigned to nitrogen vacancies) and N_A^- is the occupied acceptor-like state density between the Fermi level and E_{CNL} ($N_D^+ > N_A^-$). To explain the experimental observations we assume that the plasma treatment reduces the density of the U-shaped distribution of interface states, and hence the number of negatively charged acceptor states below the Fermi level, N_A^- , is reduced. Whilst the shift in n_s and hence the quasi-equilibrium V_{TH} with the plasma treatment can also be explained by simply increasing the discrete donor states in equation 1, the explanation of the hysteresis and reverse bias observations require changes in the acceptor-like state densities [33, 35].

Figure 6 (b) shows the modeled results as described above compared with the experimental gate transfer characteristics for sample A and sample B and C. Reasonable agreement is obtained. The lower transconductance in the measured devices is perhaps due to the influence of interface scattering which degrades the mobility and this effect is excluded in the simulation. In our model, the $\sim 2V$ negative shift in the quasi-equilibrium V_{TH} after plasma pretreatment is the manifestation of the reduced DIGS acceptor states density, N_A^- , in equation 1. The conduction band diagram of sample A under $V_{GS}=0V$ (equilibrium) and $V_{GS}=-10V$ showing the charge transfer mechanism is in figure 7. In the equilibrium condition, occupied acceptor states are below the Fermi level (red color in figure 7) and, as the gate is swept to $V_{GS}=-10V$ during measurement,

these acceptor states are lifted above the Fermi level (black color in figure 7). However, the emission time constants of electrons in these acceptor states are such that they are unable to emit during the gate transfer sweep and so behave as fixed negative states in sample A. The presence of these additional acceptor states over and above those in samples B and C results in the V_{TH} difference of $\sim 2V$. However, when the negative gate bias is applied for a long enough time such as in the reverse bias stress measurements of figure 5(a), the electrons in these acceptor states are able to reach the 2DEG channel (figure 5(a)) via hopping through the AlGaN barrier traps and/or emission into the barrier conduction band (figure 7). After nearly one hour negative gate bias stress ($V_{GS} = -10V$), the V_{TH} difference between sample A and samples B and C is $\sim 1.7V$ as seen in the figure 5(a) which is equal to the difference in the equilibrium V_{TH} , reflecting the extra charge transfer in sample A. As stated previously, the donor-like states below E_{CNL} are considered too slow to take part in the reverse bias transients.

When the gate is sufficiently forward biased, the acceptor-like states above the Fermi level are filled with electrons and are responsible for the V_{TH} hysteresis in bi-directional gate transfer sweeps (figure 1). Under the forward bias condition, to trap the same amount of charge (fixed forward bias voltage) more states closer to the conduction band would get filled in samples B and C compared to sample A, as shown by the red and black shading in figure 8. This difference in the occupation distribution of interface acceptor-like states can lead to faster electron emission in samples B and C, together with reduced hysteresis.

Our model requires a decrease in the DIGS as a result of the plasma treatment, which is opposite to that measured by Yatabe *et al* [38]. However, there are major differences in the latter's plasma etching conditions compared to ours. In our case, the plasma is chemically inert, occurs *in-situ* with the ALD oxide deposition and the power and energy are chosen to minimize etching and therefore crystal damage. X-Ray photoelectron spectroscopy measurements indicate that cleaning of the surface (reducing O-C bonds) is the dominant factor to improve the interface quality.

III. CONCLUSIONS

We have developed a model to explain the main electrical differences resulting from untreated and plasma treated surfaces in MISHEMTs. Despite the uncertainty in the interface state density and distribution, we have been able to use the DIGS model combined with discrete donors to explain consistently the observed changes in quasi-equilibrium V_{TH} , hysteresis and gate bias stress (forward and reverse) resulting from different pre-deposition surface preparations. A decrease in the overall DIGS state distribution due to the plasma treatment is sufficient to explain the range of experimental observations.

These measurements and analyses add further insight into the mechanisms affecting V_{TH} instabilities but indicate that the elimination of these effects relates to the significant reduction in interface states.

ACKNOWLEDGMENT

This work was funded by the UK Engineering and Physical Sciences Research Council under grant codes EP/K014471/1 and EP/N01202X/1

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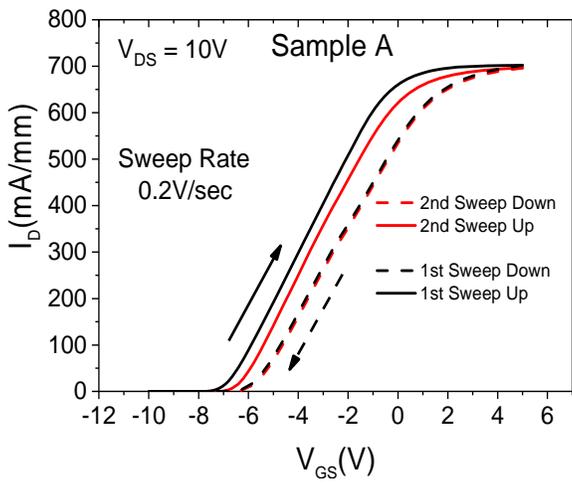
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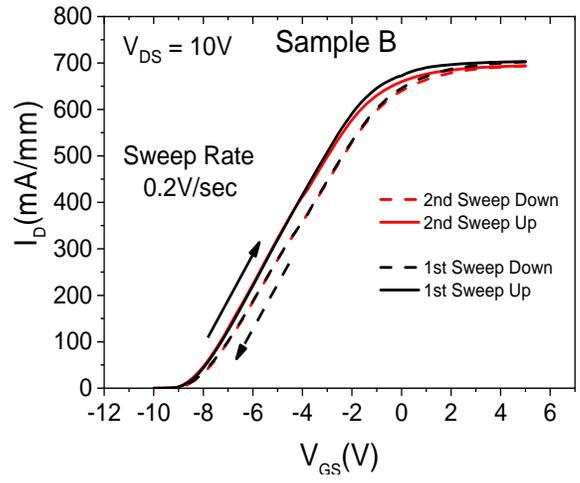
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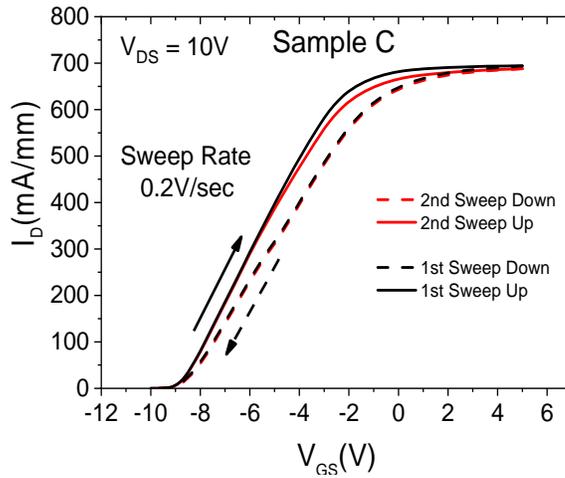
FIGURES



(a)



(b)



(c)

Figure 1. The gate transfer characteristics of AlGaIn/GaN MISHEMTs with (a) sample A (Reference) (b) sample B (*in-situ* N_2 plasma treatment) and (c) sample C (*in-situ* Ar plasma treatment).

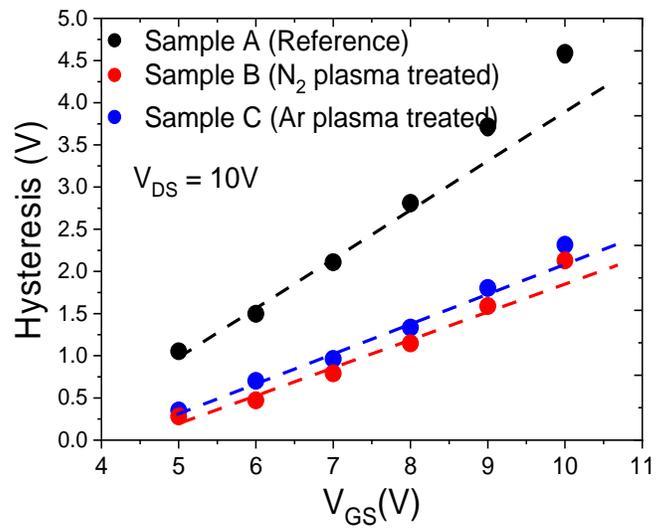
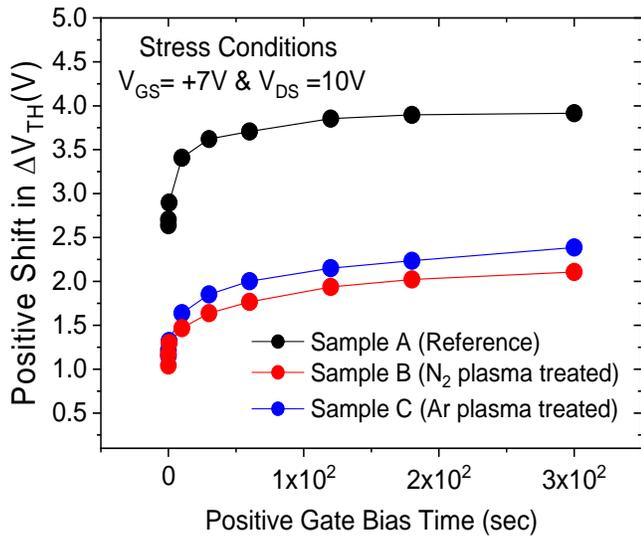
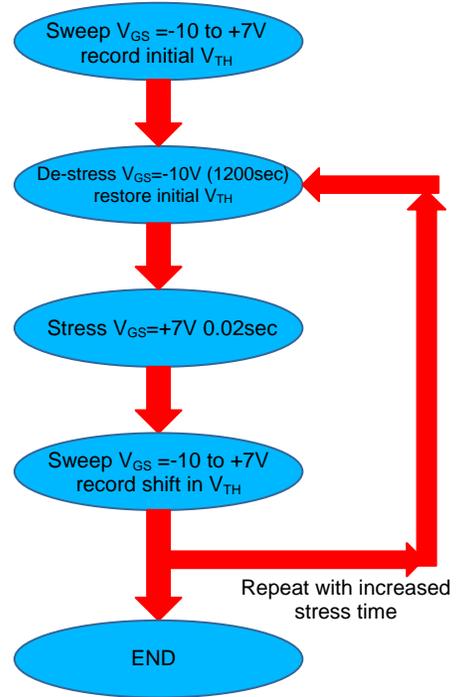


Figure 2. The build up of hysteresis with increase in the positive gate bias voltage.

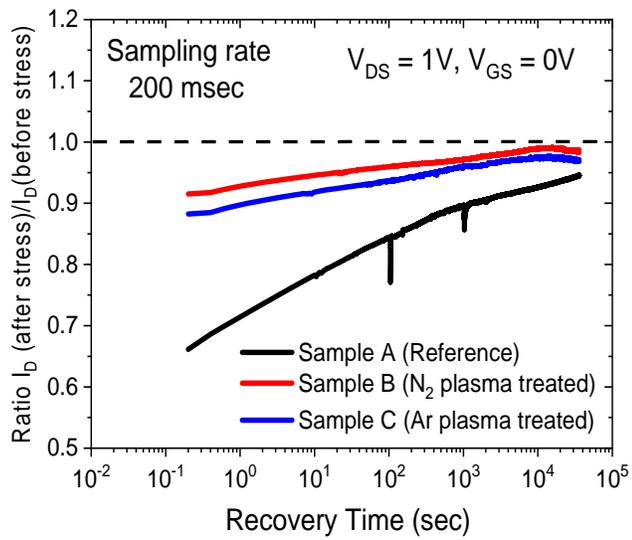


(a)

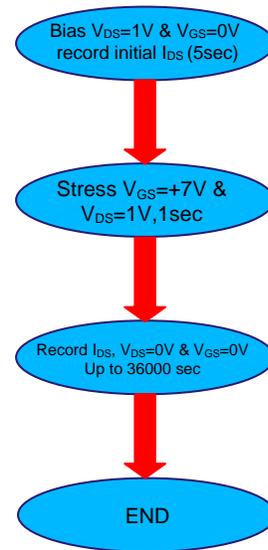


(b)

Figure 3. (a) The positive shift in V_{TH} with positive gate bias stress time (b) experimental test sequence.

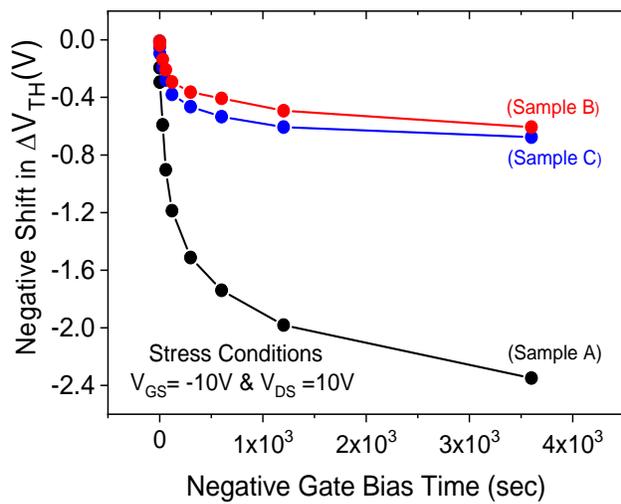


(a)

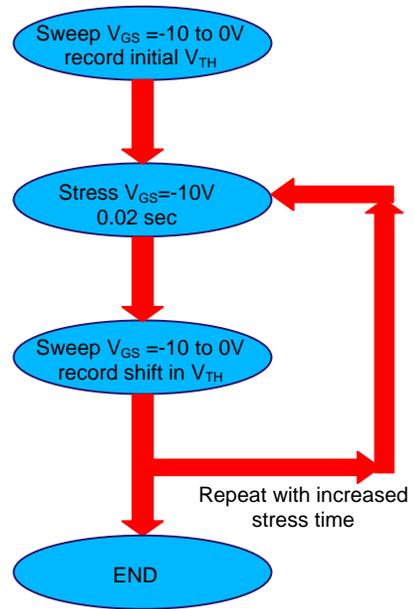


(b)

Figure 4. (a) The drain current recovery time after 1 sec $V_{GS}=+7V$ stress (b) experimental test sequence.

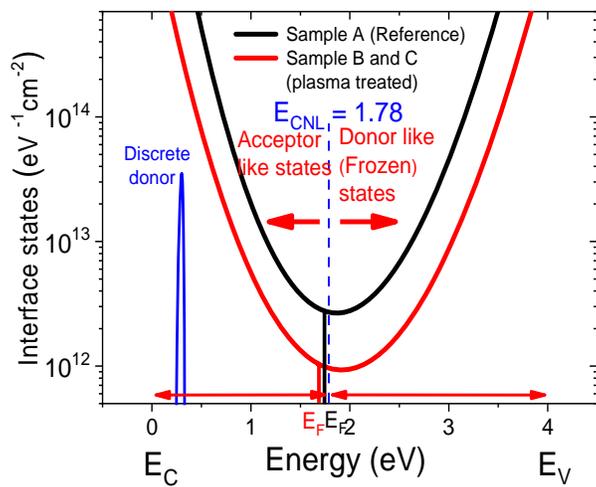


(a)

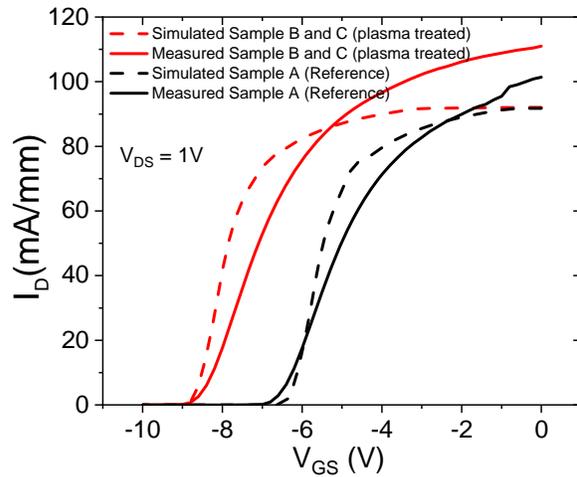


(b)

Figure 5. (a) The negative shift in V_{TH} with negative gate bias stress and (b) experimental test sequence.



(a)



(b)

Figure 6. (a) The distribution of interface states used in the model (b) Modelled and measured gate transfer sweep of sample A (reference) and samples B and C (plasma treated).

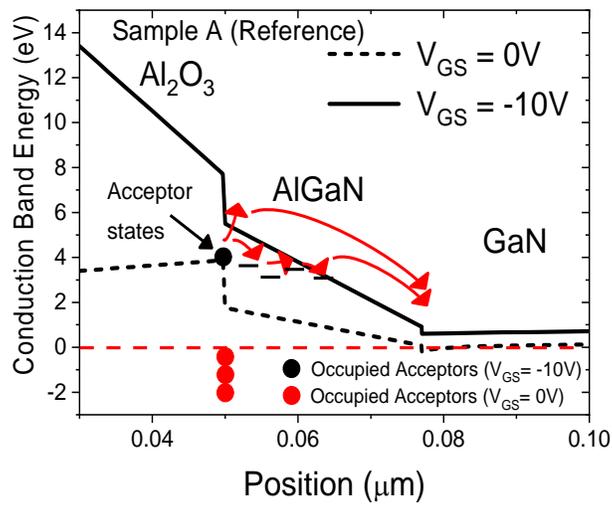


Figure 7. Conduction band diagram of sample A (reference) at $V_{GS} = 0$ and $-10V$ showing the electron transfer mechanism.

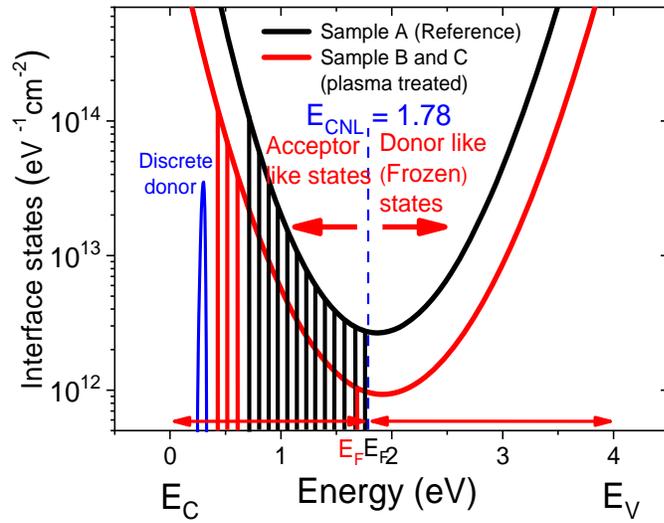


Figure 8. Filling of acceptor like states in sample A (black lines) and sample B and C (red lines) to accommodate same amount of charge (+7V) under the forward gate bias condition.