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Current-limiting DC/DC Power Converters

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***Abstract*—A new nonlinear control framework that guarantees the desired regulation (voltage, current or power) with an inherent current-limiting capability for different types of dc/dc power converters is presented in this paper. This framework is based on the idea of applying a virtual resistance in series with the inductor of the converter, which changes according to nonlinear dynamics that depend on the control task. Without requiring any knowledge of the converter inductance, capacitance or the load, the controller structure is appropriately formulated for each power electronic system based on the nonlinear model of the converter. Using input-to-state stability theory, it is proven that the inductor current remains below a maximum value at all times, even during transients, independently from load and input voltage variations. This offers an inherent current-limiting property of the converter under faults, input voltage sags and unrealistic power demands without the need of external protection mechanisms, saturation units or current limiters. Extensive simulation and experimental results validate the effectiveness of the proposed control scheme and its current-limiting property, with comparison to traditional control strategies.**

***Index Terms*—dc/dc converters, nonlinear control, current-limiting property, protection, faults**

I. INTRODUCTION

DC/DC power converters play a key role in various emerging applications including photovoltaic systems [1], [2], wind power systems [3], electric vehicles [4], dc micro-grids [5], etc, where a voltage, current or power regulation is required and therefore a wide variety of control techniques has been proposed in the literature to achieve the desired regulation scenario. Traditional control methods introduce a Proportional-Integral (PI) controller designed based on the small-signal model of the converter [6], [7]. PI controllers are applied in a single or cascaded structure and often in combination with more advanced control methods [8]. In recent works, several of these methods have been implemented using sliding control [9] or model predictive control [10] to guarantee precise output voltage regulation under a control input constraint, which is represented by the duty ratio of the converter.

Using the average nonlinear dynamic model of the dc/dc converters [11], several nonlinear control methods have been designed to achieve the desired voltage or current regulation and guarantee the stability of the closed-loop system [12], [13]. Passivity-based controllers have been effectively applied to dc/dc converters supported by a rigorous proof of stability [14], and are often combined with the traditional PI control [15]. However, most of the existing control methods for dc/dc converters require accurate knowledge of the converter parameters (inductance, capacitance) or the load to guarantee nonlinear stability, which can change during the operation. More robust versions of dc/dc power converter control include the interconnection and damping assignment passivity-based control [16], hybrid control [17] or H_∞ and μ-synthesis [18]. Since modern load types introduce complex dynamics (usually nonlinear) that can increase the nonlinearities and the number of the system states, there is a need for advanced controllers that act independently from the system parameters and guarantee the stable operation of the converter at all times.

Except from the theoretical proof of stability, the dc/dc power converters must be protected at all times and satisfy some technical limitations, e.g. limited converter current, especially during transients, faults and unrealistic power demands. Although this can be achieved using additional fuses and relays [19], there is increased interest in designing control methods that can guarantee a current-limiting property [20]. These control strategies change the original control structure to the current-limiting structure or introduce saturation units [7]. However, traditional current-limiting methods have two major drawbacks: i) closed-loop stability cannot be analytically guaranteed for the nonlinear accurate model of the converter and ii) traditional controllers with saturation units cannot maintain a limited current during transients and can suffer from integrator windup issues that may lead to instability [7], [21]. Hence, the design of a single control structure that can regulate all main types of dc/dc converters without any knowledge of the system or load parameters and guarantee stability and a given current limitation at all times, even during transients, is of significance.

In this paper, a new nonlinear control framework that can be applied to all main types of dc/dc converters and acts independently from the converter and load parameters is proposed to guarantee an inherent current limitation. The proposed control strategy applies a dynamic virtual resistance in series with the converter inductor which varies based on a nonlinear dynamical system. Using input-to-state stability (ISS) theory [22], it is shown that the inductor current never violates a maximum limit, independently from the desired regulation scenario (voltage, current or power regulation). The current-limiting property is extended to cases of faults in the input or output of the converters. Although different current-limiting controllers have been recently designed for inverters and rectifiers [23], a generic concept for any type of dc/dc converter that achieves current limitation without suffering from integrator windup and instability has not been yet proposed. The proposed work introduces for the first time a framework that does not focus on a particular converter but is applied to a family of converters and is further extended to maximize power capacity utilization under faulty conditions, opposed to the existing previously mentioned techniques for rectifiers, inverters and specific types of dc/dc converters [24]. Extensive simulation and experimental results are presented to verify the desired operation of the proposed strategy and the current-limiting capability under both normal and abnormal conditions compared to existing current-limiting methods.

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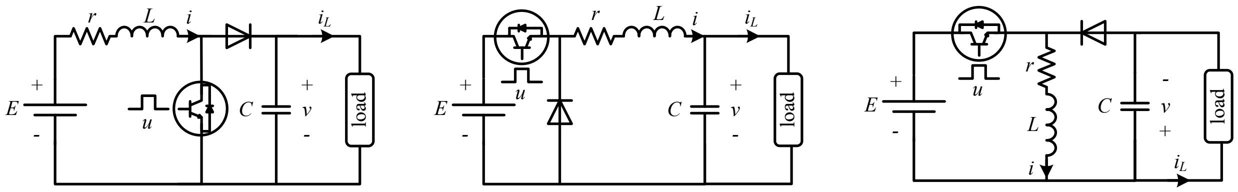

$$L\frac{di}{dt} = -ri-(1-u)v+E \quad (1)$$
$$C\frac{dv}{dt} = (1-u)i-i_L \quad (2)$$
(a)

$$L\frac{di}{dt} = -ri-v+uE \quad (3)$$
$$C\frac{dv}{dt} = i-i_L \quad (4)$$
(b)

$$L\frac{di}{dt} = -ri-(1-u)v+uE \quad (5)$$
$$C\frac{dv}{dt} = (1-u)i-i_L. \quad (6)$$
(c)

Figure 1. Schematic diagram and dynamic model for main types of dc/dc power converters: (a) boost, (b) buck and (c) buck-boost

II. Dynamic model of dc/dc power converters

All main types of power converters (boost, buck and buck-boost) consist of an inductor L with a small resistance r in series, a capacitor C, a diode and a switching element. Consider as E the dc input voltage, i the inductor current, v the output voltage and i_L the load current. The schematic diagrams of the different dc/dc power converters are shown in Fig. 1. In practice, there exists a conduction voltage drop in the diode component, but its value is very small and is often neglected. Depending on the inductor current waveform, dc/dc converters operate in continuous (CCM) or discontinuous (DCM) conduction mode. CCM can be accomplished using a high switching frequency or a larger inductor value L. Assuming CCM operation, the nonlinear average dynamic model of each dc/dc converter can be obtained, where the control input is defined as the duty-ratio $u \in [0,1]$ and allows the investigation of control design and stability analysis [11]. Hence, the boost, buck and buck-boost converter dynamics are given from (1)-(2), (3)-(4) and (5)-(6), respectively. Similarly, the average model of different dc/dc converters can be obtained, e.g. the flyback converter dynamics can be obtained from the buck-boost converter equations (5)-(6) if one replaces v with nv in (5) and i with ni in (6), where n is the winding ratio of the equivalent isolation transformer.

Note that when $u=1$, both the boost and the buck-boost converters result in a very high inductor current (equal to $\frac{E}{r}$ at the steady state). Maintaining the inductor current limited and particularly below a given value is a crucial property that should be guaranteed at all times for the protection of the converter, i.e. under transients and faults. To this end, in the sequel, a controller that can achieve different regulation tasks and inherits a current-limiting property is investigated.

III. Nonlinear control design and analysis

A. Control framework

Since the main task is to achieve a desired regulation scenario (voltage, current or power regulation) together with a current limitation for each dc/dc power converter, a new control design framework is proposed in this paper that introduces a dynamic virtual resistance w in series with the inductor of the converter which partially decouples the dynamics of the input current. Hence, independently from the type of converter, the goal is to achieve the closed-loop inductor current equation:

$$L\frac{di}{dt} = -(r+w)i+E, \quad (7)$$

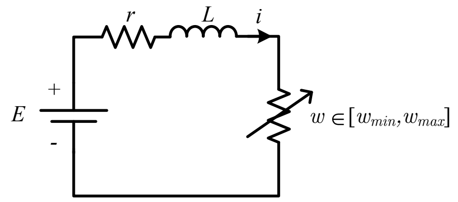

Figure 2. Equivalent circuit of the closed-loop current dynamics

from which it is clear that the proposed controller introduces a dynamic virtual resistance w in series with the inductor L and its small parasitic resistance r, as shown in Fig. 2.

In order to follow this framework and accomplish the desired task, the duty-ratio control input of each dc/dc power converter is proposed to take the form described in Table I. Similarly, for the case of the flyback converter, the control input can be defined as $u = 1 - \frac{wi}{nv+E}$. Hence, for different types of dc/dc converters, the control input u can be calculated to result in the closed-loop inductor current equation (7).

Table I
Proposed control laws for dc/dc converters

	boost	buck	buck-boost
duty-ratio u	$1-\frac{w}{v}i$	$1+\frac{v}{E}-\frac{w}{E}i$	$1-\frac{w}{v+E}i$

B. Design of the virtual resistance w

If the virtual resistance is designed to stay within a given range, then the inductor current can be limited below a desired value. There are many ways to design the virtual resistance to meet this goal, e.g. using saturated integrators, but may lead to integrator windup and instability. Inspired by the recently developed bounded integral control (BIC) method in [13], here the BIC structure is adopted in order to guarantee the boundedness of w. In this paper, the BIC is applied to the virtual resistance w and not directly to the control input u, as suggested in [13]. Hence, further analysis regarding the converter stability and current-limiting properties is required.

As a result, the virtual resistance w is designed to change according to the nonlinear second-order dynamics

$$\begin{bmatrix}\dot{w}\\ \dot{w}_q\end{bmatrix} = \begin{bmatrix}0 & -cw_q g(E,i,v,i_L)\\ \frac{cw_q g(E,i,v,i_L)}{\Delta w_m^2} & -k_q\left(\frac{(w-w_m)^2}{\Delta w_m^2}+w_q^2-1\right)\end{bmatrix}\begin{bmatrix}w-w_m\\ w_q\end{bmatrix} \quad (8)$$

with c, k_q, w_m, Δw_m being positive constants with $w_m > \Delta w_m$ and $g(E,i,v,i_L)$ being a smooth function that describes the desired regulation scenario, i.e. $g(E,i_e,v_e,i_{Le}) = 0$ at the desired equilibrium point. For example, when the

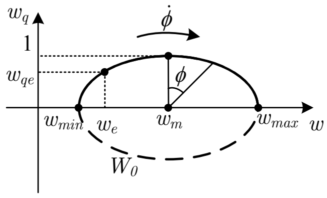

Figure 3. Phase portrait of the controller dynamics

control task is the output voltage regulation to a reference value v_{ref}, then $g(E,i,v,i_L) = v_{ref} - v$. Equivalently, this function can take the form $g(E,i,v,i_L) = i_{ref} - i$ for current regulation, $g(E,i,v,i_L) = P_{ref} - vi_L$ for power regulation, etc. The initial conditions w_0 and w_{q0} are required to satisfy $\frac{(w_0-w_m)^2}{\Delta w_m^2} + w_{q0}^2 = 1$; thus a typical choice is $w_0 = w_m$, $w_{q0} = 1$.

To investigate the nonlinear controller dynamics of w and w_q, consider the following Lyapunov function candidate

$$W = \frac{(w-w_m)^2}{\Delta w_m^2} + w_q^2. \tag{9}$$

The time derivative of W becomes

$$\dot{W} = -2k_q\left(\frac{(w-w_m)^2}{\Delta w_m^2} + w_q^2 - 1\right)w_q^2. \tag{10}$$

According to the initial conditions, it yields

$$\dot{W} = 0, \Rightarrow W(t) = W(0) = 1, \forall t \geq 0,$$

which means w and w_q will start and remain on the ellipse

$$W_0 = \left\{ w, w_q \in R: \frac{(w-w_m)^2}{\Delta w_m^2} + w_q^2 = 1 \right\} \tag{11}$$

as shown in Fig. 3. Since the controller states are restricted on W_0, then $w \in [w_{min}, w_{max}] = [w_m - \Delta w_m, w_m + \Delta w_m], \forall t \geq 0$. By considering the mathematical transformation $w = w_m + \Delta w_m \sin\phi$ and $w_q = \cos\phi$, then one can easily prove that w and w_q will move on the ellipse W_0 with an angular velocity given by

$$\dot{\phi} = \frac{c w_q g(E,i,v,i_L)}{\Delta w_m}. \tag{12}$$

Hence, assuming that the desired regulation scenario is accomplished, i.e. $g(E,i,v,i_L) = 0$, the angular velocity becomes zero and the controller states can converge to two constant values w_e and w_{qe} (proof is given in Subsection III-D). Since $w_m > \Delta w_m > 0$, the ellipse W_0 is located on the right-half plane and $w \in [w_{min}, w_{max}] > 0, \forall t \geq 0$, resulting in a positive dynamic virtual resistance.

According to (12), the angular velocity $\dot{\phi}$ becomes zero on the horizontal axis, i.e. when $w_q = 0$ and $w = w_{min}$ or $w = w_{max}$. This is desirable to avoid a possible oscillating behavior of the controller dynamics around the ellipse W_0 on the $w-w_q$ plane. In order to further explain this, assume that during a transient, the controller states try to reach the horizontal axis. Then $w_q \to 0$ which means that $\dot{\phi} \to 0$ independently from the function $g(E,i,v,i_L)$. Thus, the controller states slow down until the angular velocity changes sign. As a result, w and w_q cannot travel around the ellipse W_0 and, based on the initial conditions, they will be restricted either on the upper or the lower semi-ellipse of W_0 as shown in Fig. 3.

Furthermore, at the limits of the virtual resistance, i.e. when $w \to w_{min}$ and $w \to w_{max}$, since $w_q \to 0$, then from (8) there is $\dot{w} \to 0$, which means that the integration slows down independently from the function $g(E,i,v,i_L)$. This indicates an inherent anti-windup property of the proposed controller which smoothly slows down the integration near the limits, opposed to the case of using a saturated integrator.

C. Current-limiting property

For system (7), consider the energy stored in the inductor

$$V = \frac{1}{2}Li^2.$$

The time derivative of V is calculated as

$$\dot{V} = Li\frac{di}{dt} = -(r+w)i^2 + Ei \leq -(r+w_{min})i^2 + E\,|i|\,,$$

taking into account that $w \geq w_{min} > 0$, $\forall t \geq 0$. Hence, for every $0 < \theta < 1$ there is

$$\begin{aligned}\dot{V} &\leq -(1-\theta)(r+w_{min})i^2 - \theta i^2 + E\,|i| \\ &\leq -(1-\theta)(r+w_{min})i^2,\ \forall\,|i| \geq \frac{E}{\theta(r+w_{min})},\end{aligned}$$

which means that system (7) is ISS, where E is the dc input voltage [22]. Since E is constant (or bounded), according to the ISS property:

$$\dot{V} < 0, \forall\,|i| > \frac{E}{r+w_{min}}.$$

As a result, if initially $|i(0)| \leq \frac{E}{r+w_{min}}$, then

$$|i(t)| \leq \frac{E}{r+w_{min}}, \forall t \geq 0. \tag{13}$$

If w_{min} is selected as

$$w_{min} = \frac{E}{i_{max}}, \tag{14}$$

where i_{max} denotes the maximum allowed current of the converter, then by substituting (14) into (13), there is

$$|i(t)| \leq \frac{i_{max}}{\frac{ri_{max}}{E}+1} < i_{max}, \forall t \geq 0, \tag{15}$$

which guarantees the desired current-limiting property.

Assuming a constant (or bounded) input voltage E, the current limitation results in a power limitation of all converter types: i) for the boost converter $P = Ei \leq Ei_{max}$ and ii) for the buck or buck-boost converter $P = Eui \leq Ei_{max}$, given a maximum value i_{max}. Due to the small resistance r, current i is limited slightly below i_{max} from (15). To overcome this issue, w_{min} can be selected as $w_{min} = \frac{E}{i_{max}} - r$ instead of (14), however (14) is preferred since the current limitation is still guaranteed and the controller does not require the value of r, which might not be accurately known. Note that the ISS and the current-limiting property are guaranteed independently from the output voltage dynamics or the load, which is a unique property of the proposed controller.

D. Asymptotic stability

The current limitation has been guaranteed independently from i_L, which can represent the current of any voltage-controlled load, i.e. $i_L = f(v)$. For the asymptotic stability, the case with a resistive load R is considered for simplicity, i.e. $i_L = \frac{v}{R}$, although a similar procedure can be followed for any voltage-controlled load (e.g. power converter-fed load [25]). Let the closed-loop state vector $x = \begin{bmatrix} i & v & w & w_q \end{bmatrix}^T$. For any value of the virtual resistance $w_e \in (w_{min}, w_{max}) > 0$, consider the equilibrium point $x_e = \begin{bmatrix} i_e & v_e & w_e & w_{qe} \end{bmatrix}^T$, where for any dc/dc converter $i_e = \frac{E}{r+w_e} > 0$ from (7), $v_e > 0$ and $\frac{(w_e - w_m)^2}{\Delta w_m^2} + w_{qe}^2 = 1$ with $w_{qe}^2 > 0$. Then, the Jacobian matrix for any converter becomes

$$J = \begin{bmatrix} J_1 & 0_{3\times1} \\ J_2 & -2k_q w_{qe}^2 \end{bmatrix}.$$

Since $k_q > 0$ and $w_{qe}^2 > 0$, then J is Hurwitz if J_1 is Hurwitz where

$$J_1 = \begin{bmatrix} -\frac{r+w_e}{L} & 0 & -\frac{E}{L(r+w_e)} \\ a & -\frac{1}{RC} - b & d \\ -cw_{qe}^2 \left.\frac{\partial g}{\partial i}\right|_{x=x_e} & -cw_{qe}^2 \left.\frac{\partial g}{\partial v}\right|_{x=x_e} & 0 \end{bmatrix}.$$

Note that for the boost converter $a = \frac{2w_e E}{Cv_e(r+w_e)}$, $b = \frac{w_e E^2}{Cv_e^2(r+w_e)^2}$, $d = \frac{E^2}{Cv_e(r+w_e)^2}$, for the buck converter $a = \frac{1}{C}$, $b = d = 0$ and for the buck-boost converter $a = \frac{2w_e E}{C(v_e+E)(r+w_e)}$, $b = \frac{w_e E^2}{C(v_e+E)^2(r+w_e)^2}$, $d = \frac{E^2}{C(v_e+E)(r+w_e)^2}$. Thus, in every case $a > 0$ and $b, d \geq 0$. The characteristic equation of the system becomes

$$\lambda^3 + \left(\frac{r+w_e}{L} + \frac{1}{RC} + b\right)\lambda^2 + \alpha_1\lambda + \alpha_0 = 0,$$

where

$$\alpha_1 = \frac{r+w_e}{L}\left(\frac{1}{RC} + b\right) + cdw_{qe}^2 \left.\frac{\partial g}{\partial v}\right|_{x=x_e} - cw_{qe}^2 \frac{E}{L(r+w_e)} \left.\frac{\partial g}{\partial i}\right|_{x=x_e}$$

$$\alpha_0 = cw_{qe}^2\left(d\frac{r+w_e}{L} - a\frac{E}{L(r+w_e)}\right)\left.\frac{\partial g}{\partial v}\right|_{x=x_e} - cw_{qe}^2 \frac{E}{L(r+w_e)}\left(\frac{1}{RC}+b\right)\left.\frac{\partial g}{\partial i}\right|_{x=x_e}.$$

Using the Ruth-Hurwitz criterion, since $\frac{r+w_e}{L} + \frac{1}{RC} + b > 0$, then J_1 will be Hurwitz and equivalently x_e will be asymptotically stable if the following condition is satisfied:

$$\left(\frac{r+w_e}{L} + \frac{1}{RC} + b\right)\frac{r+w_e}{L}\left(\frac{1}{RC} + b\right) + cw_{qe}^2 h > 0, \quad (16)$$

where

$$h = \left[d\left(\frac{1}{RC} + b\right) + \frac{aE}{L(r+w_e)}\right]\left.\frac{\partial g}{\partial v}\right|_{x=x_e} - \frac{E}{L^2}\left.\frac{\partial g}{\partial i}\right|_{x=x_e}.$$

Typically $\left.\frac{\partial g}{\partial v}\right|_{x=x_e} \leq 0$ and $\left.\frac{\partial g}{\partial i}\right|_{x=x_e} \leq 0$ ($g = v^{ref} - v$ for voltage regulation, $g = i^{ref} - i$ for current regulation). Hence, for a current regulation scenario there is $\left.\frac{\partial g}{\partial v}\right|_{x=x_e} = 0$, $\left.\frac{\partial g}{\partial i}\right|_{x=x_e} = -1$ and therefore (16) always holds true independently from the converter type. For a different regulation scenario, if $h < 0$, then the controller gain c should satisfy the inequality

$$c < \frac{(r+w_e)(1+bRC)(rRC + w_eRC + L + bRLC)}{w_{qe}^2 (RLC)^2 \,|h|}. \quad (17)$$

Since $w_e \in (w_{min}, w_{max}) > 0$, then controller gain c can be suitably defined such that (17) is satisfied for any $w_e \in (w_{min}, w_{max})$, where $w_{qe}^2 = 1 - \frac{(w_e - w_m)^2}{\Delta w_m^2}$. Note that the rest of the controller parameters, i.e. w_{max}, k_q, do not affect the current-limiting property or the stability. However, since w_{min} leads to a maximum current i_{max}, similarly w_{max} will lead to a minimum inductor current i_{min}. Although i_{min} is theoretically zero, in practice a very small current flows through the parasitic elements of the converter. Hence, w_{max} can be selected as

$$w_{max} = \frac{E}{i_{min}}, \quad (18)$$

where i_{min} can be sufficiently small (mA or μA). Having defined the maximum and minimum values of the virtual resistance, then the parameters w_m and Δw_m that define the ellipse W_0 are given as

$$w_m = \frac{w_{max} + w_{min}}{2} = \frac{E(i_{max} + i_{min})}{2i_{max}i_{min}}, \quad (19)$$

$$\Delta w_m = \frac{w_{max} - w_{min}}{2} = \frac{E(i_{max} - i_{min})}{2i_{max}i_{min}}. \quad (20)$$

IV. Operation under abnormal conditions

A. Fault current-limiting property

Although it has been proven in the previous section that the inductor current i is limited independently from the regulating function $g(E, i, v, i_L)$, i.e. even if an unrealistic reference voltage, power or current is provided to the controller, it is important to guarantee that the current-limiting property holds under faulty conditions: i) faults in the output (e.g. short circuit) and ii) faults in the input (e.g. input voltage sag).

When a fault occurs in the output (load), the current-limiting property of the dc/dc converters is still guaranteed since the ISS property of the closed-loop current equation (7) is independent of the load. This means that the proposed controller will automatically reduce the output voltage to low values in order to guarantee the current limitation. However, the physical limitations of the dc/dc power converters should be taken into account, particularly for the boost converter where the output voltage is always higher than the input E. In this case, if a short circuit occurs in the output, the current will increase since the minimum output voltage is E independently from any control design (current flows through the converter diode). Assuming a resistive load in the output, the minimum value of the load for a desired current limitation below i_{max} should satisfy

$$R \geq \frac{E}{i_{max}}.$$

For load resistors below R, the boost converter cannot guarantee a current-limiting property. On the other hand, since the minimum output voltage of the buck and the buck-boost converters is zero, these two dc/dc converters can guarantee the current-limiting property under the proposed controller even if a short circuit occurs in the output.

In the second scenario, when the input voltage E drops by a percentage $p \times 100\%$, where $0 \leq p \leq 1$, the closed-loop current dynamics (7) become

$$L\frac{di}{dt} = -(r+w)i + (1-p)E. \quad (21)$$

Then according to the same ISS analysis presented in Subsection III-C, the inductor current satisfies

$$|i(t)| < (1-p)i_{max} < i_{max},\, \forall t \geq 0,$$

maintaining the desired current-limiting property under input voltage dips. However, the current is limited below a lower value than i_{max} depending on the percentage p of the input voltage dip. Hence, a modification in the proposed controller structure is required to fully utilize the capacity of the converter and limit the current at i_{max} and not at $(1-p)i_{max}$. This is described in the sequel.

B. Extending the proposed controller to fully utilize the capacity of the converter

In order to guarantee that the maximum inductor current is i_{max} even when the input voltage E varies, the closed-loop current dynamics for every dc/dc converter should be

$$L\frac{di}{dt} = -(r+w)i + E_n, \tag{22}$$

where E_n is the constant rated input value, opposed to E found in (7) which is the actual input voltage and may vary. Hence, following the same ISS analysis as described in Subsection III-C, by selecting $w_{min} = \frac{E_n}{i_{max}}$ then $|i(t)| < i_{max},\, \forall t \geq 0$ independently from E as long as initially $i(0) \leq i_{max}$. In this case, the maximum value of the inductor current will be i_{max} even if the input voltage E varies or drops below the rated value. Hence, to achieve this task, the proposed controller described in Table I is modified to take the form given in Table II but with the same dynamics (8). Note that when $E = E_n$, then the expressions of Table II become the same with the original expressions in Table I.

Table II
PROPOSED CONTROL LAWS FOR DC/DC CONVERTERS TO FULLY UTILIZE THE CONVERTER CAPACITY

	boost	buck	buck-boost
duty-ratio u	$1-\frac{w}{v}i+\frac{E_n-E}{v}$	$\frac{v+E_n}{E}-\frac{w}{E}i$	$1-\frac{w}{v+E}i+\frac{E_n-E}{v+E}$

The original controller can be useful in the boost converter case, if one compares the duty-ratio expression in Tables I and II. It is clear that the original form (Table I) does not require the measurement of the input voltage E simplifying the controller implementation. This is why this controller will be investigated in the experimental results in Section VI.

V. SIMULATION RESULTS

In order to test the proposed controller and compare it with traditional control strategies, all three main types of dc/dc converters connected to a resistive load of $100\,\Omega$ are simulated using the Simpower Systems toolbox of Matlab/Simulink. Although the average converter model was initially used for the stability analysis and the controller design, the actual switching model is tested here to verify that the developed theory holds true for the real converter system under a high switching frequency. The parameters of the system and the proposed controller are shown in Table III (same for every converter) using the controller structures from Table II with dynamics (8). The control task is to regulate the output voltage

Table III
SYSTEM AND CONTROLLER PARAMETERS (SIMULATION)

Parameters	Values	Parameters	Values
L, r	2 mH, 0.5 Ω	switching freq.	100 kHz
C	50 μF	k_q	100
E	48 V	i_{max}	2 A
c	1.5×10^5	i_{min}	1 mA

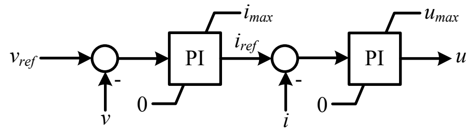

Figure 4. Traditional cascaded PI control with current limitation [7]

to a given value v_{ref}, i.e. $g(v) = v_{ref} - v$. The proposed controller is compared to a traditional cascaded PI controller with saturation units shown in Fig. 4 to achieve current limitation. The saturation of the inner loop has an upper limit at u_{max}, often less than 1 (physical limit of u), to avoid very high currents. The PI gains are chosen as $k_{pv} = 0.01$, $k_{iv} = 10$ for the voltage loop and $k_{pi} = 1$, $k_{ii} = 10$ for the current loop. Since the average value of the inductor current is needed for the control implementation, a low-pass filter is applied at the measurement of the inductor current to remove the switching ripples. This filter also helps in the case of very low currents where the converter may operate in DCM to maintain a continuous-time function for u. It is noted that for a higher switching frequency than the one used in the simulations, the ripples of the current reduce and the actual current will be the same as the filtered one leading to a current-limiting capability for the actual current. In such a case, a low-pass filter will not be needed. In all three power converter cases, the simulation time was limited to $0.4\,$s due to the limited memory of the computer and the small time step used to obtain accurate results ($0.01\,$us). Although the simulation was executed without sharing too much of the steady-state response, the main purpose was to clearly demonstrate both controller responses under different scenarios, i.e. i) changes of the reference voltage, ii) changes of the input voltage and iii) changes of the load.

Boost converter: The output reference voltage v_{ref} is set initially to $60\,$V, at $t = 0.05\,$s it changes to $80\,$V and at $t = 0.1\,$s it increases to $120\,$V, which will require a large inductor current in order to test the current-limiting property of the controllers. As it is shown in the left column of Fig. 5(a), during the first $0.1\,$s, both controllers regulate the output voltage at the desired level after a short transient. However, when the reference voltage v_{ref} increases to $120\,$V, the output voltage is regulated near $96\,$V because i tries to violate the maximum value i_{max}. Both the proposed controller and the traditional controller guarantee the current-limiting property as clearly shown in the left column of Fig. 5(b). At $t = 0.15\,$s, the reference v_{ref} changes back to $80\,$V and the output voltage smoothly returns to the desired value with the proposed controller. On the other hand, the traditional PI fails to reduce the voltage quickly due to windup issues in the outer voltage control loop caused by the saturation. In order to test the controller under abnormal conditions, at

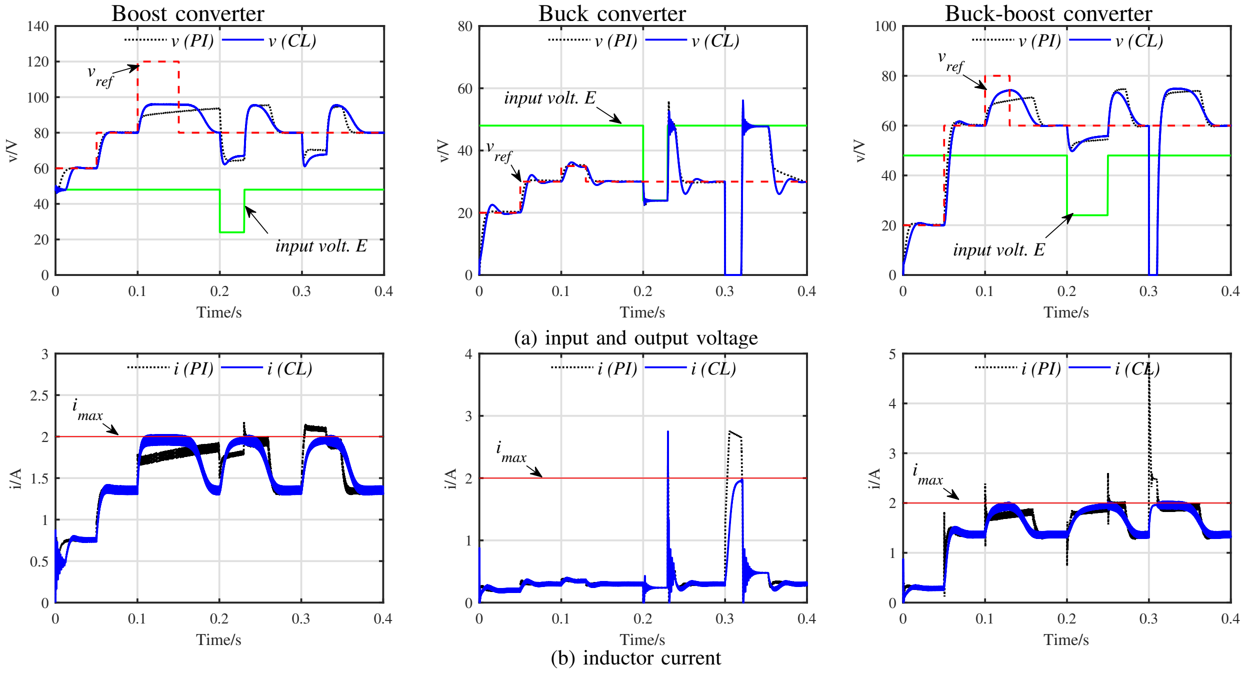

Figure 5. Simulation results with the proposed current-limiting (CL) controller and the traditional cascaded PI controller with saturation

$t = 0.2\,\mathrm{s}$ the input voltage E drops to $24\,\mathrm{V}$ and returns to the original value after $0.03\,\mathrm{s}$ (left column of Fig. 5(a)), while at $t = 0.3\,\mathrm{s}$ the load resistor R changes from $100\,\Omega$ to $50\,\Omega$ for a duration of $0.03\,\mathrm{s}$. In both cases, the inductor current increases but is always limited below i_{max}, as expected by the proposed controller (left column of Fig. 5(b)). However, the traditional current-limiting method cannot maintain i below i_{max} during transients, especially after the load change, which is a significant disadvantage compared to the proposed method.

Buck converter: Similarly, for the buck converter case (middle column of Fig. 5), initially both the proposed controller and the traditional cascaded PI controller regulate the output voltage at the desired levels. At $t = 0.2\,\mathrm{s}$, the input voltage drops to $24\,\mathrm{V}$ and returns to its original value after $0.03\,\mathrm{s}$. Since the output voltage cannot be regulated at $30\,\mathrm{V}$ due to the inherent limitation of the converter, the voltage is regulated at the higher possible value ($24\,\mathrm{V}$). When the input voltage returns to its original value, both controllers smoothly regulate the output voltage at v_{ref} but the instantaneous value of the current results in a peak that exceeds i_{max}. Nevertheless, the average inductor current is always below i_{max} due to the limited power of the converter, as shown in the middle column of Fig. 5(b). However, when a short circuit occurs in the output at $t = 0.3\,\mathrm{s}$, the proposed controller guarantees the current-limiting property opposed to the traditional cascaded PI.

Buck-boost converter: Finally, a buck-boost converter is investigated (right column of Fig. 5) and as in the previous cases, when the inductor current is below i_{max}, the output voltage reaches the desired level. When the reference voltage changes to $80\,\mathrm{V}$, the output voltage is regulated to a lower value since the current increases and reaches the limit (right column of Fig. 5(b)). At the time instant $t = 0.2\,\mathrm{s}$, the input voltage E drops to $24\,\mathrm{V}$ for a duration of $0.05\,\mathrm{s}$, as shown in the right column of Fig. 5(a), and at $t = 0.3\,\mathrm{s}$, a short circuit occurs at the output for $0.01\,\mathrm{s}$ in order to test the controller performance under abnormal conditions. In both the cases of the input voltage drop and the short circuit, with the proposed control framework, i never violates i_{max} as shown in the right column of Fig. 5(b). On the other hand, with the traditional current-limiting technique, the inductor current violates several times the limit. The current limitation is not guaranteed during the transients. Hence, it is verified that the proposed controller can protect all three types of dc/dc converters from high currents at all times, i.e. during transients, unrealistic power demands, faults. In the cases of the buck and the buck-boost converters, it can additionally protect the device from short circuits in the output. This shows the significance of having a rigorous stability proof and current limitation based on the nonlinear ISS theory. As a result, when a higher output voltage is required, the buck-boost converter should be used instead of the boost since the current limitation is maintained independently from the load. Note that although both the PI and the proposed controller can suffer from saturation in the control input u, due to the physical limit of the converter, the PI suffers from saturation and windup additionally in the outer loop, thus failing to guarantee the current limitation and setting the proposed scheme superior in handling the required bounds for the system state i.

VI. Experimental Results

To further evaluate the effectiveness of the proposed control framework, the boost converter is experimentally tested. The input voltage E of the converter is set at $48\,\mathrm{V}$ and the load resistor is $R = 100\,\Omega$. The proposed controller is chosen from the boost converter scenario in Table I with dynamics (8), where the measurement of the input voltage is not needed to minimize the total number of sensors used. This is the main difference between the boost converter tested in the experiments compared to the one in the simulation results.

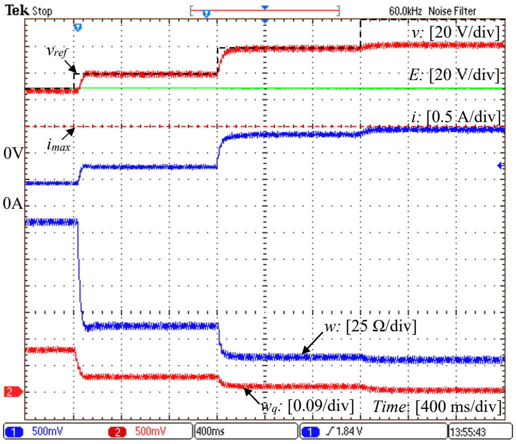

Figure 6. Experimental results of the boost converter with the proposed controller under reference output voltage changes

In addition, different converter parameters were used due to practical limitations of the available experimental setup. Although the converter parameters are not optimized, the purpose of this section is to experimentally demonstrate the current-limiting controller that has been introduced for the first time in this paper. For the optimization of the converter the reader is referred to [26]. The implementation of the proposed controller is conducted in the discrete time domain by discretizing the integral functions (8) using the TMS320F28335 DSP with a sampling frequency of 16 kHz and a switching frequency of 50 kHz. As underlined in [11], the higher the sampling frequency the more accurate the average model becomes with respect to the actual switching system. Hence, for the given sampling frequency, the delay in the discrete control implementation is small and can be ignored. Therefore, the stability analysis and the current-limiting property are valid as shown in the experimental results that follow. The different system parameters compared to Table III are $L = 2.2\,\text{mH}$, $C = 300\,\mu\text{F}$, $i_{max} = 1.5\,\text{A}$ and $t_s = 0.05\,\text{s}$.

A. Change of the output voltage reference

Fig. 6 shows the time response when the reference signal v_{ref} changes. The controller is enabled at $t = 0.4\,\text{s}$ with $v_{ref} = 60\,\text{V}$, at $t = 1.6\,\text{s}$ the reference value increases to 80 V and at $t = 2.8\,\text{s}$ it changes to 120 V. As it is shown in Fig. 6(a), the proposed controller quickly regulates v to v_{ref} for the first 2.8 s, but when v_{ref} increases to 120 V, the output voltage is regulated near 83 V. The reason is that the inductor current increases and tries to violate the maximum value $i_{max} = 1.5\,\text{A}$. Fig. 6(a) shows also the current response which increases and is limited slightly below i_{max}, due to the small r which have been ignored in the controller design. To understand how the controller states behave, their time response is also shown in Fig. 6 where finally $w \rightarrow w_{min}$ and $w_q \rightarrow 0$ as explained in the theory.

B. Change of the load

While the proposed controller has regulated the output voltage at $v_{ref} = 60\,\text{V}$, the load in the output changes from $100\,\Omega$ to $70\,\Omega$. As it is shown in Fig. 7, the output voltage returns to its desired value after a very short transient. The inductor current increases but still remains below i_{max}.

A larger load change, i.e. from $100\,\Omega$ to $40\,\Omega$, is also tested when the output voltage reference is again $v_{ref} = 60\,\text{V}$ in Fig. 8. As it is observed in Fig. 8(a), the output voltage drops after the load change. This is because the current increases and due to the current-limiting property of the converter cannot exceed i_{max}. Since $i \rightarrow i_{max}$, then the maximum output voltage can be calculated from the power equivalence between the input and the output as $v = \sqrt{E i_{max} R} = 53\,\text{V}$; thus the proposed controller leads the output voltage to this value (Fig. 8(a)).

It is highlighted that according to the analysis presented in Subsection IV-A, for the given input voltage E, the minimum load resistance for a boost converter to achieve current-limitation with any control technique is obtained from the power equivalence and the minimum output voltage $v = E$ as $R_{min} = \frac{E}{i_{max}} = 32\,\Omega$. This limitation does not apply to the buck or the buck-boost converter as illustrated in the simulation results, since in these cases the current limitation is guaranteed even under a short circuit in the output.

C. Change of the input voltage

In order to investigate the cases of input voltage sags, two different scenarios are tested where E drops from 48 V to 40 V (Fig. 9) and from 48 V to 24 V (Fig. 10), while v is regulated at $v_{ref} = 60\,\text{V}$. In the first case, the inductor current increases but does not violate the limit and as a result the output voltage is regulated at the desired value. In the second case, where a 50% input voltage drop occurs, the output voltage drops to maintain the current limiting property. Since the original controller (Table I) is used and a 50% input voltage drop occurs, i.e. $p = 0.5$, then according to the analysis presented in Subsection IV-A, the current will be limited below $0.5 i_{max} = 0.75\,\text{A}$. Indeed, as shown in Fig. 10, the limit of the current drops as soon as the input voltage drops and is limited below 0.75 A according to the theory. Although the full capacity of the converter is not utilized due to the original controller used (Table I), this controller is preferred since no input voltage sensor is required and $i < i_{max}$ is still guaranteed at all times.

VII. Conclusions

A new control framework for dc/dc power converters was developed in this paper to achieve different regulation scenarios with a current-limiting property. The current limitation was achieved without requiring any knowledge of the converter parameters or the load and was extended to the cases of faults in the input and the output of the converter, leading to an inherent protection property of every dc/dc converter via the control design. This was accomplished without additional protection circuits, saturation units or switching actions in contrast to traditional approaches.

Future research will focus on the optimization of the converter parameters, on the analysis the proposed current-limiting framework under both CCM and DCM operation including the time delay issue in the implementation and on the design of the controller gain to further improve the transient performance and address the duty-ratio saturation issue.

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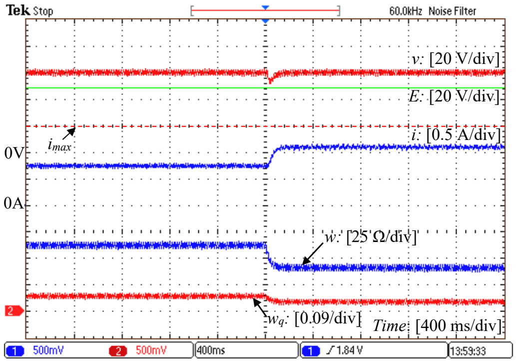

Figure 7. Experimental results of the boost converter with the proposed controller when $v_{ref} = 60\,\text{V}$ and the load changes from $100\,\Omega$ to $70\,\Omega$

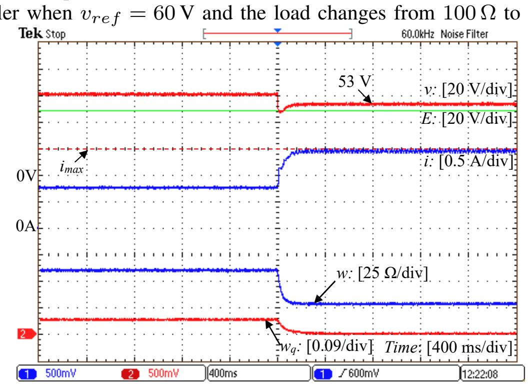

Figure 8. Experimental results of the boost converter with the proposed controller when $v_{ref} = 60\,\text{V}$ and the load changes from $100\,\Omega$ to $40\,\Omega$

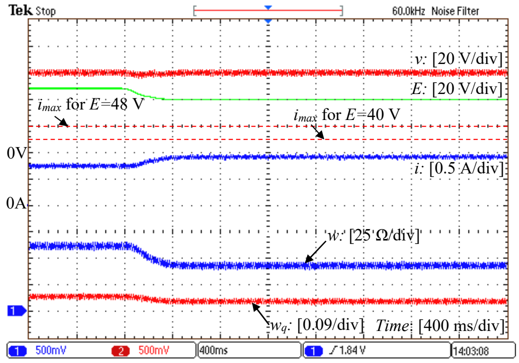

Figure 9. Experimental results of the boost converter with the proposed controller when $v_{ref} = 60\,\text{V}$ and the input voltage drops ($48\,\text{V} \rightarrow 40\,\text{V}$)

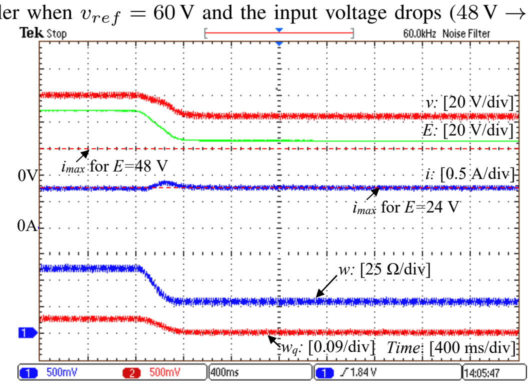

Figure 10. Experimental results of the boost converter with the proposed controller when $v_{ref} = 60\,\text{V}$ and the input voltage drops ($48\,\text{V} \rightarrow 24\,\text{V}$)

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