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Real-time Measurement of Temperature Sensitive Electrical Parameters in SiC Power MOSFETs

Antonio Griffo, *Member, IEEE,* Jiabin Wang, *Senior Member, IEEE*, Kalhana Colombage, Tamer Kamel, *Member, IEEE*

***Abstract*— This paper examines a number of techniques for junction temperature estimation of SiC MOSFETs devices based on the measurement of Temperature Sensitive Electrical Parameters (TSEPs) for use in online condition monitoring. Linearity, sensitivity to temperature and circuit design for practical implementation are discussed in detail. A demonstrator based on the measurement of the quasi-threshold voltage, the turn-on transient characteristic (*di/dt*), the on-state voltage and the gate current peak is designed and validated. It is shown that the threshold voltage, the estimation of the gate current peak and the on-state voltage have potentially good sensitivity to temperature variation and linearity over a wide operating range. Very low sensitivity to temperature is shown for (*di/dt*). The proposed method can provide a valuable tool for continuous health monitoring in emerging applications of SiC devices to high reliability applications.**

***Index Terms*—Power semiconductor devices, Condition monitoring, Power MOSFETs, Temperature measurements**

I. INTRODUCTION

POWER electronic systems play an increasingly significant role in high reliability applications such as the automotive and aerospace sectors. However, stringent safety requirements and conservative design practices pose significant challenges to the adoption of novel and relatively unproven technologies such as the use of novel wide band-gap (WBG) devices e.g. Silicon Carbide (SiC) power MOSFETs or Gallium Nitride (GaN) high electron mobility transistors which have the potential to significantly increase efficiency and power density. Continuous condition monitoring of power devices can potentially reduce failure rates and alleviate reliability concerns by providing real-time information on the state of health of the devices and indication on the remaining useful lifetime [1]-[2].

Reliability of power electronic components is significantly affected by the device operating conditions. It is well known that two of the most significant stress factors for power electronics modules are absolute temperature and temperature variations which result in thermo-mechanical stress due the different coefficients of thermal expansions (CTEs) of materials in the modules [3]-[4]. Repetitive thermal cycling can eventually cause cracks and voids in solder joints, bond-wire lift-off, and delamination within module interconnection resulting in increased thermal resistance and ultimately even higher junction temperatures [5].

The measurement or estimation of junction temperature during the operation of a power electronic converter is therefore essential for its condition monitoring and prognosis of the remaining useful life [6].

Monitoring of devices junction temperatures during real-time operation of a power electronics converter can be realized with either direct or indirect methods [7]. Direct temperature measurements using optical or physical contact methods have been proposed in literature [8]-[9]. Optical methods using optical fibers [8] and infrared thermal imaging can provide an accurate spatial temperature map of the power electronic module. However, these methods require the chip to be optically connected to the detection system and therefore the protective dielectric gel has to be removed. Similarly, physical contact methods require a direct contact with the chip with a thermo-sensitive material [9] or temperature probes requiring significant alterations to module packaging and dielectric gel. Whilst potentially the most accurate ways of monitoring temperature, the invasive nature of direct measurement methods make them only suitable in laboratory testing conditions and therefore unsuitable for general applications.

It is well known that a number of electrical parameters in semiconductor devices exhibit a measurable temperature dependence. The measurement of Temperature Sensitive Electric Parameters (TSEPs) can potentially provide a more practical, albeit indirect, solution for temperature monitoring of power devices [10]-[13]. The non-invasive nature of TSEPs-based approaches can allow temperature estimation on standard packaged modules without modification to the module itself, only requiring access to terminal electrical quantities.

A number of studies have been published on the use of TSEPs for Silicon (Si) MOSFETs and IGBTs power devices, including the monitoring of *dI/dt* during turn-on or *dV/dt* during turn-off transients [14]-[16], Miller capacitance discharge time [17], threshold voltage [18]-[20], on-state voltage drop [21]-[23], voltage across source/emitter parasitic inductance [24], internal gate resistance [25]-[26], gate drive turn-on transients [27].

Despite the increased interest in the use of WBG devices, only very limited literature is available in the public domain on the use of TSEPs for SiC MOSFETs [28]-[29]. Furthermore, most of the publications on TSEPs focus on the description of the underlying physical properties and often do not provide

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circuit design guidelines for practical implementation of TSEPs measurement in a real-time condition monitoring system.

The paper presents an overview of the methods for junction temperature estimation based on the measurement of TSEPs and discusses the feasibility of online monitoring of TSEPs of SiC MOSFET devices. Four potential TSEPs are identified, namely the quasi-threshold voltage, the turn-on transient (*di/dt*) characteristic, the on-state voltage and the gate current peak, based on sensitivity to temperature and suitability for online measurement under converter switching operation. Comprehensive design and experimental validation of the proposed online monitoring techniques are presented.

II. Temperature Sensitive Electric Parameters in SiC MOSFETs

The temperature dependence of the electrical characteristics of semiconductor devices arises as a result of the thermal dependency of a number of parameters, the most significant being the bandgap energy $E_g(T)$, the effective mobility $\mu(T)$ and intrinsic concentration $n_i(T)$ of the charge carriers. Similarly to most semiconductor materials, the bandgap energy $E_g(T)$ decreases as temperature increases, whilst the intrinsic concentration increases with temperature [30]. The mobility $\mu(T)$ in SiC devices has a more complex dependency on temperature depending on doping levels and density of traps at the gate oxide/SiC interface resulting in bulk mobility to decrease but channel mobility to potentially increase with temperature [31]-[32]. Temperature effects on these parameters can be summarised by the empirical relations:

$$E_g(T) = E_g(T_0) - \alpha_1 \frac{T^2}{T + \beta_1} \tag{1}$$

$$n_i(T) = N^{\alpha_2} \exp\left(-\frac{\gamma}{T}\right) \tag{2}$$

$$\mu(T) = \mu_0 \frac{\beta_2 \left(\frac{T}{T_0}\right)^{\alpha_3}}{1 + \beta_2 \left(\frac{T}{T_0}\right)^{\alpha_4}} \tag{3}$$

where $\alpha_i, \beta_i, \gamma$ are fitting coefficients. As a consequence, most terminal device characteristics are temperature dependent.

The sensitivity to temperature rise of on-state resistance, threshold voltage V_{th}, drain current commutation rate dI_{DS}/dt and gate current Miller plateau are evaluated through analytical modelling and experimental measurements on SiC MOSFETs and compared to those of Si IGBTs in [29]. A general conclusion is that the use of TSEPs in SiC devices is relatively more challenging than in Si IGBT. This is due to faster switching transients and lower sensitivity to temperature which are caused by the wider band-gap requiring more thermal energy to excite charge carriers as well as smaller chip areas resulting in lower Miller capacitance.

The on-state voltage $V_{DS,on}$, threshold voltage V_{th}, the internal gate resistance ($R_{G,int}$) indirectly estimated by measuring the peak of gate current and the turn-on transient (di_{DS}/dt) have been selected for further analyses based on their suitability for online measurement under converter switching operation.

A. On-state voltage $V_{DS,on}$

The on-state resistance $R_{DS,on}$ and consequently the voltage across the device during forward conduction $V_{DS,on}$ have a reasonably good sensitivity to temperature as shown in the measurements in Fig. 1. However, the temperature dependence is potentially nonlinear and current-dependent, therefore its use in online monitoring requires current measurement in order to decouple the load dependency from thermal effects. $V_{DS,on}$ is also dependent on the state-of-health of device-to-packaging interconnects and indeed the collector-emitter voltage V_{CE} in IGBTs has also been proposed as a condition monitoring indicator of wirebond lift-off and solder fatigue [33].

The main challenge in the practical use of the $V_{DS,on}$ for online monitoring resides on the significant voltage excursion across drain-source terminals during converter switching, ranging from few Volts during conduction to well over the dc-link voltage V_{dc} during turn-off transients. These voltage excursions complicate the design of signal acquisition circuitry with significant challenges in terms of high dynamic range and isolation between the low-voltage monitoring circuit and the high-voltage power stage. A number of circuits suitable for on-state voltage measurement derived from commonly used methods for de-saturation protection have been proposed using either passive (diode) or active solutions for disconnecting the measurement circuitry during turn-off transients [22]. The emitter-follower circuit illustrated in Fig. 1 shows a practical solution to the measurement of $V_{DS,on}$ of the device $M1$ under test [21]. The device $M2$ isolates the measuring circuitry connected to V_m from the high voltage side when the drain D voltage rises above the reference $9V$ during turn-off transient of M1, effectively limiting V_m to safe voltage levels. When the device M1 under test is switched on, $V_{DS,on}$is a few volts, and M2 is heavily saturated. Hence the measurement voltage V_m across R is effectively equal to $V_{DS,on}$. When M1 is switched off, V_{DS} quickly increases to the DC link voltage. As soon as V_{DS} raises above $9V$, the gate-source voltage of M2 drops to zero effectively switching M2 off, isolating the measurement point from the high voltage. With this circuit, the voltage measurement range is reduced to a few volts, and hence accuracy and resolution can be significantly improved.

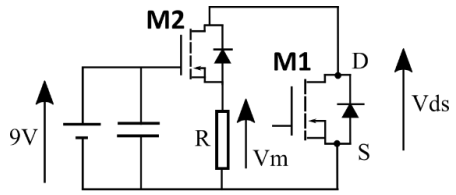

Fig. 1. Circuit schematic for $V_{DS,on}$ measurement

B. Threshold voltage V_{th}

The threshold voltage V_{th} is the minimum gate-source voltage required to switch on the device. Physically, V_{th} is the minimum gate bias starting to induce an inversion layer of free electrons underneath the gate oxide, creating a conductive channel between drain and source in MOSFET or collector and emitter in IGBT. The increase of carrier concentration and the decrease of bandgap with temperature results in a decrease of

V_{th} with temperature, typically modelled as an approximately linear dependence. Practical measurement of V_{th} , such as those reported in datasheets, requires the definition of a current level at which the gate measurement is taken. Although, current comparison can be effectively used in static conditions, similarly to those used in datasheet measurements, it is not practical for online measurements during switching transients.

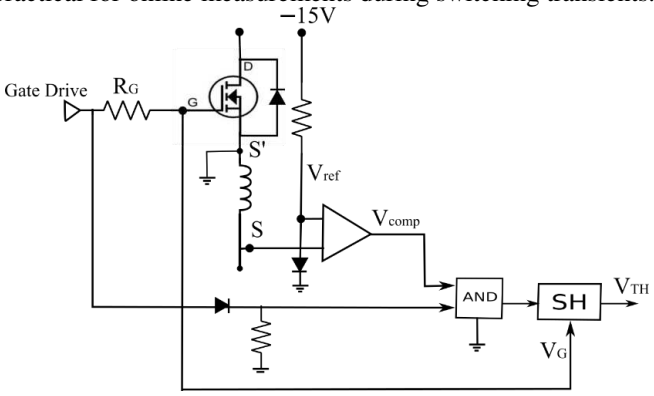

Fig. 2. Schematic circuit for quasi-threshold voltage measurement

The main challenge in online detection of V_{th} during turn-on transients lies in the sampling of the gate voltage at the correct instant in time since the gate-source voltage V_{gs} has very fast rising times typically up to $1V/ns$. A potentially suitable method used for the detection of a quasi-threshold voltage, adapted from [19],[34] where it was proposed for IGBT applications, is illustrated in Fig. 2. A voltage across the parasitic inductance between the auxiliary Kelvin source (S') and the source (S) is generated when the device current i_{DS} starts to rise during device turn-on. The rising edge of the voltage $v_{SS'}$ across the parasitic inductance, which is proportional to di_{DS}/dt, can be used to trigger the sample and hold circuitry acquiring the gate-source voltage $v_{GS'}$ effectively capturing the start of conduction and therefore the quasi-threshold voltage. An AND gate activated by the gate drive signal, is used to avoid spurious triggering due to noise outside of the switching transients. Illustrative waveforms of the gate drive signal, gate-source voltage $v_{GS'}$, voltage across the external gate resistance V_{RG} and the voltage across the parasitic inductance $v_{SS'}$ during a turn-on event, are shown Fig. 3.

A potentially significant benefit of V_{th} use as TSEP is its independence from load current.

C. Internal gate resistance ($R_{G,in}$)

The internal gate resistance $R_{G,int}$ is the lumped equivalent of the distributed resistance of the polysilicon gate and metal contacts in the MOSFET device. From terminal point of view, $R_{G,int}$ can be considered in series with the parallel of the gate-source and gate-drain capacitances. The time constant τ_{on} of the equivalent gate capacitance charging process during turn-on before V_{th} is reached can be expressed as:

$$\tau_{on} = \left(R_{G,ex} + R_{G,int}\right)\left(C_{GS} + C_{GD}(V_{DS})\right) \qquad (4)$$

where $R_{G,ex}$ is the external gate resistance , C_{GS} and C_{GD} are the gate-source and gate-drain capacitances, respectively. At turn-on, for a fixed DC-link voltage, the drain-source voltage V_{DS} can be considered constant, hence C_{GD} can also be considered

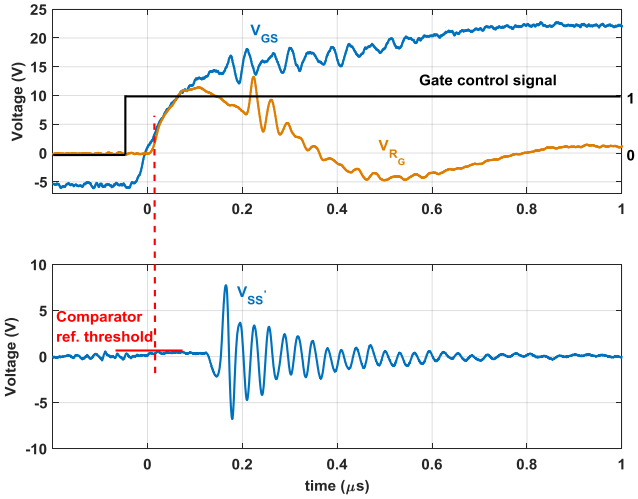

Fig. 3. Typical waveforms during SiC MOSFET (CCS020M12CM2) turn-on transient: gate drive signal, gate-source voltage V_{GS}, voltage across the external gate resistance V_{RG} (top) and the voltage across the parasitic inductance $V_{SS'}$ (bottom).

constant. C_{GS} does not change significantly until V_{th} is reached. $R_{G,ex}$ is assumed to be constant at a known ambient temperature. It follows that $R_{G,int}$ becomes the dominating temperature dependant parameter in (4) affecting gate current during turn-on. Assuming the simplified RC circuit representation of gate charging process, the peak of the gate current i_G can be considered proportional to $R_{G,in}$. A simple peak detector circuit measuring the voltage across the external gate resistor ($V_{RG,ext}$) whose peak is directly proportional to the gate current [25]-[27], is outlined in the schematic shown in Fig. 4.

Similarly to V_{th}, the internal gate resistance as TSEP is potentially load independent. Heavy doping of polysilicon required for low resistivity gates, typically results in low temperature coefficient of its resistivity [35], potentially resulting in low sensitivity of $R_{G,in}$ as a TSEP.

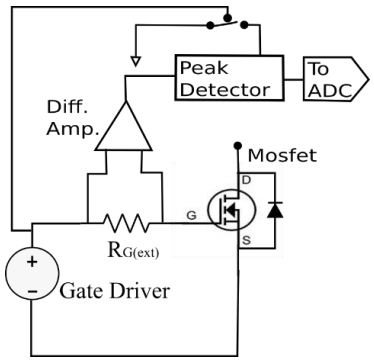

Fig. 4. Schematic circuit for gate current peak detection

D. Turn-on transient (di_{DS}/dt)

The rate of change of device current i_{DS} during a turn-on transient can be expressed as [28]:

$$\frac{di_{DS}}{dt} = \mu \frac{C_{ox}W}{L}(V_{GS} - V_{th}) \frac{V_{GG}}{R_G(C_{GS} + C_{GD})} e^{-\frac{t}{R_G(C_{GS}+C_{GD})}} \quad (5)$$

where μ is the electron mobility, C_{ox} is the intrinsic gate oxide capacitance, W/L is the gate width/length ratio, V_{GG} is the gate drive voltage.

The negative temperature coefficient of both threshold voltage V_{th} and mobility μ have contrasting influence on di_{DS}/dt. While a reduction in V_{th} with temperature would favour faster turn-on, the reduction of mobility would have opposite influence on di_{DS}/dt. As a first order approximation, the temperature dependency of μ could be neglected in the initial phase of the turn-on process, resulting in the prediction of increase of di_{DS}/dt with temperature. Extensive measurements reported in [29] shows that the temperature variation of di_{DS}/dt is device and circuit dependent. For large devices di_{DS}/dt increases with temperature, however the variation becomes very small for low current devices. The gate drive resistance R_g also has a strong influence on di_{DS}/dt and its sensitivity to temperature variations becomes vanishingly small for low values of R_g required for switching losses minimization. Gate drives with variable output resistances have been proposed as a potential solution for occasional temperature monitoring [18]. In conclusion, the practical use of di_{DS}/dt as TSEP is non-trivial not only because of the extremely fast transients resulting in challenging acquisition circuit design, but also due to a potentially very low temperature sensitivity and current dependence.

Since the voltage $V_{SS'}$ across the source parasitic inductance $L_{SS'}$ is proportional to the rate of change of i_{DS}, the peak value of $V_{SS'}$ will be used as an indirect measurement of di_{DS}/dt as illustrated in Fig. 5. The peak detector can be realised with a precision half-wave rectifier, a circuit also known as active diode, and a resettable memory capacitor as shown in Fig. 6. The memory capacitor hold the peak value of the voltage across $L_{SS'}$ over the turn-on transient until is reset in the next switching cycle. The integration of $V_{SS'}$ can be used to estimate the output current i_{DS} as illustrated in Fig. 7. This can provide a practical way of estimating device current which can be used to decouple load and temperature dependence of the proposed TSEPs.

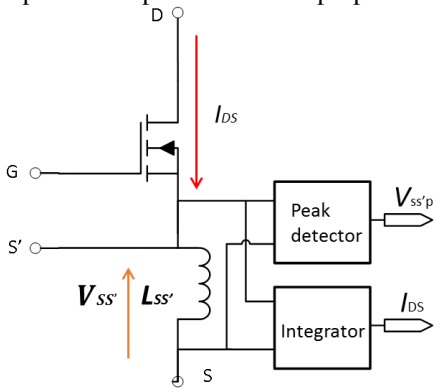

Fig. 5. Schematic circuit for measurement of peak voltage and current across $L_{SS'}$

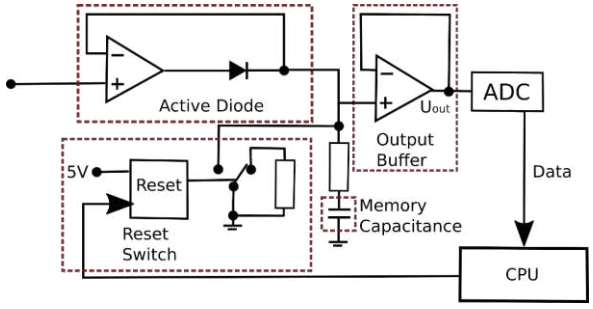

Fig. 6. Schematic circuit for peak detector

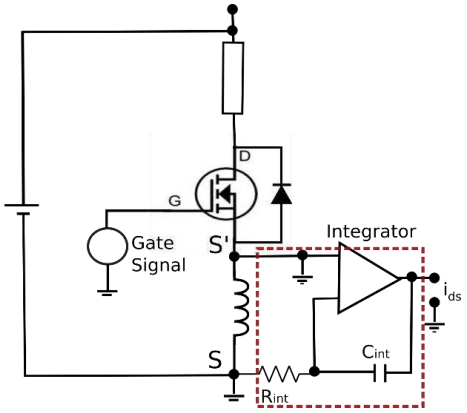

Fig. 7. Current measurement using integration of $V_{SS'}$

A qualitative comparison of the analysed TSEPs for SiC MOSFETs is summarized in Tab. 1.

TABLE I
COMPARISON OF TSEPS FOR SIC MOSFETS

TSEP	ADVANTAGES	DISADVANTAGES
On-state voltage drop (V_{DS})	• Good potential sensitivity • No modification to module	• Not linear in SiC • Current dependent • Small value and less sensitive to temperature variation in SiC • Non-trivial circuit isolation
Threshold voltage (V_{th})	• On-line monitoring possible via an auxiliary Kelvin source and parasitic inductance	• An auxiliary Kelvin source is required • Less temperature sensitive in SiC • Susceptible to noise
Turn-off and Turn-on times or di/dt	• On-line monitoring possible via an auxiliary Kelvin source and parasitic inductance	• Low temperature sensitivity • High dI/dt or short duration • Complex behaviour in SiC
Internal Gate Resistance/ current	• No module modification is required, possible also on three-terminal devices (without auxiliary Kelvin source)	• High resolution ADC is required • Susceptible to noise

III. TSEPS MONITORING CIRCUIT DESIGN

The methods for online TSEPs monitoring described in the previous section have been implemented in a data acquisition

and control circuit board whose main functionalities are shown in the block diagram of Fig. 8. Two high resolution (18-bit) Analog-to-Digital Converters (ADC) are at the core of the proposed design. The ADCs, configured with a full differential range of ± 4.096V provide a resolution of 0.031 mV. The voltages across the external gate resistance V_{Rg}, the voltage between the source and auxiliary source connection $V_{SS'}$, the gate-source voltage $V_{GS'}$ and the voltage across the drain-source V_{DS} are all measured on the power SiC MOSFET. An additional channel is dedicated to thermistor (NTC) temperature sensor for module baseplate temperature monitoring purpose. Resettable peak detectors and integrators are used to measure the peak of $V_{SS'}$ and V_{Rg} during turn-on and integrate $V_{SS'}$, respectively, as described in the previous sections. A supervisory CPU (ARM Cortex M4) controls the data acquisition communicating with the ADCs and controlling the reset signals for the integration and peak detection, generates the control signals for the gate drives and manages the USB communication interface with a supervisory PC for data storage and display.

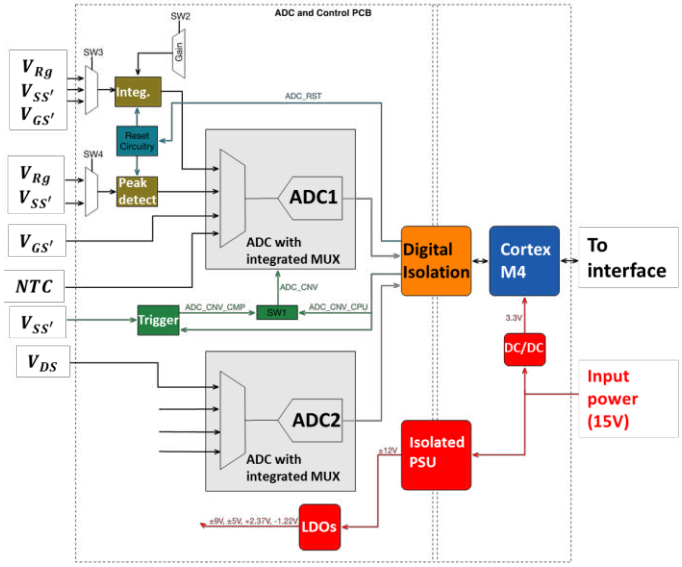

Fig. 8. Schematic diagram of the designed aquisition board for TSEPs monitoring

The timing of the control signals is managed by the CPU depending on the specific TSEP to be measured. The data transfer from ADCs and CPU is through SPI bus and the required physical isolation between the analogue side (referenced to the power converter ground) and the digital side (CPU) is obtained with the use of opto-coupled digital isolator integrated circuits. Photos of the top and bottom sides of the manufactured board, annotated with the main features and components, are shown in Fig. 9. The board, manufactured on a four-layer PCB measures 78mm x 50 mm.

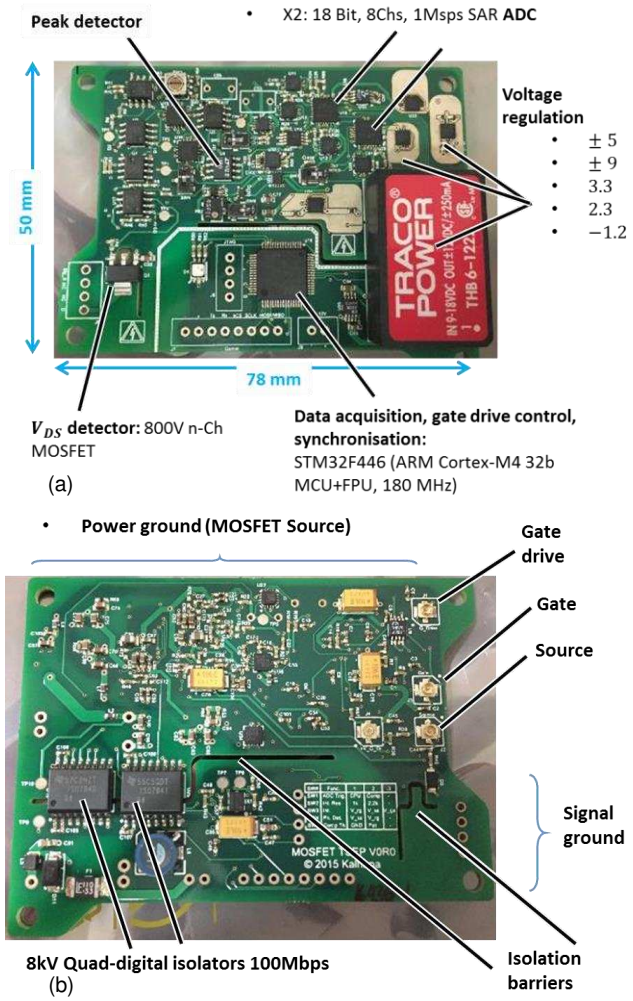

Fig. 9. Top (a) and bottom (b) side of the aquisition board

IV. Experimental Setup

Experimental assessment of the proposed TSEPs monitoring has been performed using a double pulse testing setup whose schematic and principle of operation are illustrated in Fig. 10. A photo of the experimental setup is shown in Fig. 11. An air-cored inductor (170μH) is used as load. A temperature controlled hot-plate is used for testing at different conditions. A SiC six-pack module (Cree CCS020M12CM2) has been used. The module is mounted on PCB providing planar DC link connections. An off-the-shelf gate drive (Prodrive Technologies - PT62SCMD12) has been used. An interface PCB is used to isolate the CPU and the computer through USB interface. Although the ADC PCB also contains digital isolators to isolate the Kelvin source (GND) from the CPU, the digital interface and isolation PCB adds extra protection for the user and the computer. In addition, this PCB also contains a USB to serial bridge (for SPI communication over USB) as well as JTAG connection to the CPU (through external J-Link emulator). The gate drive signal generated by the CPU in the ADC PCB is also routed through this PCB.

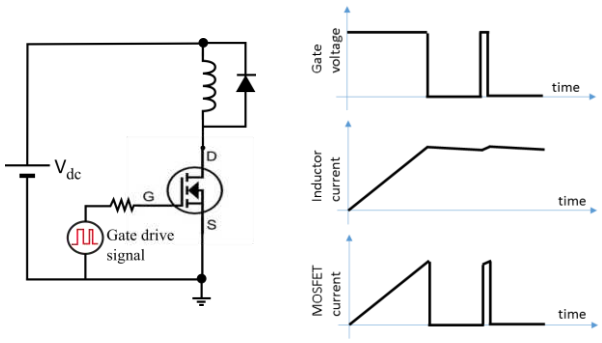

Fig. 10. Schematic circuit (left) and exemplary waveforms (right) of a double pulse test

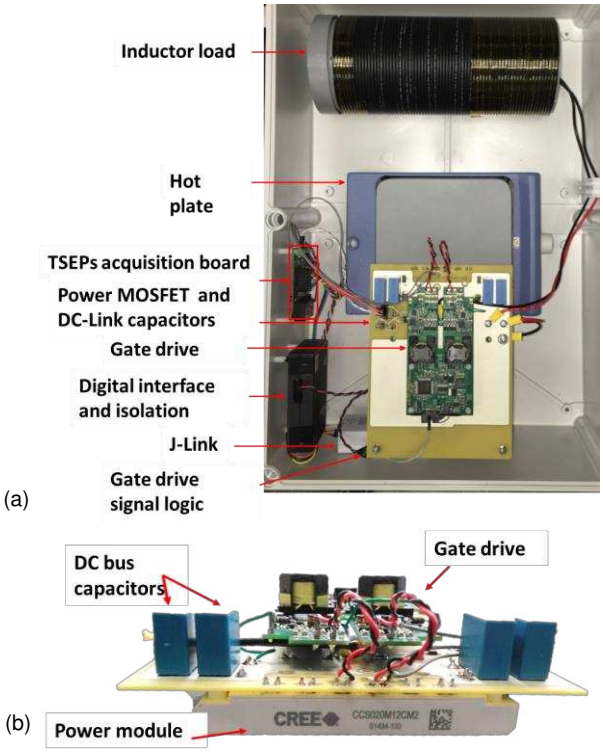

Fig. 11. Experimental setup (a) and view of the power module (b)

V. Results and Discussion

Experimental measurements have been performed on the SiC module up to its maximum rated current (29.5A at 25°C) and at temperatures ranging from ambient to 130°C. Temperature is controlled with the hotplate and monitored through the integrated NTC in the module. If sufficient time is allowed between the application of the double pulse transients, device self-heating is minimized and, in steady-state conditions, the device temperature will be equal to the baseplate temperature measured by the integrated NTC.

A. On-state voltage $v_{DS\,on}$

The measured on-state voltage $v_{DS\,on}$ as function of temperature and load current with $v_{GS} = 20V$ is shown in Fig. 12. A good sensitivity of $13.7mV/°C$ at maximum current is demonstrated, similar to the sensitivity of approximately $10mV/°C$ reported in the datasheet reported in the device datasheet using offline methods. A small discrepancy might be due to slightly different testing conditions e.g. gate drive voltage and device variability. A good linearity with temperature is also evident. The on-state voltage is, however, current-dependent and therefore the use of $v_{DS\,on}$ as TSEP requires an independent measurement of device current in order to decouple the load from temperature effects. Device current measurement can be obtained either through resistive shunts or using the integration of parasitic inductance voltage $V_{SS'}$ as described in the previous section. However a shunt may compromise packaging and add extra loss to converter, both are not desirable.

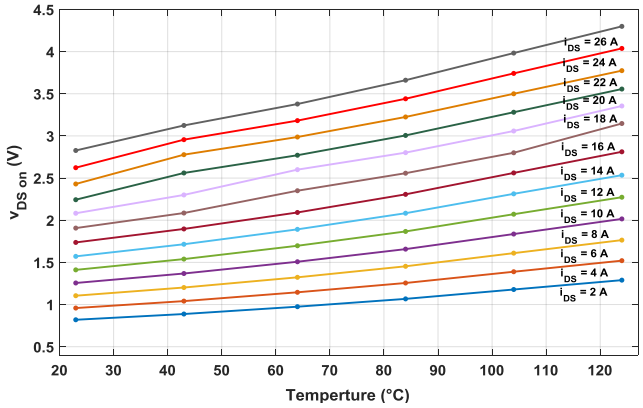

Fig. 12. Measured on-state voltage $v_{DS\,on}$ as function of temperature and load current

B. Quasi-threshold voltage

The measured quasi-threshold voltage as function of temperature and load current using the method described in section II.B is shown in Fig. 13. The expected negative temperature coefficient of v_{th} is confirmed. A relatively good linearity is observed. Good sensitivity of ~9.3mV/°C is shown. The invariance to load current of v_{th} is also confirmed.

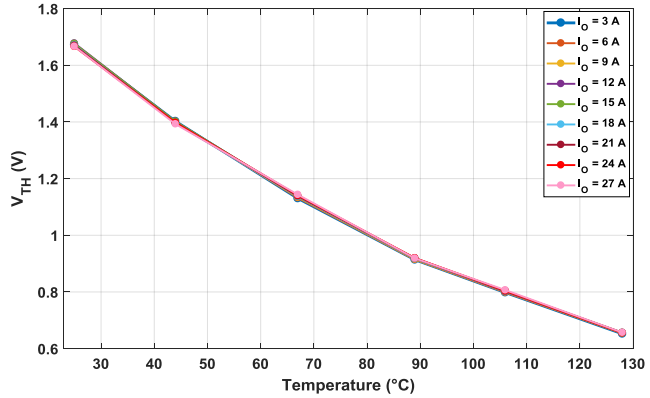

Fig. 13. Measured quasi-threshold voltage vs temperature and load current

C. Internal gate resistance (R_{Gin})

The estimated internal gate resistance as function of temperature and load current according to the methodology of section II is shown in Fig. 14. A good load invariance and linearity with temperature is demonstrated, although the relatively small sensitivity of $3.6m\Omega/°C$ makes the method potentially sensitive to noise. Temperature variation in external

gate resistance and in the gate drive circuit will also affect the accuracy of estimation. Therefore, the external gate resistance should be selected with very low temperature coefficient. The effect of variation of gate drive characteristic with temperature may be decoupled by measurement of the gate voltage.

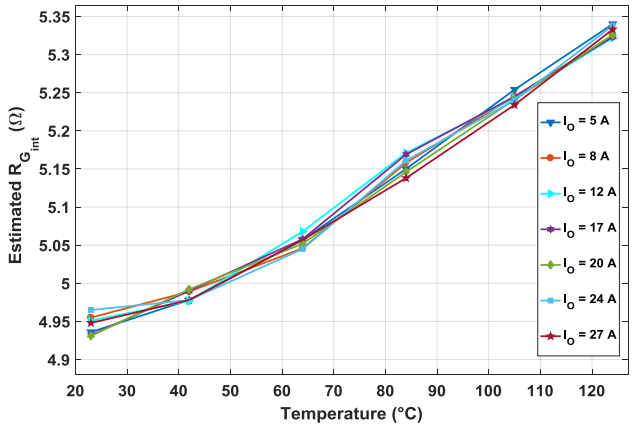

Fig. 14. Measurement of the estimated internal gate resistance as function of temperature and load current

D. *Turn-on transient* (di/dt)

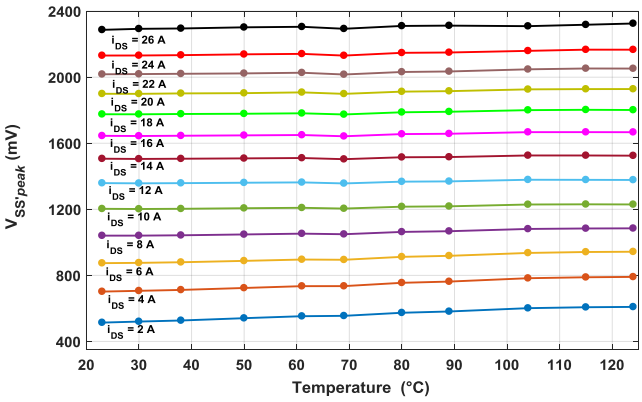

Fig. 15. Measured peak voltage $v_{SS'peak}$ over parasitic source inductance as function of temperature and current

Fig. 15 illustrates the measured peak voltage $V_{SS'}$ variations with temperature and load current across the parasitic inductance between source and auxiliary source connection, according to the methodology described in Section II. This voltage is a signal proportional to di_{DS}/dt. A very low sensitivity to temperature variation is evident, highlighting the difficulty in using this signal as TSEP. Indeed, the voltage variation due to load current is more significant, and hence decoupling the temperature effect from the load would be more difficult.

Figs. 16-17 show the measured integrated voltage $\int V_{SS'} \cdot dt$ over the parasitic source inductance as function of drain-source current and temperature, respectively. Although a very low sensitivity to temperature variation makes this signal impractical as TSEP, the very good linearity makes it a good candidate for device current monitoring, providing a practical method for current effect decoupling for other current-dependent TSEPs such as the on-state voltage.

Based on the measurement results of the four candidate TSEPs, it is evident that di_{DS}/dt is not very sensitive to temperature variation, and hence this parameter would not be suitable for online junction temperature monitoring. In contrast, both the threshold voltage V_{th} and drain-source on-state voltage $V_{DS,on}$ exhibit good temperature dependency. However, V_{th} is shown to be independent of device (load) current, which makes it attractive for practical implementation. While $V_{DS,on}$ is also highly dependent on device current, the relationship is quite linear, and hence by employing the device current measurement technique shown in Fig. 16, it is possible to decouple the load effect. Thus, $V_{DS,on}$ may also be a promising candidate TSEP for online junction temperature. While the internal gate resistance variation is also independent of device current, its sensitivity is relatively low and the signal-to-noise by employing this parameter as online junction temperature would be poor. This may compromise the quality of online monitoring in the electronically noisy environment.

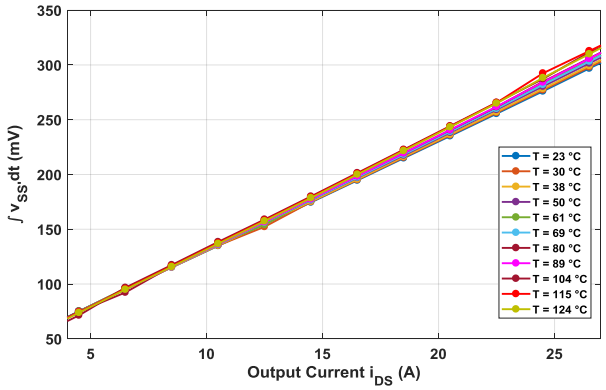

Fig. 16. Measured integrated voltage $v_{SS'peak}$ over parasitic source inductance as function of drain-source current for different values of temperature

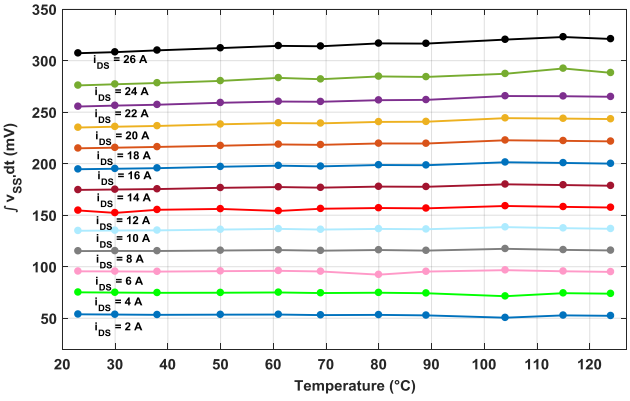

Fig. 17. Measured integrated voltage $v_{SS'peak}$ over parasitic source inductance as function of temperature for different values of drain-source current

CONCLUSION

The paper has reviewed the use of temperature sensitive electrical parameters for online temperature estimation in SiC power MOSFETs. Four TSEP candidates have been identified as most promising when taking into account criteria of sensitivity and linearity to temperature variation, dependence

on loading conditions as well as practicality in real-time measurement.

Practical circuits for measurement of the identified TSEPs have been described, designed and implemented in a high-resolution data acquisition board. The capabilities of the proposed acquisition board for online monitoring during converter operation have been demonstrated with extensive experimental validation using a double-pulse test setup and a commercial SiC module.

The quasi-threshold voltage v_{th} and the on-state voltage $v_{DS,on}$ show potentially good sensitivity to temperature variation and linearity over a wide operating range. Relatively lower sensitivity has been demonstrated for a TSEP based on the estimation of the internal gate resistance $R_{g,in}$. Both v_{th} and $R_{g,in}$ show relative insensitivity to load current variation. Very low sensitivity to temperature has been shown for di_{DS}/dt making this parameter unsuitable for temperature estimation.

It is worth noting that the ageing process can affect the measured parameters resulting in less accurate temperature estimation. Recalibration, or rescaling with ageing could be necessary. On the other hand, the availability of alternative TSEPs-based temperature estimation could be used to decouple the effects of ageing or even provide an ageing indicator. The possibility of continuously monitoring the state-of-health over device lifetime, tracking degradation and potentially provide prognostic information on the remaining useful life with the proposed TSEP monitoring concept will be explored in the future work.

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