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# PWM Harmonic Signature Based Islanding Detection for a Single-Phase Inverter with PWM Frequency Hopping

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**Abstract** -- Distributed generation (DG) has gained popularity in recent years due to the increasing requirement for renewable power sources. A problem that exists with DG systems is the islanding of DG units that creates safety issues for personnel as well as the potential for damage to utility infrastructure. Therefore, islanding detection methods are utilized to mitigate the risk of islanded operation of DG units. A new passive method of islanding detection based on the signature of the PWM voltage harmonics is proposed. The viability of the algorithm is investigated with the use of an analytical and time domain model of the inverter and further validated with experimental results. Furthermore, an extension of the detection scheme is proposed for use in multi-inverter scenarios composed of adaptive frequency hopping to eliminate unwanted tripping.

**Keywords**—*passive islanding detection, PWM harmonic signature, frequency hopping*

## I. INTRODUCTION

Islanding is defined as the condition where the distributed generator (DG) continues to operate with local loads after the utility grid has been disconnected [1]. Unintentional islanding is undesired since it is a hazard to utility workers and causes possible damage to equipment as a result of asynchronous re-closure. Asynchronous re-closure occurs when the utility recloses with an energized DG which is out of phase with the utility and can therefore cause large currents to flow, hence possibly damaging the DG converter infrastructure [2]. Islanding also has the potential to interfere with the power restoration service of the utility [3].

According to the IEEE1547 standard for interconnecting distributed resources with electric power systems, it is a requirement for grid connected DG systems to be able to detect islanding within 2 seconds and cease to energize the area electrical power system (EPS) that is coupled through the point of common coupling (PCC) [4].

As a consequence, a diverse range of islanding detection methods have been developed and reported in literature each with their merits and limitations.

The two main categories of islanding detection are passive and active methods. Passive methods consist of the detection of islanding through non-invasive means whereas active methods introduce a small perturbation to the grid current and thereby has some impact on power quality. The advantage of the active methods is the reduction/elimination of the non-detection zone (NDZ). In addition to the two main groups, there are also detection methods that rely on communication with the grid and inverter.

A variety of passive methods have been reported in literature such as over/under voltage protection (OVP/UVF) and over/under frequency protection (OFP/UF) methods [3]. These basic types of detection methods have a large NDZ and therefore are not sufficient in most applications of DG systems. Other types of passive detection methods include voltage phase jump [5], harmonic voltage or current detection methods [6] as well as the passive method proposed in [7] which monitors the oscillations in rate of change of frequency at the PCC.

The harmonics based methods consist of either detecting change in the total harmonic distortion [6], detecting changes in the individual low order harmonics [8], or monitoring the changes in the switching harmonics due to the PWM operation of the inverter [10].

A few examples of active methods of detection are, slide-mode frequency shift (SMS) [11], active frequency drift and Sandia frequency shift (SFS) [11-14], Sandia voltage shift (SVS) [11], methods based on impedance measurement by harmonic injection [15-18], impedance measurement by output power shift [8] and impedance measurement by active frequency drift [9].

Other types of active methods include DQ-frame based feedback methods [19]; methods based on the perturbation of the reactive power [20, 21, 22] and second order generalized integrator (SOGI) PLL based methods [23] that introduce a small disturbance in the phase of the inverter current. A more recent method involves a multi principle local area measurement and communication based scheme where the islanding method is applied to a refinery power system [24].

Although active methods significantly decrease the NDZ, they share the disadvantage of degrading the power quality to some degree and some of the active methods have the disadvantage of causing instability to the grid in multi-inverter scenarios [25]. Furthermore, with the common prevalence of photovoltaic (PV) inverter systems, there may be situations where the islanding detection mechanisms of multiple inverter systems which are connected to the same utility, fail to detect islanding due to the interaction between these systems [2].

## II. PROPOSED METHOD

This paper presents a new detection technique that has been developed to overcome the drawbacks of islanding detection schemes reported in literature. The proposed islanding detection method consists of monitoring the frequency spectrum of the voltage at the PCC ( $V_{PCC}$ ). When islanding occurs, the shunt impedance at the PCC for high frequencies increases and this results in the increase of PWM voltage harmonics. A fast Fourier transform (FFT) is performed on the  $V_{PCC}$  signal for each cycle of the fundamental frequency after which the switching harmonic sidebands are compared with the noise floor to obtain a relative magnitude. A look up table (LUT) is utilized to compare the obtained magnitude to the trip value for the given modulation index. The decision logic then determines whether islanding has taken place and if so, the inverter is shut down. Two sideband harmonic components are used as the signature of the inverter's harmonics for the detection of islanding which provides a degree of immunity from false tripping due to external noise sources.

Whilst PWM harmonic voltage based anti-islanding has been reported in [10], no experimental demonstration has been performed. The proposed method differs from the method reported in [10] through utilisation of multiple harmonic components, thereby detecting the unique signature of the inverter under consideration for the purposes of noise immunity. Further extension of the algorithm whereby the PWM frequency is varied upon encountering multi-inverter interference is also investigated.

Furthermore, the limitations common to both the proposed method and the method reported in [10] due to large capacitive loads, as well as the positive effect of series impedance of the capacitive load on the ease of detection are investigated.

## III. MODELLING OF INVERTER LCL FILTER AND UTILITY GRID

In order to analyze the behaviour of the grid-connected inverter upon islanding, it is necessary to establish a model of the system at the high frequency level. The schematic given in Fig. 1 represents the inverter's LCL filter, the RLC load and the grid. The RL represents a combination of the most common resistive and inductive loads while C represents capacitance for any power factor correction or harmonic filtering. The grid can be considered a short circuit at the high frequencies of interest due to the large capacitor banks that are common for power factor

correction. However, the series impedance ( $Z_{grid}$ ) of the power lines must be considered in the model. The circuit breaker ( $SW_1$ ) represents the breaking point when islanding occurs.

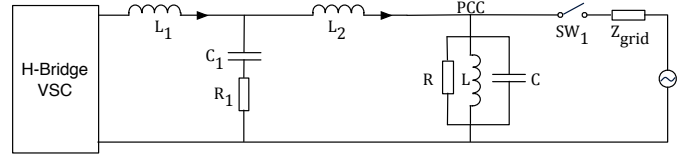


Fig. 1. Equivalent model of inverter, RLC load and grid

The high frequency voltage harmonics are generated in the inverter due to the voltage source converter's (VSC) PWM operation and the individual harmonic components can be quantified as given in (1) [26]. For the H-bridge inverter under investigation, unipolar PWM modulation scheme is utilized and therefore the harmonics appear centred around integer multiples of the switching frequency (10 kHz), starting from double the switching frequency onwards as illustrated in Fig. 2, where the harmonic orders are normalized to the 50 Hz fundamental. As can be seen, the two side bands at 20 kHz  $\pm$  50 Hz have the highest magnitude.

$$V_{inv}(t) = V_{dc} M \cos(\omega_o t) + \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} J_{2n-1}(m\pi M) \cos([m+n-1]\pi) \cos(2m\omega_{sw}t + [2n-1]\omega_o t) \quad (1)$$

According to IEEE standard 519-1992, current harmonics over the 35<sup>th</sup> order generated by the inverter must be lower than 0.3% of the maximum load current for short circuit current ratios lower than 20. Therefore the inverter LCL filter can be designed to meet these regulations. For the purposes of analysis and experiment, the following inverter specifications given in Table I are used.

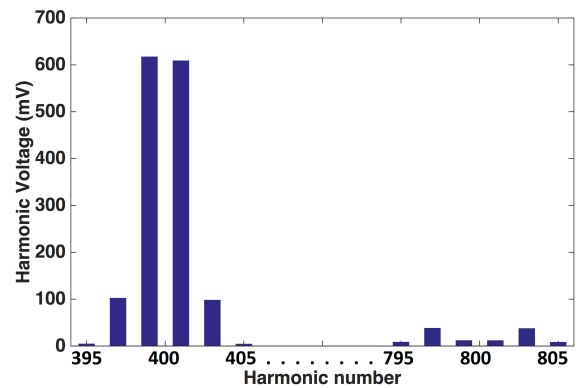


Fig. 2. Harmonics of unipolar PWM VSC switching at 10 kHz

TABLE I. INVERTER SPECIFICATIONS

Inverter active power	$L_1$	$L_2$	$C_1$	$R_1$
2.2 kW	5 mH	145 $\mu$ H	6.8 $\mu$ F	1.2 $\Omega$

For the ease of analysis, the inverter consisting of the VSC and LCL filter can be simplified by a Thévenin equivalent circuit as shown in Fig. 3 where  $e_{th}(h)$  and  $Z_{th}(h)$  are given by (2) and (3) respectively. The impedance seen by the inverter before and after islanding for the parallel RLC load is defined by (4) and (5). Therefore the voltage harmonics present at the PCC before and after islanding can be evaluated as given in (6) and (7).

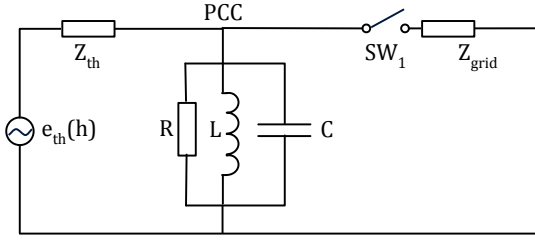


Fig. 3. Thévenin equivalent circuit of inverter with RLC load

$$e_{th}(h) = \frac{1 + j\omega_h R_1 C_1}{1 + j\omega_h R_1 C_1 - \omega_h^2 L_1 C_1} |V_{inv}(h)| \quad (2)$$

$$Z_{th}(h) = \frac{j\omega_h \left\{ \begin{array}{l} L_1(1 + j\omega_h R_1 C_1) + \\ L_2(1 + j\omega_h R_1 C_1 - \omega_h^2 L_1 C_1) \end{array} \right\}}{1 + j\omega_h R_1 C_1 - \omega_h^2 L_1 C_1} \quad (3)$$

$$Z_{pre-islanding}(h) = R \parallel L \parallel C \parallel Z_{grid} \quad (4)$$

$$Z_{post-islanding}(h) = R \parallel L \parallel C \quad (5)$$

$$\left| V_{PCC-pre-islanding}(h) \right| = \frac{\left| \frac{e_{th}(h)}{Z_{th}(h) + Z_{pre-islanding}(h)} \right|}{\left| Z_{pre-islanding}(h) \right|} \quad (6)$$

$$\left| V_{PCC-post-islanding}(h) \right| = \frac{\left| \frac{e_{th}(h)}{Z_{th}(h) + Z_{post-islanding}(h)} \right|}{\left| Z_{post-islanding}(h) \right|} \quad (7)$$

It is clear that during islanding, the impedance at the PCC for switching frequencies increases due to the absence of the low impedance shunt component of the grid. It is this increase that also causes an increase in the voltage harmonics that appear at the PCC, which is the basis of the detection method. However, as the capacitance of the RLC load increases, the post-islanding impedance for the switching frequencies decreases. Therefore the difference

between the highest level of non-islanded state voltage ripple and islanded state voltage ripple reduce to levels that are not detectable for higher values of load capacitance.

IEEE standard 929 states that the islanding detection method must be able to detect islanding for an RLC load that is resonant at the grid frequency and having a quality factor under 2.5. In order to quantify the detectable zone as a function of load capacitance  $C$ , the following Fig. 4 is presented whereby the grid impedance,  $Z_{grid}$ , at high PWM frequencies is assumed to be zero for a 2.2 kW power level. The figure shows the variation of harmonic voltage difference  $\Delta V(h)$  before and after islanding for an RLC load resonant at 50 Hz.

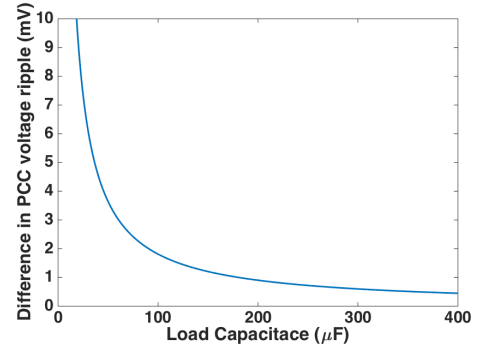


Fig. 4. Difference in voltage ripple (20.05 kHz) for an RLC resonant load with varying load capacitance

Although the ideal grid condition of 0  $\Omega$  for high frequencies has been assumed for analysis of the detection zone, in practice the series grid inductance at the switching frequency will be a finite value, which sets the baseline value of the voltage harmonics above which the trip threshold lies. Furthermore, in reality the parallel RLC load will have a series impedance component which represents cable effect at the switching frequency as well as ESR of the load capacitance and load inductance as shown in Fig. 5.

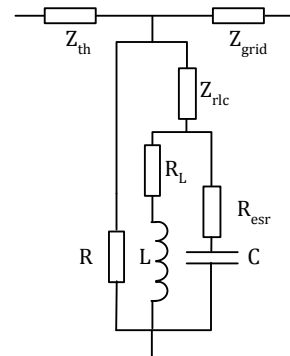


Fig. 5. RLC load with parasitic impedance elements

TABLE II. CONDITIONS FOR THE RIPPLE VOLTAGE ANALYSIS

Symbol	Description	Value
<b>P</b>	Inverter active power	2.2 kW
<b>R</b>	Load resistance	26 $\Omega$

Symbol	Description	Value
C	Load capacitance	0 to 350 $\mu$ F sweep
$R_L$	Inductor series resistance	10 m $\Omega$
$R_{esr}$	Capacitor ESR	10 m $\Omega$
$ Z_{rlc} (20 \text{ kHz}) $	RLC series impedance	0 to 5 $\Omega$
$ Z_{grid} (20 \text{ kHz}) $	Grid impedance	2.5 $\Omega$
M	Modulation index	0.62

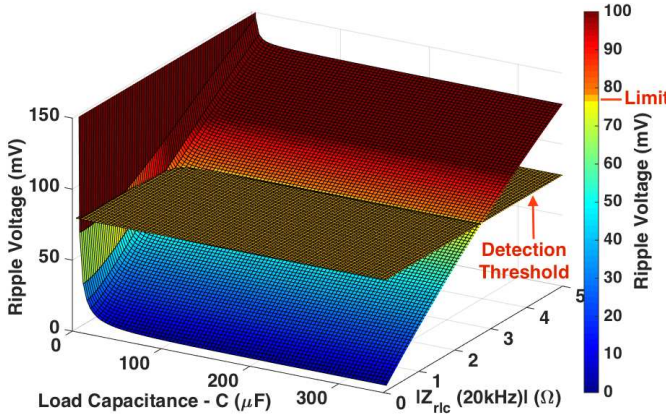


Fig. 6. Voltage ripple after islanding as a function of load capacitance (C) and series impedance at 20 kHz ( $|Z_{rlc} (20 \text{ kHz})|$ )

Fig. 6 shows the variation in post-islanded switching voltage ripple (20.05 kHz) present at the PCC for the conditions given in Table II for an RLC load resonant at 50 Hz (The value for L is chosen for resonance at 50 Hz).

In Fig. 6, islanding is detectable if the magnitude of the post islanding voltage ripple lies above the detection threshold plane. The detection threshold plane is defined as a value that is 5% larger than the worst-case value of voltage ripple present under normal operation (i.e. when no RLC load is connected to the inverter and the inverter is not islanded). It is found that islanding is detectable for all values of series impedance,  $|Z_{rlc} (20 \text{ kHz})|$  for load capacitances that are under 3.65  $\mu$ F. For series impedances higher than 2.75  $\Omega$ , islanding is detectable for all values of load capacitance. The effect of spurious noise that can be present in the sensed voltage is minimized by comparing both harmonic components (19.95 kHz and 20.05 kHz) to the threshold values.

#### IV. ISLANDING DETECTION

##### A. Detection Algorithm

The block diagram of the islanding detection algorithm is illustrated in Fig. 7 and the detailed flow chart is given in Fig. 8 (a). Voltage at the PCC ( $V_g$ ) is first attenuated after which it is band-pass filtered. This stage removes the fundamental (50 Hz) signal thereby maximising the ADC's dynamic range as well as removing out-of-band signals that are not of interest. The ADC digitises the filtered signal after which the signal is processed in the FPGA. The data processing is overseen by the control logic, which first takes 8192 data samples (20 ms of data = 1 cycle of the fundamental) from the ADC to the FIFO memory and

initiates the FFT transform. The higher sampling frequency and hence the 8k size for the FFT is used to increase the FFT process gain, thereby increasing the signal-to-noise ratio (SNR) as the design is a proof of concept. For actual implementation, the sampling rate and resulting FFT size may be reduced dramatically. After the data is processed through the FFT logic, data points except the harmonic sideband components are averaged to obtain the noise floor. The level of the noise floor is subsequently checked for any interference as a form of sanity check. The final part of the algorithm is the comparator logic, which compares the 2 harmonic components (19.95 kHz and 20.05 kHz) to the detection threshold in the LUT (predefined as worst-case ripple +5% for the operating power range). If both components are above the trip limit, the logic asserts the islanding detected signal. This process repeats itself every  $\sim 20$  ms (20 ms capture window + FFT process time which depends on the FPGA speed and actual FFT size used in final implementation) and therefore the typical detection time is also  $\sim 20$  ms.

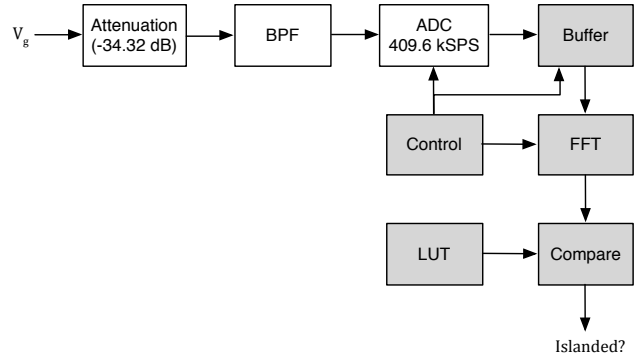


Fig. 7. Block diagram of islanding detection algorithm

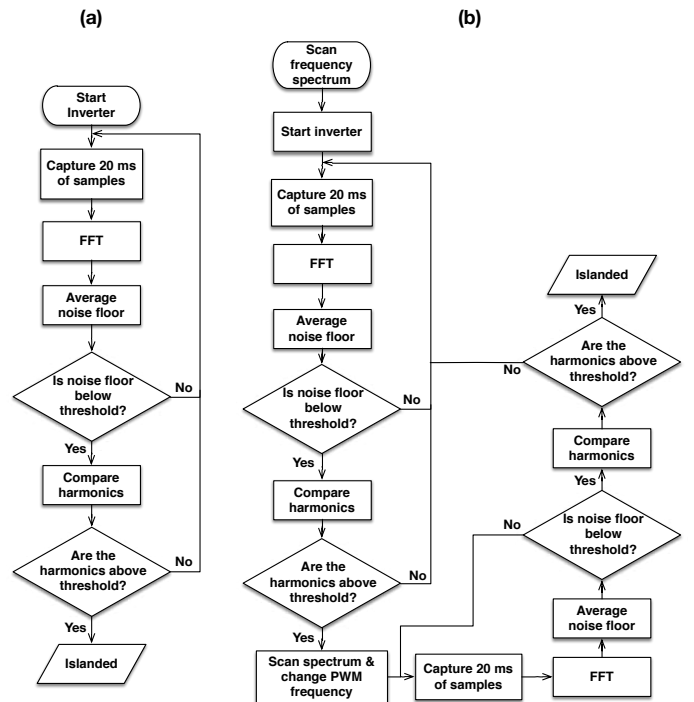


Fig. 8. (a) Islanding detection algorithm. (b) Islanding detection algorithm for multi-inverter operation

### B. Noise immunity from other switching converters

It is possible that other power converter systems operating nearby to the inverter could cause a false trip if the external systems operate at the same switching frequency, thereby causing the magnitude of the voltage harmonics to exceed the threshold value. If noise immunity from other switching converters is a design criterion, the detection logic can be configured to dynamically change the inverter PWM frequency for the subsequent cycle of fundamental frequency upon detection of the first trip condition. The 2<sup>nd</sup> PWM modulation frequency to be ‘hopped’ to is determined by scanning the adjacent spectrum (20 kHz  $\pm$  4 kHz), and selecting a frequency that has a low level of noise present, and is an integer multiple of the grid frequency. If the spectrum of the subsequent cycle also matches the sideband characteristics for islanding condition, it can be determined that actual islanding has taken place and inverter operation ceased. The detailed flow chart of the islanding detection algorithm for multi-inverter operation is illustrated in Fig. 8 (b).

It must be noted that the amount of inverters that can be supported by the islanding detection algorithm is limited to the spectral bandwidth (20 kHz  $\pm$  4 kHz in this instance) and therefore optimum utilization may be obtained by interleaving the spectrum. For instance, if  $\pm 3$  sideband harmonics around 20 kHz are considered (19.75 to 20.25 kHz), it is observed that the harmonics are separated by 100 Hz and hence occupies a bandwidth of 500 Hz. Therefore, it is possible to interleave another inverter between the harmonic spurs that are separated by 100 Hz, yielding a total bandwidth of 600 Hz for 2 inverters. Therefore, the 16 kHz - 24 kHz band can support 13 pairs of inverters, or 26 in total. As an example, in a residential application, each utility phase in a neighbourhood may contain 26 separate inverters. Each inverter must therefore scan the available band and self-allocate a suitable switching frequency before initiating power switching.

### V. SIMULATION OF ISLANDING ALGORITHM

The algorithm has been simulated in MATLAB using the SimPowerSystems toolbox to validate its performance. The first simulation test case consists of islanding under an RLC load that is resonant at 50 Hz where the RLC parameters are listed in Table III. Furthermore, the PWM frequency hopping multi-inverter (2 inverters simulated) islanding detection algorithm has been validated in Simulink for which the conditions are also shown in Table III.

TABLE III. SIMULATION TEST CONDITIONS

Parameter	RLC Load (Resonant) Test	Multi Inverter Test
R	26.18 $\Omega$	13.09 $\Omega$
L	33.77 mH	Not Used
C	300 $\mu$ F	Not Used
R <sub>L</sub>	10 m $\Omega$	N/A
R <sub>esr</sub>	10 m $\Omega$	N/A

Parameter	RLC Load (Resonant) Test	Multi Inverter Test
Z <sub>rlc</sub> (20 kHz)	2.75 $\Omega$	N/A
Z <sub>grid</sub> (20 kHz)	2.5 $\Omega$	2.5 $\Omega$

#### A. Simulation case 1 – RLC resonant load

Since the RLC load is resonant at 50 Hz, the islanding condition lies in the NDZ of the OVP/UVP and OFP/UFP methods. Fig. 9 and Fig. 10 show the V<sub>PCC</sub>, inverter current and V<sub>PCC</sub> spectral content variation over time. It can be observed that the islanding is successfully detected after 20 ms (1 electrical cycle) after islanding occurs.

After islanding, the magnitude and the frequency of V<sub>PCC</sub>’s fundamental component continue to be unaffected, but the voltage ripple of the 19.95 kHz component (and 20.05 kHz) increases to 77 mV from 49 mV after islanding. Therefore islanding is successfully detected, as the detection threshold is 76 mV.

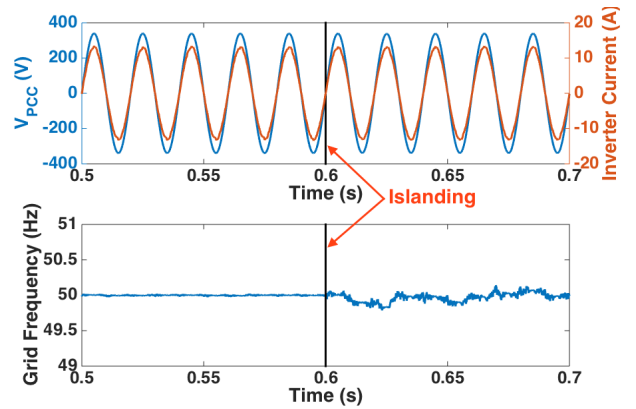


Fig. 9. V<sub>PCC</sub>, inverter current and V<sub>PCC</sub> frequency (RLC Load)

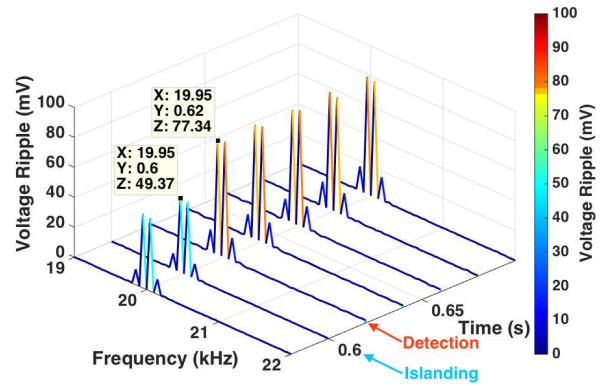


Fig. 10. Time domain plot of the V<sub>PCC</sub> spectral content (RLC Load)

#### B. Simulation case 2 – detection of islanding under multiple inverter operation

In the situation where immunity from false tripping due to other converters operating with the same PWM frequency is required, the adaptive PWM hopping method can be used at the cost of increasing the detection time from  $\sim$ 20 ms to  $\sim$ 40 ms (2 electrical cycles).

The simulation can be summarized as follows, where the device under test in which the islanding detection algorithm

is applied is referred to as ‘Inverter 1’ and the external system that causes interference is referred to as ‘Inverter 2’.

Initially ‘Inverter 2’ is non-operational and ‘Inverter 1’ feeds power to the utility grid. At  $t = 0.6$  s, ‘Inverter 2’ starts operating at the same 10 kHz device switching frequency (20 kHz harmonics generated), which causes the harmonics seen at the PCC to increase as shown in Fig. 11.

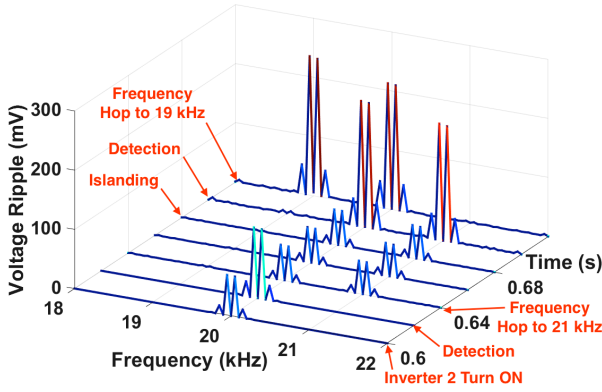


Fig. 11. Time domain variation of the  $V_{PCC}$  spectral content (2 inverter case)

At  $t = 0.62$  s, upon detection that the harmonic voltage limits have been exceeded, the islanding prevention algorithm of ‘Inverter 1’ scans the adjacent spectrum for a suitable frequency with low interference, and changes its PWM frequency to 10.5 kHz (harmonics at 21 kHz). After the subsequent electrical cycle (at  $t = 0.64$  s), the FFT of  $V_{PCC}$  reveals that the harmonic spectrum for ‘Inverter 1’ is below the limits that would be identified as being islanded. Therefore ‘Inverter 1’ continues to operate at 21 kHz. At  $t = 0.68$  s, actual islanding occurs where the breaker opens and therefore the 2 inverters (both operating at 2.2 kW) continue to power the local resistive load. At  $t = 0.7$ , the islanding detection algorithm detects the increased voltage harmonics and therefore changes the PWM frequency to 9.5 kHz (causing voltage harmonics to appear at 19 kHz). In the following electrical cycle ( $t = 0.72$ ), it can be seen in Fig. 11 that despite the frequency jump, the harmonics are still at the increased level (234 mV). Therefore, at  $t = 0.72$  s, islanding is detected since the algorithm detected increased harmonics in 2 consecutive cycles of the grid voltage.

The proposed algorithm for islanding detection has therefore been shown to provide immunity from false tripping due to external power converters operating at the same PWM frequency.

## VI. DESIGN OF ISLANDING DETECTION HARDWARE

### A. Voltage detection hardware design

The detection of the small signal high frequency components present at the PCC can be achieved by sampling the grid voltage through an ADC converter. However, since most commercially available voltage transducers are not able to detect signals with bandwidth exceeding 20 kHz, a resistor divider based circuit is designed where the isolation between the high voltage side

and the low voltage controller is introduced after the ADC stage with the use of ADUM1400 digital isolators.

The resistor divider attenuates the grid voltage by a factor of 52 (34.32 dB) in order to reduce the peak value of the signal to under  $\pm 7$  V so as to be compatible with the analogue signal conditioning circuit.

In order to maximize the dynamic range of the ADC, the fundamental grid frequency component is removed by filtering and the remaining high frequency signal is amplified prior to digitisation. An active band-pass filter was designed for this purpose, which also serves as the anti-aliasing filter for the ADC. Fig. 12 shows the frequency response of the 4<sup>th</sup> order multiple feedback Chebyshev band pass filter that was designed for the filtering. Since the dominant switching harmonics appear at 20 kHz, the pass-band of the filter was chosen to be between 16 kHz-24 kHz with a gain of 34 dB and attenuation at the fundamental frequency (50 Hz) of -87 dB.

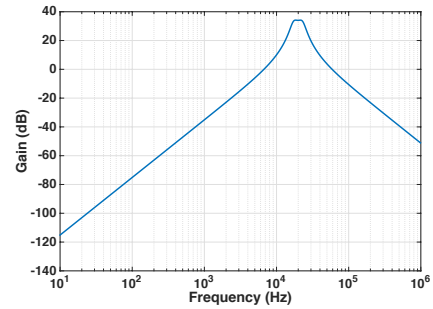


Fig. 12. Voltage sensing circuit band pass filter frequency response

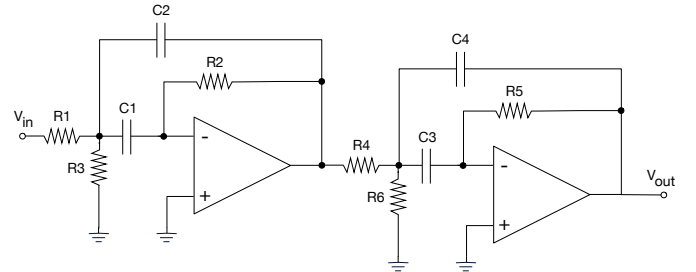


Fig. 13. Band pass filter schematic

This configuration allows the full dynamic range of the ADC to be utilized whilst preventing saturation of the ADC at the highest value of ripple voltage (i.e. when islanding takes place with a purely resistive load). The schematic of the op-amp based filter circuit is shown in Fig. 13. A 16-bit SAR ADC converter (ADS8422) thereafter digitises the signal with a sampling frequency of 409.6 kSPS. The ADC output is carried in an 8-bit data bus and therefore the data bus is clocked at twice the sampling frequency. The ADC is interfaced through three ADUM1400 digital isolator chips, which provide the galvanic isolation required for safety. An NI cRIO-9082 controller is used for processing the data for the experimental demonstration.

### B. Inverter current detection circuit hardware design

A current sensing circuit has been designed with similar band pass characteristics as the voltage sensing circuit with an independent ADC. Although the current sensing circuit is not used in the detection of islanding, it serves the purpose of measuring the grid impedance at 20 kHz frequency for analysis purposes.

The current sensing element consists of a 10 mΩ shunt resistor through which the inverter current passes. The voltage signal that appears across the resistor due to the PWM ripple current is small in magnitude and therefore the succeeding filter stage is designed with a high gain at the pass band frequency. For instance, if the ripple current magnitude is assumed to be 0.3% of the fundamental current, the rms value of voltage present across the shunt resistor due to the ripple current is only 275 μV.

The filter circuit consists of a 6<sup>th</sup> order multiple feedback Chebyshev band pass filter with a pass band of 16 kHz-24 kHz, pass band gain of 60 dB and attenuation of -115.7 dB at 50 Hz. Since the filter contains 6 poles, it is implemented with 3 op-amps.

## VII. EXPERIMENTAL RESULTS

The experimental setup used for the islanding tests is shown in Fig. 14. The inverter is connected to the grid and the load via a low frequency (50 Hz) isolation transformer. A dedicated isolation and data acquisition board is designed and constructed. The inverter control and island detection algorithms are implemented on NI CRIO-9082.

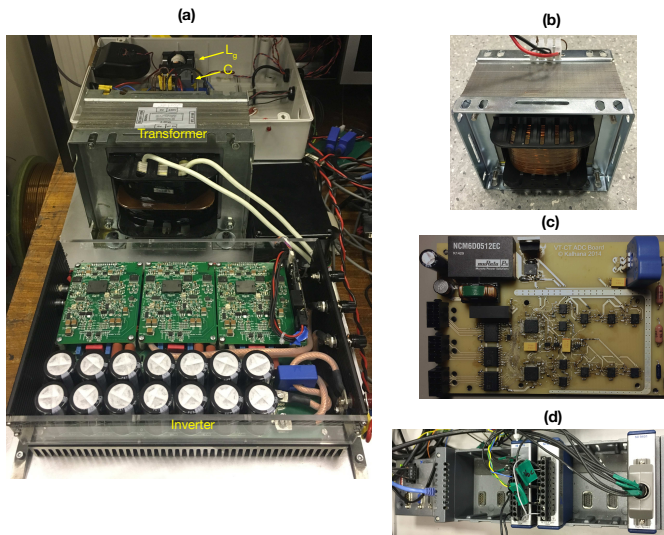


Fig. 14. Experimental setup that was used for islanding test. (a) Low frequency transformer based inverter. (b) Inductor (318 mH) used for RLC test. (c) Islanding detection data acquisition circuit (d) NI cRIO-9082 used for data processing and detection algorithm

### A. Estimation of grid impedance

The magnitude of the grid impedance at 20 kHz ( $|Z_{\text{grid}}(20 \text{ kHz})|$ ) can be estimated by measuring the magnitude of the high frequency components of  $V_{\text{PCC}}$  and  $I_{\text{g}}$  during operation of the inverter when the RLC load is not connected. The results that were obtained for the utility grid

of the laboratory when the inverter was operating at 2.2 kW are given in Table IV.

TABLE IV. ESTIMATED GRID IMPEDANCE FROM MEASURED VALUES OF VOLTAGE AND CURRENT RIPPLE

Parameter	Value	Parameter	Value
$ V_{\text{PCC}}(19.95 \text{ kHz}) $	73.4 mV	$ V_{\text{PCC}}(20.05 \text{ kHz}) $	72.2 mV
$ I_{\text{g}}(19.95 \text{ kHz}) $	30.0 mA	$ I_{\text{g}}(20.05 \text{ kHz}) $	30.1 mA
$ Z_{\text{grid}}(19.95 \text{ kHz}) $	2.44 Ω	$ Z_{\text{grid}}(20.05 \text{ kHz}) $	2.39 Ω

The experimentally derived high frequency grid impedance value has been utilized as a starting point for determining the worst-case ripple magnitude. It must be noted that in practical realization of the system, the maximum acceptable grid impedance for high frequencies must be determined on a case-by-case basis dependant on the grid configuration (for which the detailed analysis is beyond the scope of this paper).

### B. Resistive load islanding test

Experimental validation has been carried out for an islanding condition with a purely resistive load (26.2 Ω) at 2.2 kW, and the results are depicted in Fig. 15 and Fig. 16. In Fig. 15, the band pass filtered ADC captured data is shown together with the magnitude of the 19.95 kHz voltage harmonic component (from the FFT of the band pass filtered signal). The islanding takes place at  $t = 0.011 \text{ s}$ , and the system detects the islanding at 0.02 s (9 ms detection time). Since the FFT is performed for each cycle (20 ms), the first FFT magnitude value is lower than the steady-state islanded magnitude since the FFT time window contains both islanded and non-islanded data in the first cycle. It must be noted that the system is allowed to operate after the islanding is detected to observe the behaviour under islanding condition. Since the resistive load is not resonant at 50 Hz and due to the difficulty in having an exactly matched active load in the experiment, the dynamic behaviour of the system is such that the inverter output frequency increases after the islanding and the inverter is subsequently shut down after a few cycles for protection. Of course, it is possible to implement droop control after the islanding for stable islanded operation, but this is beyond the current scope. Nevertheless, it is evident that the resistive load islanding is detectable.



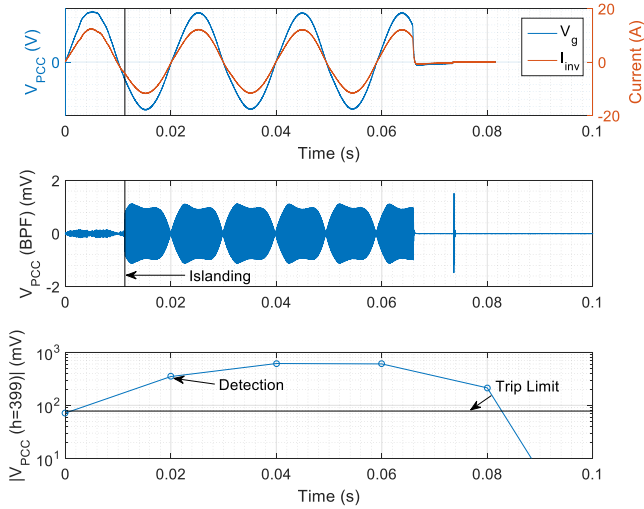


Fig. 15. Islanding test waveforms for resistive load test (top: voltage and inverter current at PCC, middle: the band pass filtered signal from the ADC, bottom: the FFT magnitude of the 19.95 kHz component)

Fig. 16 shows the pre and post islanding (steady state) voltage ripple. The pre-islanding voltage ripple of the 19.95 kHz component is 71.57 mV and under post islanding, it reaches 612.8 mV. The values obtained experimentally compare to the analytical prediction of 70.5 mV and 444.3 mV, and to the numerical simulation results of 72.19 mV and 442.2 mV for pre- and post-islanding cases, respectively. It can be seen that the predicted and measured pre-islanding ripple matches. The higher value of post islanding voltage ripple can be attributed to the series inductance of the load resistor bank, which is neglected in analytical prediction and in numerical simulation.

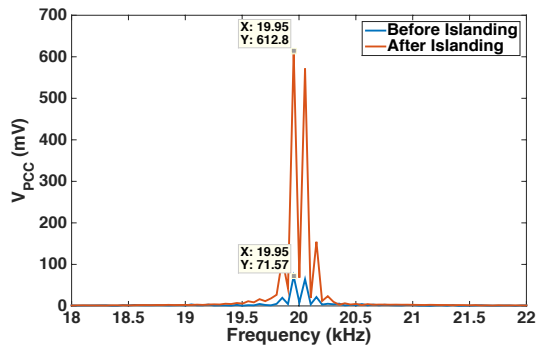


Fig. 16. Islanding test frequency spectrum for resistive load test

### C. RLC load islanding test

The RLC load-based islanding detection test has been carried out with the conditions depicted in Table V for an inverter power output of 2.2 kW. The resulting waveforms are presented in Fig. 17 and the spectrum of the switching frequency harmonics in Fig. 18. Islanding takes place at  $t = 0.051$  s and is detected at  $t = 0.06$  s (9 ms detection time). Similar to the resistive case, the first FFT output after the islanding contains both pre and post islanding data, and therefore the magnitude is initially lower than the steady-state islanded harmonic magnitude. Furthermore, at  $t = 0.075$  s, contact bounce due to arcing occurs on the relay that emulates the islanding and extinguishes at  $t = 0.082$  s. Although this contact bounce causes a transient in the

measured voltage for 7 ms, the experiment outcome is not affected. It can be seen that islanding is successfully detected for the RLC load under consideration. The pre-islanding voltage ripple of the 19.95 kHz component is 55.1 mV and after islanding, it reaches 132.7 mV. The values obtained experimentally compare to the analytical prediction of 57.6 mV and 131.2 mV for pre- and post-islanding cases, respectively. It is observed that the predicted and measured post-islanding ripples match better than the purely resistive test case. This is because the load resistor bank's series inductance is the reason for the large difference between the prediction and measurement that appears during the resistive load test. However, it can be seen that in the RLC load test, the capacitance is the dominant shunt component for high frequencies and therefore the series inductance of the load resistor has a negligible effect on the post-islanding ripple.

In simulations, the system when islanded with a RLC load that is resonant at 50 Hz is capable of continuous operation. However, during the experimental tests with an RLC load, it was observed that the system becomes unstable after  $\sim 0.5$  s of the islanded operation. This is attributed to the noise and other disturbances that occur in the experiment because the PLL and the current control loop is highly sensitive to these disturbances and therefore causes the voltage/frequency to drift beyond the safe limits.

TABLE V. RLC TEST CONDITIONS

R ( $\Omega$ )	L (mH)	C ( $\mu$ F)	R <sub>L</sub> ( $\Omega$ )	R <sub>csr</sub> (m $\Omega$ )	Z <sub>rlc</sub> (20 kHz)  ( $\Omega$ )
26.4	318	32.3	6.28	20	5

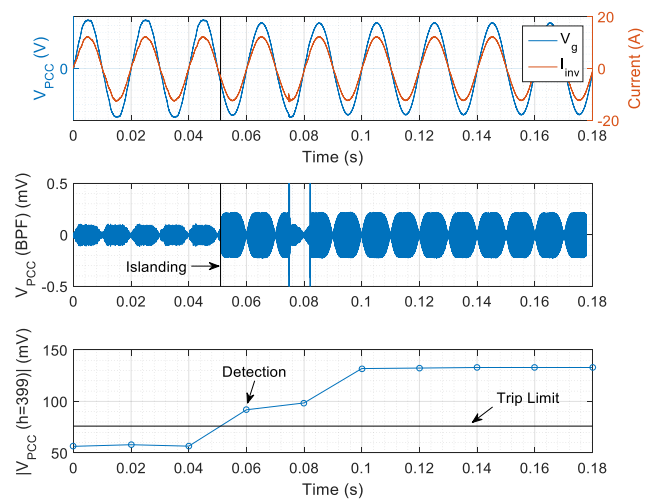


Fig. 17. Islanding test waveforms for RLC load test (top: voltage and inverter current at PCC, middle: the band pass filtered signal from the ADC, bottom: the FFT magnitude of the 19.95 kHz component)

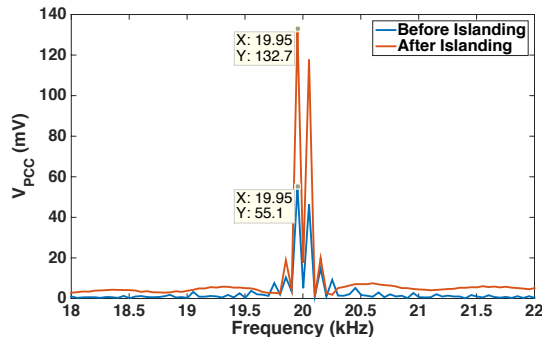


Fig. 18. Islanding test frequency spectrum for RLC load test

## VIII. CONCLUSION

A new islanding detection algorithm has been presented which has the advantage of multi-inverter compatibility compared to similar voltage harmonic monitoring methods.

Furthermore, the difficulty in detection for PWM harmonic based methods when capacitive loads are present has been analyzed and the detectable conditions as a function of the load's characteristics established. The algorithm has been simulated and two test cases demonstrated experimentally in hardware.

The detection hardware designed and demonstrated herein has been over-engineered since the exercise was purely as a proof-of-concept. It follows from analysis of the measured signal-to-noise ratio (SNR: 124 dB relative to 340 V peak grid voltage) and spurious free dynamic range (SFDR: 71 dBFS) of the prototype detector, that the hardware may be optimized in terms of ADC resolution and sample rate to achieve a trade-off between performance and cost. In particular, it is feasible to use the integrated 12-bit ADCs that are common in many low cost DSP/microcontrollers that are used in the control of grid converters.

The requirement for computing power can be minimized by either optimising the FFT length or by utilising an optimized version of an FFT algorithm that caters only for the frequency range of interest.

The proposed frequency hopping method may also be suitable for other active islanding detection schemes where low order harmonics are injected. Further investigations are required for its applicability in these schemes.

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