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Enabling Rapid Production and Mass Customisation of Electronics Using Digitally Driven Hybrid Additive Manufacturing Techniques

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Abstract— Additive Manufacturing processes can facilitate the rapid iterative product development of electronic devices by optimising their design and functionality. In addition, these methods present a number of potential advantages for improving the production speed and complexity of mass customised and bespoke electronics. In this paper, we present a new digitally driven hybrid fabrication process chain, capable of producing functional, multilayer electronics embedded within geometrically complex 3D printed structures. This has been achieved by interleaving stereolithography, micro-dispensing and surface mount assembly. The resultant combination of different template-less manufacturing techniques enables both the formation of multi-material circuits (conductors and dielectrics) and where the package housing encapsulates the electronics and forms part of the final 3D device. This paper also details the developments around depositing novel freestanding z-axis interconnects. A 555 timer circuit with flashing LED manufactured within a 3D pyramid was used as a demonstrator. The demonstrator contained circuits with feature sizes down to 170µm, and packaged components of 0603 size, a Small Outline Integrated Circuit (SOIC) and a SMD LED. In addition, flip chip packaging on 3D printed substrates has been demonstrated.

Keywords—Additive manufacturing; 3D printing; Flip-chip packaging; bespoke electronics; digitally driven fabrication

I. INTRODUCTION

The template driven nature of traditional electronics manufacturing requires volume production to achieve economic viability. This results in long pre-production timescales and a lack of customisation and versatility. During electronics manufacturing a wide range of materials including conductors and dielectrics must be used in order to generate complex circuitry and interconnects. Additive Manufacturing (AM) technologies, commonly termed 3D printing, are being widely publicised and promoted as the future of manufacturing [1][2]. Their direct digital manufacturing capability allows rapid production of unique and complex geometries directly from a 3D CAD model without the need for templates or molds. To-date the vast majority of research in this field has been conducted on the use of individual AM processes which, in isolation suffer limitations in the range of materials, processing speed and resolution for the resulting part. In order to enable truly functional products using 3D printing, the integration of multiple digitally driven processes is proposed as the solution to many of the current limitations arising from standalone AM techniques. Advantageous process characteristics can be combined and the differing material capabilities of these processes provides a larger range of applications [3] such as microfluidics, embedded sensor systems and electronics packaging.

This paper presents the integration of direct light projection (DLP) based Stereolithography (SL) and direct write (DW) technology, facilitating the creation of fully functioning, packaged electronic circuits from a digital model. This process chain is shown in figure 1. The combination of these manufacturing techniques coupled with mid-process cleaning, pick and placement of surface mount devices (SMDs) and thermal curing provides the multi-material, multi-process functionality required to produce high quality, high density printed electronics.

In recent years a few other hybrid processes have been proposed for the purpose of additively manufacturing electronic devices. All these methods either rely on depositing the electronic circuit after the 3D printed substrate has been manufactured or by directly embedding a pre-packaged printed circuit board (PCB) within the device. This does not allow true multilayer circuit capability or demonstrate packaging of fine pitch SMDs.

The University of Texas at El Paso were the first to demonstrate the fabrication of electronics through additive manufacturing by combining laser based top-down Stereolithography with direct writing of conductive inks. This was achieved by producing photopolymer substrates containing trenches for the circuit layout and through holes for

the off-axis connections [4]. The trenches were then filled using dispensing and the through holes pumped with a low viscosity conductive ink [5]. A three-dimensional accelerometer sensing circuit on a domed surface was produced to demonstrate the use of this approach [6]. Albeit this technique enables the fabrication of basic electronic devices it currently does not lend itself to high density multilayer electronics. This is due to the cavities for housing the components inhibiting placement of small surface mount devices and where only the surface of the substrate is used for placing the components. The channels are however required to constrain the low viscosity ink that would spread if not contained. Finally, the SMD interconnections have a low standoff that could potentially impact the mechanical reliability.

In 2012, Optomec and Stratasys demonstrated the manufacture of an unmanned aerial vehicle by printing conductors onto a 3D printed plastic part to generate the electric power for the propeller engine and also to print functional strain gauges [7]. This was achieved by coupling Fused Deposition Modelling with DW technologies, in particular aerosol jetting, a process which has been shown to allow the production of high resolution (10µm) electronic circuits. Again this approach was limited to depositing the functional electronics after the manufacturing of the printed plastic object has been completed however, this process has the ability to deposit on to a three-dimensional surface.

In 2016, Voxel8 will release a material extrusion system that couples both Fused Filament Fabrication (FFF) and dispensing within one machine [8]. This allows the direct generation of electronic circuits for rapid prototyping however the resolution of the FFF process is typically limited to 0.8mm features in the x and y axes due to the 0.4mm diameter nozzle. FFF also suffers from stair stepping issues in the z-axis due to the large layer thicknesses.

Recently, a concept for encapsulation of electronic circuits was proposed by Niese et al. by using the Additive 3D Molded Interconnect Device (ADDMID) process [9] and a doped

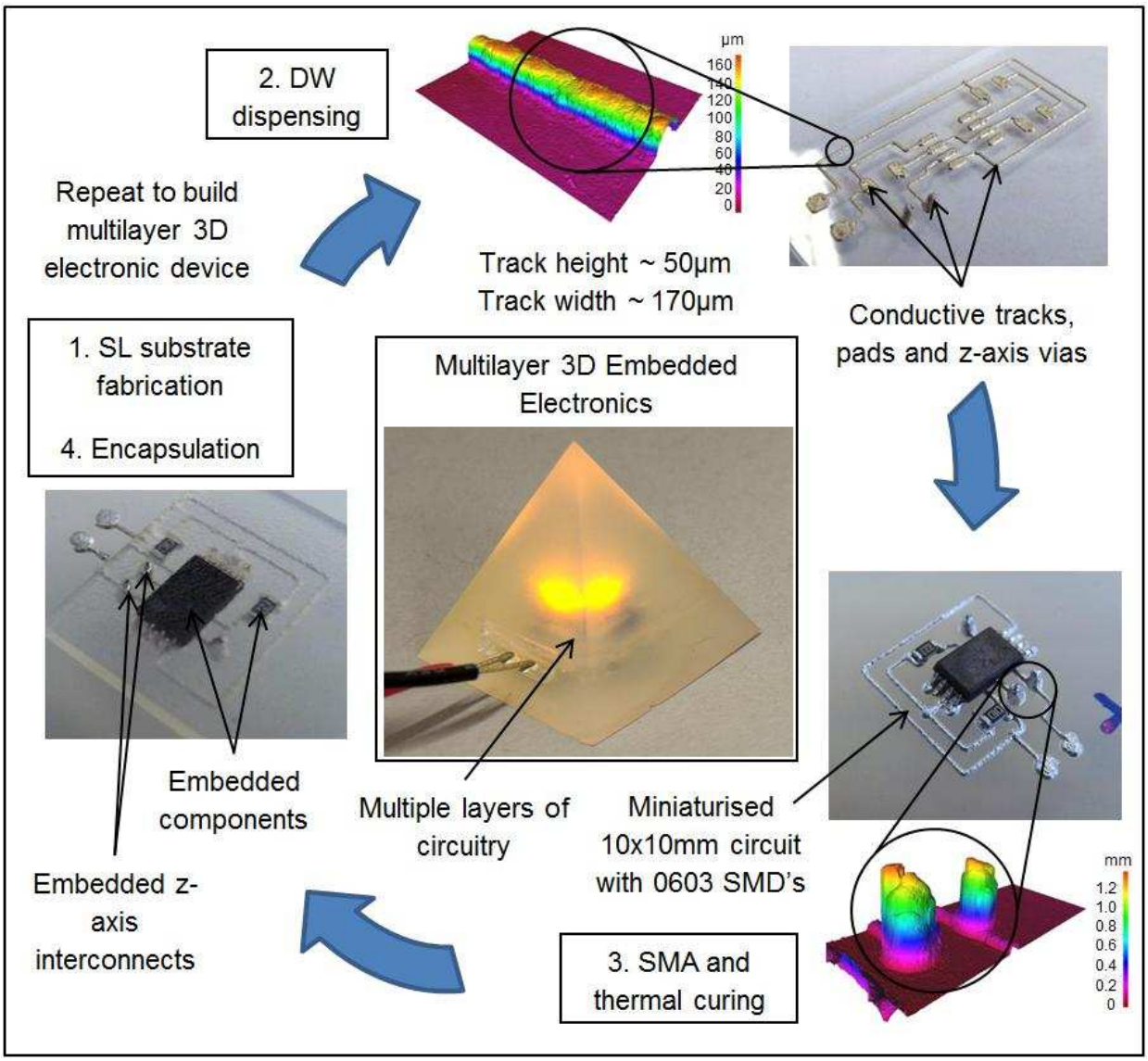

Fig. 1. Hybrid Additive Manufacturing process flow for electronics fabrication

photopolymer to encapsulate PCBs and create metallic channels to route a power source. Stereolithography replaces traditional injection molding to create polymer parts for laser processing. Despite its use of a laser for subtractive processing, the Molded Interconnect Device (MID) process remains a digitally driven process. Post processing is still required to pump fabricated channels with conductive ink and deposit interconnections between the encapsulated PCB and power source.

II. Hybrid Additive MAnufacturing of Electronics

A new technique has been developed to digitally fabricate fully functioning multilayer electronics using a unique combination of AM technologies. This process and material combination allows conductors to be printed on the surface of the photopolymer substrate, with no need for channels to control the flow of the silver conductive material. In addition, high aspect ratio z-axis through layer connections have been built to create contact between the layers of circuitry and embedded components. Multilayer freestanding pillars and the circuit traces are simultaneously printed and subsequently thermally cured prior to their encapsulation with corresponding components. The SL method, materials and dispensing processes are also compatible with surface mount pick and place technology, therefore permitting multilayer circuitry to be embedded within a cured photopolymer substrate. This compatibility is derived from the use of Isotropic Conductive Adhesives (ICAs) to form the conductive tracks, SMD interconnects and z-axis vias, allowing surface mount assembly directly onto the deposited conductors. The SL material is an acrylic formulation containing a photo initiator and inhibitor and is sensitive to ultraviolet (UV) irradiation. MakerJuice Labs SF resin was chosen for use in this process.

The SL system utilises a Digital Micromirror Device (DMD) as a dynamic mask, projecting UV light onto the underside of a transparent vat, resulting in selective photopolymerisation of the material. Advancement in DLP technology has significantly improved the resolution of DMD's making it suitable for micro-scale SL applications [10][11]. The LED projection approach results in a faster build time when compared with the traditional SL vector scanning methods. When this is combined with a 'bottom up' projection orientation it ensures a flat substrate surface finish with roughness average (R_a) values consistently below 200nm. The bespoke system shown in figure 2 is equipped with a 405nm light source with a projection resolution of 81µm for a 140mm x 87mm working area. The layer thickness is controlled through the software and values of both 100µm and 50µm have been investigated. The build platform height has been adapted to provide micrometer precision through the use of a depth micrometer to control the home position. Finally, a default average light intensity of 0.962mW/cm^2 was measured through the base of the vat and anti-stiction PDMS layer at the projection distance of 164mm from the lens, resulting in iteratively investigated optimum exposure times of 10 seconds per 100µm layer and 6 seconds per 50µm layer. The system

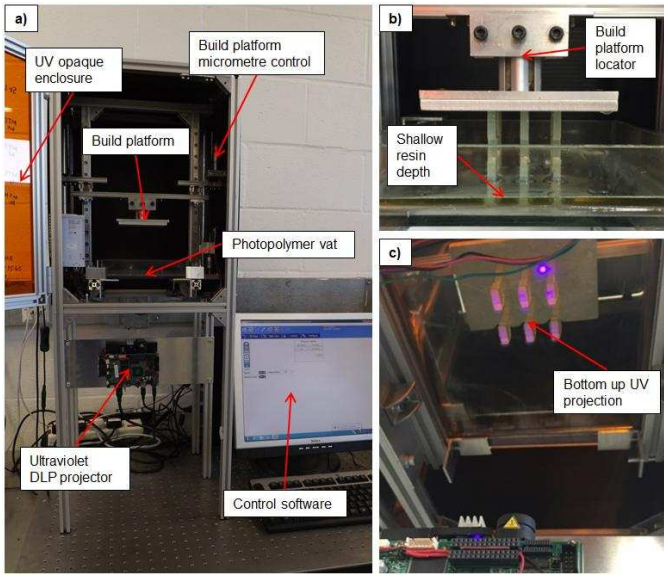

Fig. 2. a) Stereolithography apparatus setup and b) aligned build platform with c) bottom up UV projection capability

intensity can be increased to a maximum of 3.16mW/cm^2 however this causes much faster deterioration of the PDMS layer and can cause eventual degradation of the reflective surface of the DMD.

After producing a set number of layers the substrate is then passed into a mid-processing module that ultrasonically removes the uncured resin from the part. This mid-processing is a necessary step to interleave the SL stage with the following manufacturing steps. The part is cleaned in isopropyl alcohol which results in minimal part degradation and causes no change to the mechanical properties of the cured material.

Subsequently, the pneumatic dispensing system in figure 3, combined with a silver conductive epoxy is used to print the z-

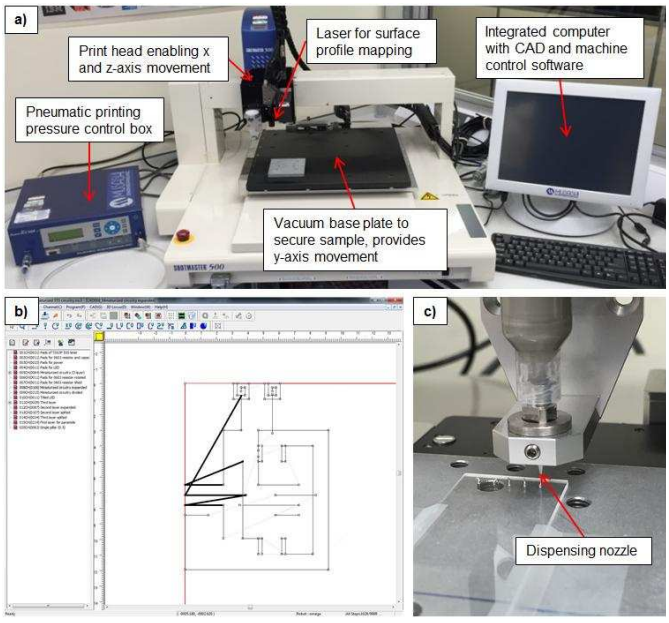

Fig. 3. a) Dispensing apparatus with b) integrated CAD capability and c) filled syringe and deposition nozzle

axis connections, SMD interconnects and conductive tracks, thereby eliminating traditional multistage template driven methods. Two commercially available silver based conductive adhesive materials, Epotek E4110-PFC and Epotek EJ2189, with maximum specified particle sizes of 20µm and 40µm respectively, were selected for deposition through nozzles with 250µm, 200µm and 100µm internal diameters. The low 104°C glass transition temperature (Tg) of the photopolymer substrate resulted in the selection of ICAs with low temperature curing characteristics. An investigation to determine an optimum curing regime below the Tg of the substrate found that 80°C for 3 hours gave the lowest resistivity, while causing no thermal degradation to the photopolymer. Sheet resistance of the traces was measured using a four point probe. The profile date of the tracks was measured using optical microscopy and inputted into a Matlab code to compute the cross-sectional area of the traces. Using this data and the measured sheet resistance the volume resistivity of both epoxies were calculated at $4x10^{-4}\Omega cm$ with this curing regime. This value is one order of magnitude lower than the manufacturer's data sheet [12][13]. Characterisation of this dispensing process found that the optimal trace printing parameters of 300kPa print pressure and 7mm/s print speed through a 100µm nozzle, resulting in a 169µm track width and 42µm height. Optimised pillar dispensing parameters achieved a free-standing z-axis pillar with the highest aspect ratio of 2.25:1 and average diameters of 672µm and average heights of 1518µm. This was achieved using a printing pressure of 80kPa, print speed of 7mm/s and nozzle diameter of 200µm. Both the best achieved dispensed traces and pillars were produced using the higher viscosity ICA, Epotek E4110-PFC. Compatibility with surface mount technology allows SMD placement directly onto the silver epoxy before thermal curing at 80°C, limiting the number of deposition stages and materials. After the components are placed and cured into position, the part can then be placed back into the SL apparatus to embed the current layer as shown in figure 4. Since a bottom-up projection system is used, the layering is achieved by pulling the part away from the projection window by a set-thickness thereby achieving a high degree of planarization and low surface roughness during the embedding. This results in an ideal surface on which to deposit subsequent layers. Embedding layers ranging in thicknesses from 1mm to 2mm were used to encapsulate 1206 and 0603 SMD's. The strength of the embedding layer adhesion to the substrate below was shown by a maximum tensile load just 1.6% lower at a 1mm layer thickness when compared to 1565N for a standard 100µm exposure. That increases to a 20% reduction over a 2mm exposure demonstrating a failure load of 1241N. A 60 second exposure was found to optimally cure a 1mm thick layer while 180 seconds was required to sufficiently polymerise a 2mm layer. This complete process can then be repeated numerous times to fabricate multilayer electronic devices, with the facility to create highly complexity.

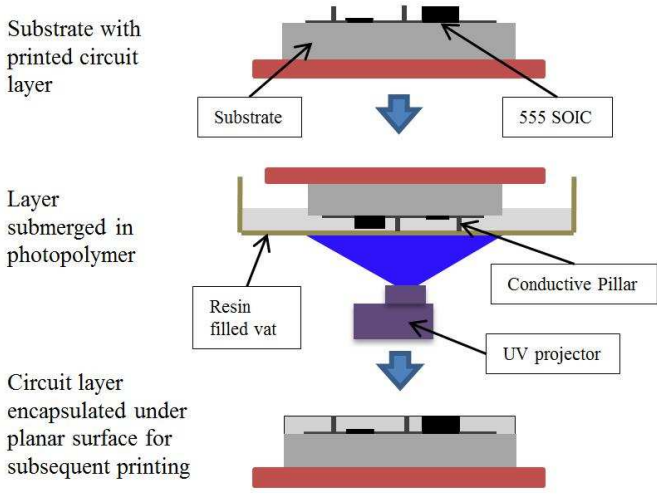

Fig. 4. Three stage embedding process using bottom up SL apparatus

III. Flip Chip Packaging Using Hybrid AM

Consumer demands for lighter, cheaper, smaller and smarter electronic products is pushing the electronics industry to utilise the smallest packaging footprint possible. In this respect, flip-chip packaging is seen as the ideal platform to satisfy these requirements. As well as packaging multiple layers of circuitry, this particular manufacturing process chain has demonstrated a low temperature flip chip packaging process by using the silver epoxy used to generate the circuit layer to produce small interconnects by the process shown in figure 5. For this particular application, Epotek EJ2189 ICA proved to produce higher resolution interconnect bumps with a lower standoff and bump diameter. This was due to its lower viscosity therefore allowing more controlled dispensing of smaller volume deposits. To determine the viability of this method for packaging, bare die with a perimeter daisy chain pattern were flip chip assembled to a 3D printed circuit.

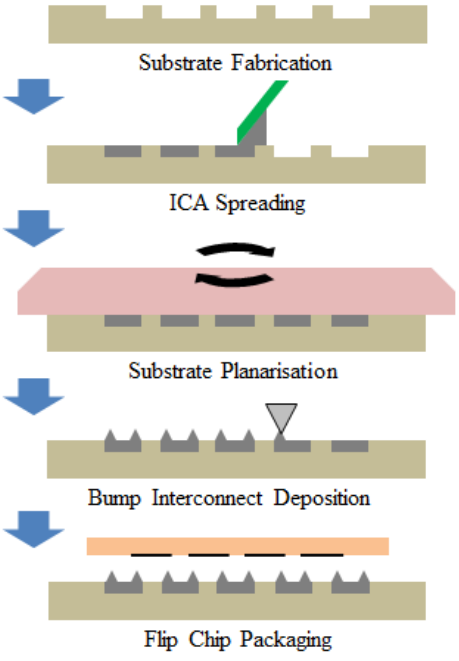

Fig. 5. Flip chip packaging method achieved through hybrid AM

The Stereolithography process has been used to create trenches which were then filled with conductive epoxy, and subsequently interconnects were deposited to bump the substrate pads. The pads had a diameter of 195µm at a pitch of 457µm.

Trench sizes were fabricated between 100µm and 200µm in depth, 200µm in width and 650µm in length, with the effect on visual and dimensional quality observed. A 200µm depth demonstrated an improved feature resolution and also enabled a larger volume of conductive material to be deposited into the features. A scalpel blade was then used to sweep conductive material across the planar surface filling the trenches in the process. Multiple passes in different directions ensured that the entire volume of the trenches in both orientations was filled. The excess epoxy deposited on the substrate surface was then removed using a lint free cloth lightly soaked in Isopropyl Alcohol. The silver filled epoxy was then thermally cured before an additional polishing process was used to planarize the layer and remove any trace of ICA from the substrate surface as displayed in figure 6.

The die footprint was 6.3mm x 6.3mm. Only pre-bumped daisy chain bare die could be sourced, therefore, die with solder bumps were used to prove the feasibility of this technique. This solder increases the standoff height by 140µm. The type of ICA, printing pressure, print gap and dispensing time were varied to optimise interconnect deposition, to generate fine interconnect bumps. Feature diameters as small as 259µm in diameter and 275µm in height were achieved printing at a pressure of 40kPa for 0.2 seconds, with a print gap of 40µm and a 200µm nozzle. Printing pressure was shown to produce a significant effect on the bump and trace dimensions. Figures 7b and c show two sets of interconnects produced at different printing pressures and demonstrate that print pressures outside the range of 30kPa to 60kPa produce either insufficient or excessive material deposits. Figure 7a presents relationships between this material, printing pressure, print gap and actuation time. The smallest diameter printed using the higher viscosity epoxy was 348µm.

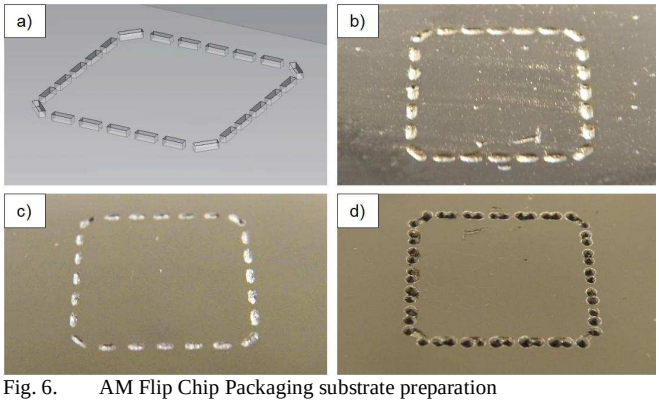

Fig. 6. AM Flip Chip Packaging substrate preparation

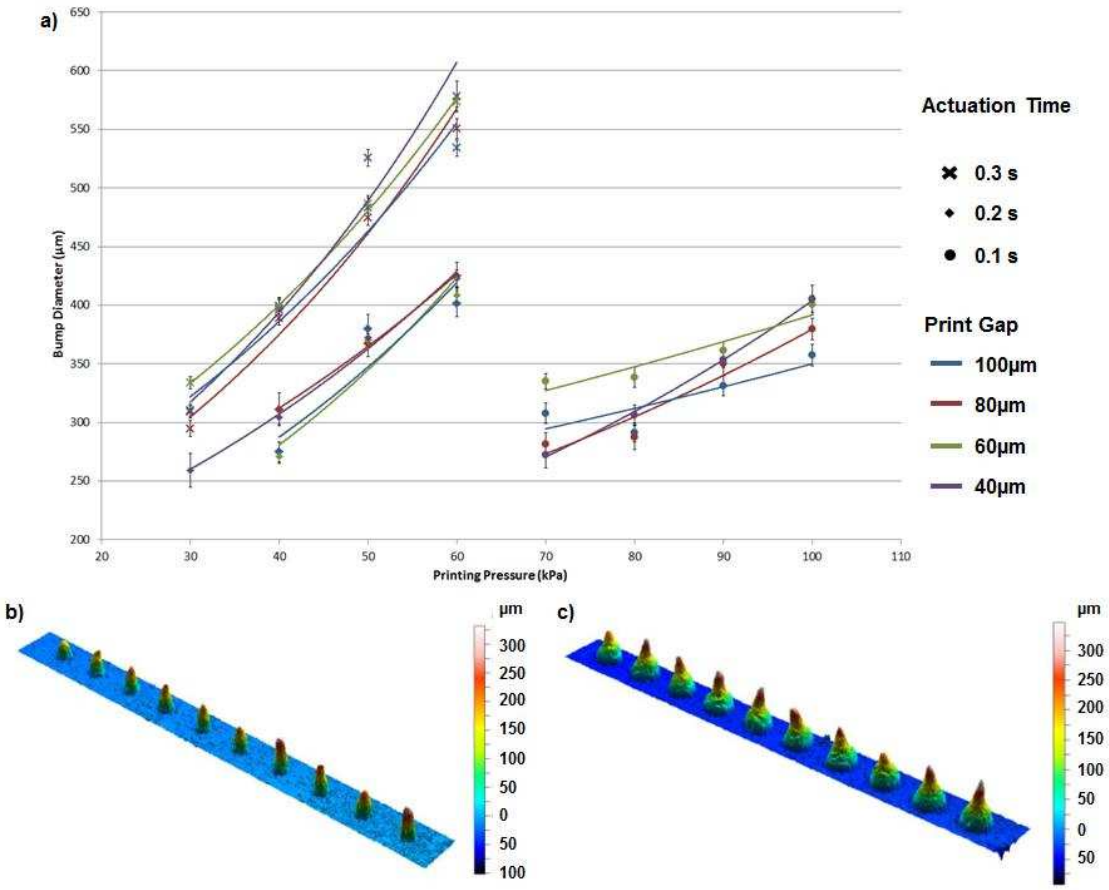

Fig. 7. Relationship between interconnect bump diameter, print gap and print actuation time has been a) graphed and profiles shown of bumps produced at pressures of b) 30kPa and c) 60kPa

Print gap appears to have differing effect on the epoxy dependent on viscosity. Interconnect diameters produced in the higher viscosity E4110-PFC ICA decrease with the print gap however, in the low viscosity EJ2189 epoxy, there was minimal correlation between bump diameter and print gap.

Optimised bump dispensing parameters were then applied to deposit interconnects on each end of the filled channels on the substrates in figure 6. A manually operated flip chip bonding machine (Finetech FINEPLACER® with Leica Wild M3Z Optical Microscope) with ±3µm alignment accuracy was used to package the daisy chain test die. The corresponding daisy chain pattern was deposited on the photopolymer surface at a pressure of 40kPa, actuation time of 0.2 seconds and print gap of 40µm through a 200µm diameter nozzle. This pattern was aligned with the centre of the bond pads, creating a full connection around the perimeter of the bare die. This circuit layer also contained a series of redistribution traces, shown in figure 8a, to allow probing of each pair of interconnections and to enable the full electrical characterisation of the circuit in series.

Before bonding, the resistance between UBM pads on the chip was measured at 0.2Ω. Following packaging with no additional bonding pressure, the resistances between adjacent epoxy test pads were measured at an average of 5.2Ω. The resistance increase is a product of both the filled epoxy channels and interconnects. Additional samples were packaged with a bonding pressure of 8g to increase contact area with the solder bumps and to compensate for any differences in ICA interconnect print heights. This resulted in the average resistance dropping to 3.2Ω between redistribution traces.

Figure 8b shows an optical microscope image with successful connections made along the perimeter edge of the chip. This figure shows consistent bump geometries and successful alignment of both dispensed features with channels and interconnects with solder bumps. Figures 8c and 8d also demonstrate errors encountered during the packaging process, including inconsistent material deposition leading to a significantly reduced bump height and misalignment during placement resulting in a shift of the chip on the substrate. Although an electrical connection was made on the misaligned edge, the resistance increased to an average of 15Ω. By flattening the solder bumps via grinding and using the same 8g bonding pressure, average contact resistance was reduced to 2.3Ω.

IV. Demonstrators

To demonstrate the capability of this recently developed digitally driven manufacturing process chain, a single layer 555 flashing timer circuit was manufactured as shown in figure 9a. This circuit incorporates 1206 SMD resistors, capacitors, LED and a Small Outline Integrated Circuit

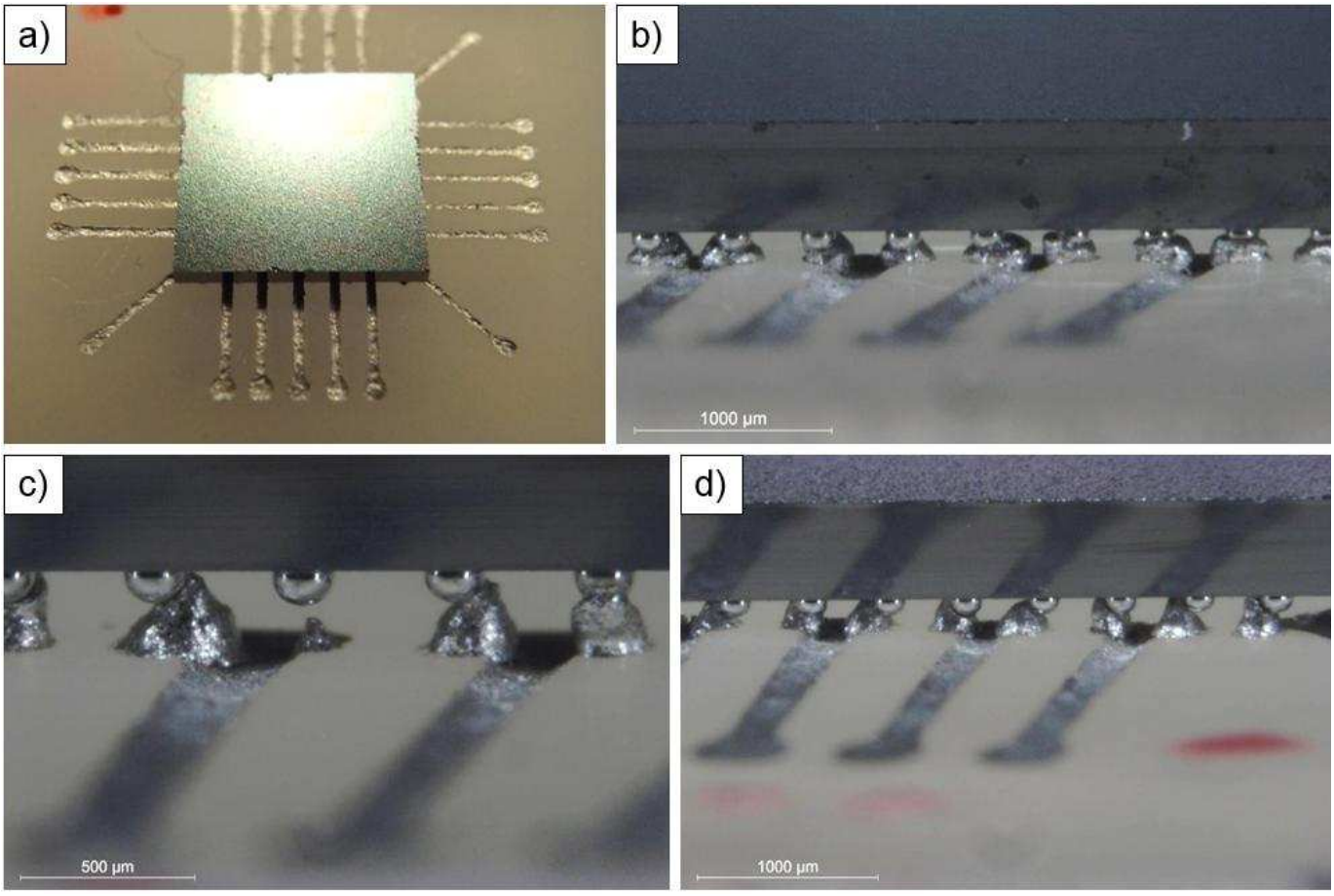

Fig. 8. a) Flip chip aligned and cured in position, b) dispensed and cured interconnects, c) inconsistent interconnect heights and d) misalignment

(SOIC) based on a rectangular photopolymer substrate. This circuit was then encapsulated using the SL process by a 2mm thick layer of photopolymer to completely embed the electronic circuit. After this was successfully fabricated, the multilayer capability was demonstrated using the same 555 configuration, but a resistor and a LED were moved to the top layer and conductive connections were made to the bottom layer via a pair of freestanding pillars built in the z-axis as shown in figure 9b. Finally, a third layer, figure 9c, was added and the electronics minimised through reducing the track widths and using smaller 0603 components. This was achieved by moving the LED to the top layer, placing a resistor and capacitor on the second layer and leaving the 555 SOIC and other discreet components on the base. A total of five z-axis connections were formed between layers, three on the base and two on the second layer. The reduction in SMD size also facilitated the reduction in embedding layer thickness from 2mm to 1.2mm and overall, the area footprint of the circuit was reduced by 70%.

Finally, the 3D capability of the process has been demonstrated through the production of the same triple layer 555 timer circuit within the pyramid structure as shown in figure 10. To allow geometrically complex demonstrators to be produced, 14mm x 14mm x 1.2mm cavities were produced layer-by-layer in which circuitry including tracks, interconnects, z-axis conductors and SMD's were then deposited. The cavity with corresponding assembled circuit layer was then filled while facing upwards. Any bubbles were left to settle out and the part re-aligned in the SL system before the top of the cavity was positioned on the base of the vat before a flood exposure from the UV projection source for90 seconds to complete the embedding process. After embedding, further thin layers of 100µm thickness were deposited to create the complex external geometry while leaving a central cavity for the next layer of electronics.

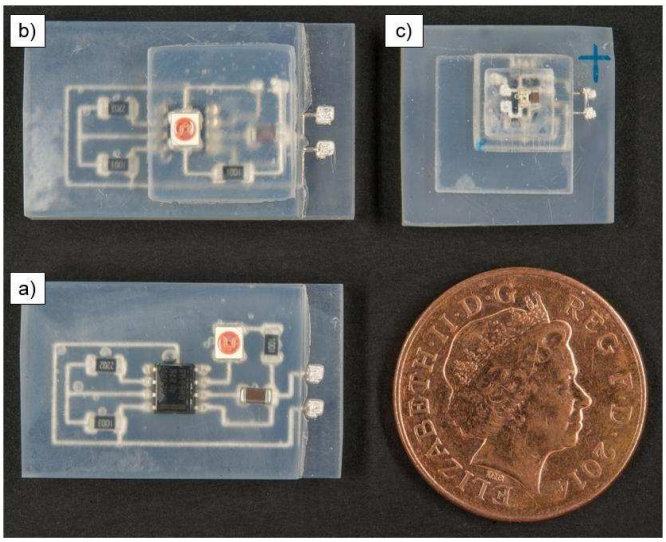

Fig. 9. Demonstrators of a) 1 layer, b) 2 layers and c) 3 miniaturised layers of embedded circuitry

V. Conclusions

This paper has presented a novel hybrid manufacturing method for the production of multilayered, embedded electronics. This method combines DLP SL and material dispensing processes with mid-process cleaning, conventional surface mount assembly and thermal curing to overcome a number of standalone AM manufacturing limitations.

A bespoke bottom up Stereolithography system was developed to fabricate 3D substrates and to embed electronics. The bottom up exposure method produces a high quality surface

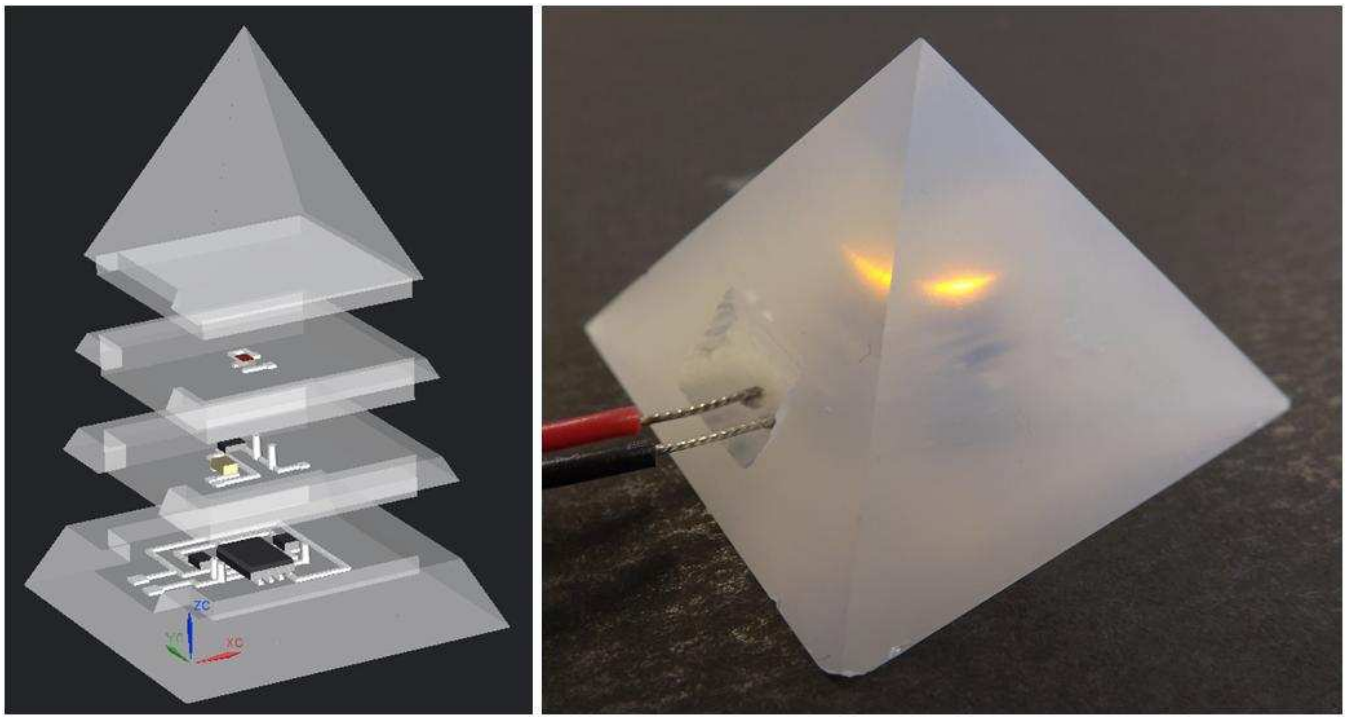
Fig. 10. a) Pyramid demonstrator design and b) fully functioning example

onto which subsequent circuitry can be deposited and enables encapsulation of thick layers. The mid processing stage allowed the two 3D printing processes to be interleaved without cross-contamination of the apparatus. The deposition of silver-based conductive materials enabled the multipurpose deposition of the circuit layer, z-axis connection and interconnects. Using a silver filled ICA enabled a low-temperature packaging process however, the low Tg of this particular photopolymer limits the applications for high operating temperature devices.

Utilising this manufacturing method, a range of demonstrators have been fabricated to prove the capability of this technology. Demonstrators with both single and multiple layers have been produced with SMD components as small as 0603 successfully integrated in the 3D printed part. The ability to produce complex packaging geometries has been shown through the development of a pyramid shaped demonstrator with embedded electronics.

Finally, this hybrid additive manufacturing approach has been applied to flip chip packaging on a photopolymer substrate, showcasing its potential for use in advanced packaging applications. To-date, interconnects as small as 259µm have been produced with a pitch of 457µm and aligned with a daisy chain test die. The resulting bumped die demonstrated successful electrical contact between adjacent traces and around the full perimeter of the 6.3mm x 6.3mm chip.

The combination of these template-less fabrication technologies shows potential as a manufacturing technology for both iterative product development and end user applications in a number of industrial fabrication scenarios including lab on chip or microfluidics, embedded sensor systems, mechatronics and electronic packaging.

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