Proceedings Paper:

Schulte-Braucks, C, Glass, S, Hofmann, E et al. (7 more authors) (2016) Process modules for GeSn nanoelectronics with high Sn-contents. In: 2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon, EUROSOI-ULIS 2016. EUROSOI-ULIS 2016, 25-27 Jan 2016, Vienna. IEEE , pp. 24-27. ISBN 9781467386098

https://doi.org/10.1109/ULIS.2016.7440043

Process Modules for GeSn Nanoelectronics with high Sn-contents

C.Schulte-Braucks, S. Glass, E. Hofmann, D. Stange, N. von den Driesch, Q.T. Zhao, D. Buca, S. Mantl
Peter-Grünberg-Institute 9 (PGI-9) and JARA-FIT
Forschungszentrum Jülich GmbH
52428 Jülich, Germany

J.M. Hartmann
University of Grenobles Alpes, F38000 and
CEA, LETI, MINATEC Campus, F-38054,
Grenoble, France

Z. Ikonic
Institute of Microwaves and Photonics, School of Electronic and Electrical Engineering
University of Leeds
LS2 9JT, Leeds, United Kingdom

***Abstract*—In this paper we present a systematic study of GeSn n-FETs. First, process modules such as high-k metal gate stacks and NiGeSn - metallic contacts for use as source/drain contacts are characterized and discussed. GeSn alloys of different Sn content allow the study of the capacitance-voltage (CV) and contact characteristics of both direct and indirect bandgap semiconductors. We then present GeSn n-FET devices we have fabricated. The device characterization includes temperature dependent IV characteristics. As important step towards GeSn for tunnel-FET $Ge_{0.87}Sn_{0.13}$ tunnel-diodes with negative differential resistance at reduced temperature are shown. The present work provides a base for further optimization of GeSn FET and novel tunnel FET devices.**

Keywords—GeSn, MOSFET, high-k/metal gate, NiGeSn

I. INTRODUCTION

GeSn alloys are group IV semiconductors that rapidly evolved within the last years. Thanks to the availability of high-Sn content and strain relaxed layers, we were recently able to prove the existence of a fundamental direct bandgap in a group IV alloy grown on Si [1]. Having direct bandgap (DBG) GeSn alloys is a definite boon for Si based photonics. However such alloys may also serve as performance booster for nanoelectronic devices. The small effective mass and reduced scattering at the center of Brillouin zone allows increased mobility of Γ- electrons and performance improvement of GeSn MOSFETs. In addition the possibility of combining direct band-to-band tunneling and the low bandgap should yield efficient band to band tunneling in tunnel field effect transistors (TFETs).

Theoretical k.p - calculations predict a significant mobility enhancement as soon as the population of Γ-valley increases. For indirect GeSn alloys the mobility is dominated by electrons occupying the L-valley until Sn contents around 9 at.% are reached. For larger Sn contents above the indirect to direct bandgap transition, the Γ-valley becomes populated and the boost in electron mobility becomes significant. The calculated Sn-dependent Γ-valley population and mobility is presented in Fig.1. The mobility of Γ–electrons itself is much larger than mobility of L-electrons, due to a much smaller effective mass and density of states of the former. In direct GeSn, with the L valley not considerable above Γ, strong intervalley Γ–L scattering limits the mobility of Γ–electrons. However when Sn-content and thus the Γ-L spacing further increase this scattering process is suppressed. As a consequence the Γ mobility, as well as the average mobility, strongly increase.

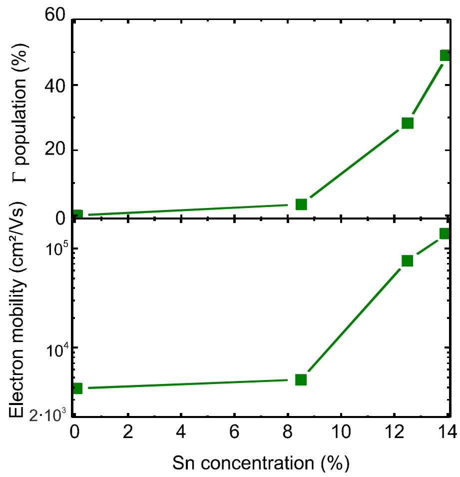

Fig. 1. Calculated Γ-valley population (top) and electron mobility vs Sn-content (bottom) as obtained by k.p-theory.

This research received funding from the EU FP7 project E2SWITCH (619509) and the BMBF project UltraLowPow (16ES0060 K).

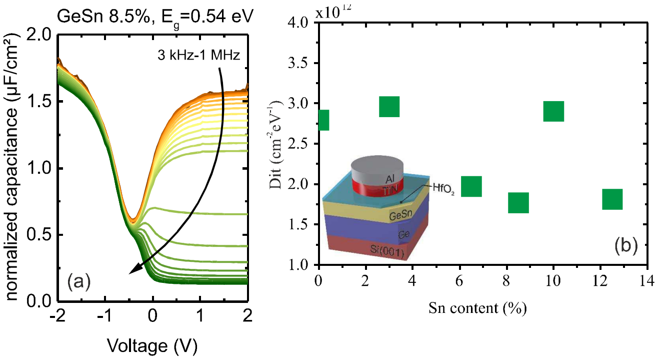

Fig. 2(a) CV-characteristics of TiN/6 nm $HfO_2/Ge_{0.915}Sn_{0.085}$ MOScap for a set of frequencies. (b) Dit at midgap for several Sn-contents extracted at low-T.

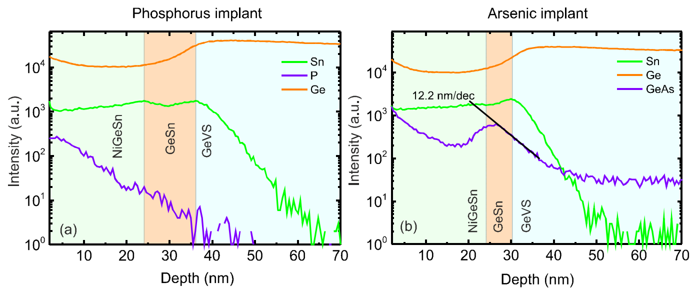

Fig. 4. SIMS-profiles of NiGeSn/GeSn contacts: For Phosphorous impantation no segregation was observed (a), whereas there is a clear peak in the Arsenic profile (b).

Preliminary works on p- and n- MOSFETs [2], [3] and even TFETs [4] based on GeSn alloys have been reported, however, with Sn-contents and strain values far below the indirect to direct transition. The low solid solubility of Sn in Ge < 1at.% and the far non-equilibrium growth results in a very limited thermal budged < 350°C for Sn-contents above 10 at.% making process integration challenging as elevated processing temperatures would result in Sn-segregation and precipitation.

In this work we discuss advances on low temperature (T) process modules for GeSn-FET devices with Sn-contents up to 13 at.% including high-k/metal gate stacks with interface trap densities in the 10^{12} $eV^{-1}cm^{-2}$-range and low resistivity NiGeSn contacts with ultra-low Schottky barrier heights. Emphases is placed on the fabrication and characterization of tunneling diodes with 13 at.% Sn as well as on first steps toward direct bandgap GeSn n-FETs.

II. Experimental

Due to the low solid solubility of Sn in Ge < 1 at.% GeSn layers with Sn-contents up to 13 at.% are grown far from equilibrium growth conditions in an industry compatible AIXTRON TRICENT RPCVD reactor [5]. All process modules were kept below 350°C in order to avoid Sn - diffusion and segregation. As a first key module MOS-capacitors (MOScaps) with high-k/ metal gate stacks on GeSn have been investigated. After surface preparation in HF-HCl wet cleaning 6 nm HfO_2 dielectric followed by 40 nm TiN metal were deposited at low temperature by atomic layer deposition (ALD) and sputter deposition, respectively. MOScaps with Sn-contents between 0 at.% (Ge-substrate) and 12.5 at.% were fabricated. In doing so standard CMOS technology such as photo lithography and reactive ion etching were used to define structures. The fabrication ended up with a lift off process including the deposition of 150 nm Al for contacts followed by forming gas annealing at 300°C. A set of Capacitance-Voltage (CV)-curves for different frequencies measured on $TiN/HfO_2/Ge_{0.915}Sn_{0.085}$ is shown in Fig.2(a). The good $GeSn/HfO_2$ interface quality is evidenced by the small frequency dependent flat-band voltage shift and the small frequency dispersion in accumulation. As a characteristic of low bandgap semiconductors, the CV-curves feature a strong minority carrier inversion response even at high frequencies > 100 kHz. As a consequence the so called weak-inversion hump hinders a reliable extraction of interface trap density (Dit) at room temperature [6]. However, at lower temperatures the minority carrier inversion response is reduced and by applying the low-T conductance method Dit values of $2x10^{12}$ $cm^{-2}eV^{-1}$ at midgap were extracted for GeSn capacitors with different Sn contents (Fig. 2(b)).

Metal-semiconductor-metal diodes based on NiGeSn/GeSn Schottky contacts were fabricated using an oxide mask. After native oxide removal, 10 nm of Ni were deposited by sputter deposition and ~ 23 nm NiGeSn was formed by rapid thermal annealing for 10 s in N_2/H_2 forming gas atmosphere. Unreacted

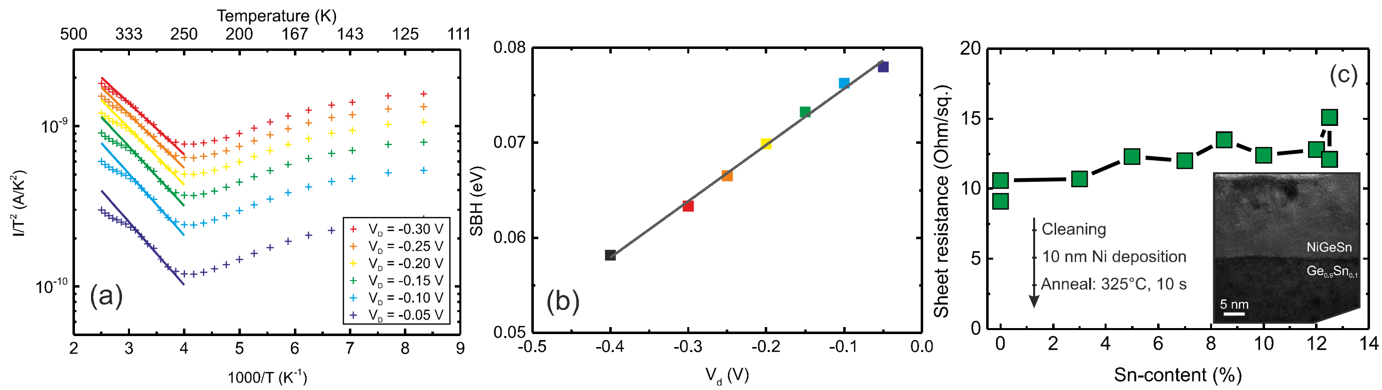

Fig. 3. Investigation of NiGeSn Schottky-contacts (a) Arrhenius plot of current characteristics. The linear region is fitted and SBH is exctracted from the slope. (b) SBH vs. applied bias from (a). The SBH for 0 V is extracted by extrapolation to 0 V. (c) Sheet resistance for NiGeSn fabricated on several GeSn substrates. The inset depicts a TEM micrograph of a NiGeSn/GeSn contact.

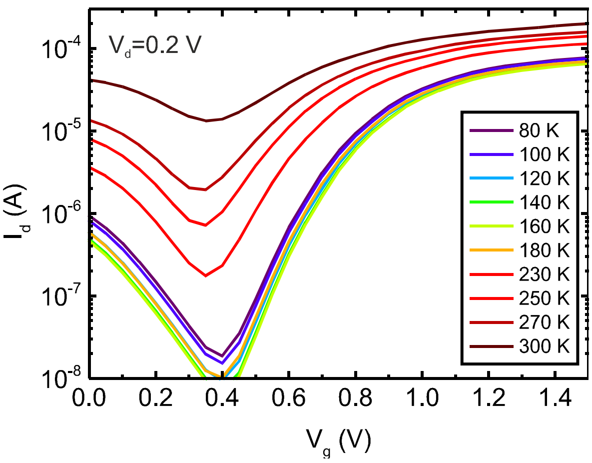

Fig. 5. Tranfer characteristics of $Ge_{0.93}Sn_{0.07}$ n-FETs at different temperatures.

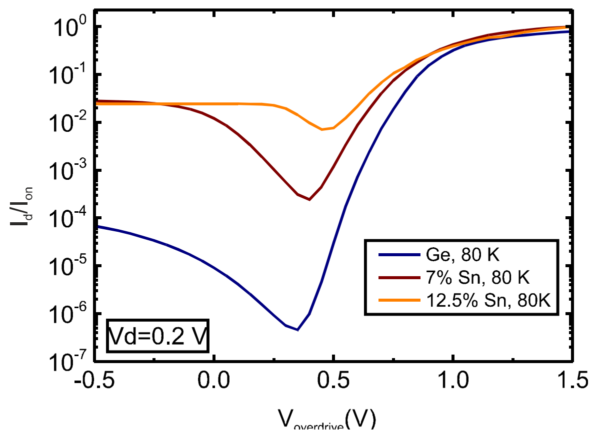

Fig. 6. I_d/I_{on} ratio of GeSn n-FETs at 80 K for several Sn-contents.

Ni was removed by sulfuric acid (96 % aq.). The lowest sheet resistance was obtained by stano-germanidation at 325°C [7]. The low-resistive NiGeSn-phase could be maintained over the complete available Sn-content range from 0 to 12.5 at. %. The sheet resistance of NiGeSn for several Sn-contents is shown in Fig.3(c). Furthermore a smooth NiGeSn/GeSn interface was obtained as shown by the cross-sectional Transmission-Electron-Microscopy (TEM) image in the inset of Fig.3(c). I-V characteristics of two back-to back connected NiGeSn/GeSn Schottky diodes were measured in a temperature range from 350 K down to 100 K. From Arrhenius plots of the current characteristics for different voltages (Fig.3(a)) the Schottky-barrier height (SBH) was extracted by fitting the linear region. In order to exclude the image force lowering by the applied voltage the SBH at 0 V was obtained by plotting the extracted SBH from Fig.3(a) against the applied bias and extrapolating to 0 V, as shown in Fig.3(b). Similar to NiGe/Ge contacts the Schottky barrier of NiGeSn on GeSn for holes is very small. A SBH of 0.08 eV has been extracted for NiGeSn/$Ge_{0.875}Sn_{0.125}$ (p-type) which makes NiGeSn an ideal contact for p-type devices. However, this implies very high Schottky barriers for electrons leading to high S/D resistances for n-type GeSn and demanding further investigation on n-type GeSn-contacts.

Dopant segregation (DS) is a well know method for SBH-tuning [8]. The dopant segregation effect on GeSn with n-type dopants is presented below. Both P and As were first implanted into GeSn test-structures at a dose of $1x10^{15}$ cm^{-2} at energies of 7 and 13 keV, respectively. Then a NiGeSn layer was formed with the above mentioned annealing parameters. Subsequently doping profiles were analyzed by means of Time of Flight Secondary-Ion-Mass-Spectrometry (ToF-SIMS). Whereas there is no peak visible in the doping profile for P, a snowplough effect has been observed for As leading to a peak in the As-concentration at the NiGeSn/GeSn interface (Fig.4). The differences in DS for As and P might be attributed to differences in solubility and diffusion.

Combining the above described process modules GeSn n-MOSFETs were fabricated with Sn contents of 0 at.%, 7 at.% and 12.5 at.% using ion implanted source/drain (S/D) contacts after forming a gate stack with TiN/HfO_2. The transfer curves of the GeSn-nFETs for a series of temperatures are shown in Fig.5. At room temperature the device shows a low I_{on}/I_{off} ratio and a reduced on current at lower temperature due to the poor n+/p junctions in the S/D regions. The limited thermal budget used in order to avoid Sn diffusion, here 350°C, was not sufficient to recrystallize the amorphized regions created by ion implantation, leading to very poor junctions with low activation and high access resistances. This is even more critical for high Sn content devices as shown in Fig.6 at 80K. Apart from the un-healed implantation damage the unintentional background doping of GeSn increases with increasing Sn-content. Furthermore the bandgap is decreased. Both factors lead to increased S/D-leakage and gate induced drain-leakage (GIDL) which is caused by band to band tunneling and increases exponentially with the reduced bandgap. This is also visible in the temperature dependence of the transfer characteristics in Fig. 5. The S/D leakage strongly decreases for temperatures below 200 K. The solution for maintaining crystalline GeSn is the use of in-situ doping and selective growth in the S/D region. The in-situ doping is discussed below in terms of tunneling diodes.

As demonstration of the potential of direct bandgap GeSn for band to band tunneling, and the advantage of in-situ doping over ion implantation, we have fabricated GeSn tunneling diodes as an important step towards advanced GeSn based

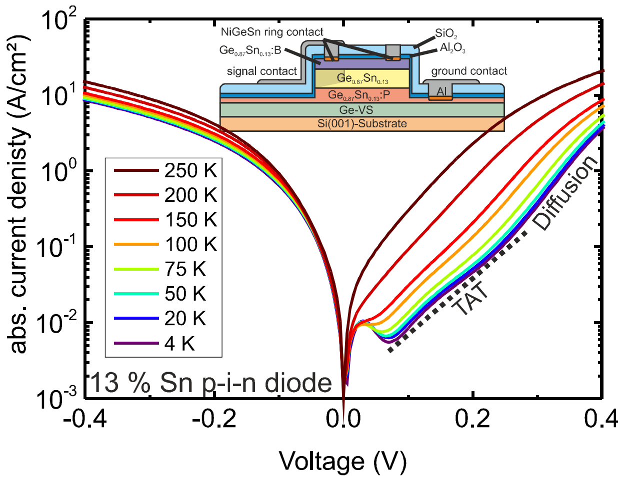

Fig. 7. Temperature dependent I-V measurements of a $Ge_{0.87}Sn_{0.13}$ p-i-n diode showing clear NDR for low-T.

TFETs. We could push the Sn-content up to 13 at.% as a follow up to previous results with a stack of 9 at.% and 11 at.% [9] enabling an even lower bandgap and higher directness of the GeSn. As a proof of band-to-band tunneling negative differential resistance (NDR) is observed at low-T (Fig.7), demonstrating a high doping level of both p and n-type dopants, which is essential for MOSFETs and TFETs. However, due to enhanced diffusion and trap assisted tunneling (TAT) in this low-bandgap semiconductor the NDR vanishes for temperatures above 100 K. In forward bias > 0.1 V two distinct regions separated by a kink in the slope of the I-V curve are visible. Whereas the medium part of the curve 0.1 V < V_d < 0.3 V can be attributed to TAT, diffusion current is dominating for strong forward bias > 0.3 V. We expect further improvements in the peak to valley current ratio and a move towards room temperature NDR with optimized doping profiles.

III. Conclusion

We presented process module developments for GeSn-FETdevices including high-k metal gate stacks, NiGeSn contacts as well as GeSn-nFETs with Sn-contents >10 at.%. MOScaps with HfO_2 on GeSn showed good C-V characteristics with Dit levels of 10^{12} $eV^{-1}cm^{-2}$. Uniform NiGeSn contacts on p-GeSn indicated very small Schottky barrier heights, while the Schottky contacts on n-GeSn can be optimized by As dopant segregation. Junctions made by ion implantation face challenges due to the metastability of GeSn, which can be solved by in-situ doping as illustrated by GeSn-tunnel diodes with 13 at.% Sn which show characteristic negative differential resistance at low-T.

References

[1] S. Wirths, R. Geiger, N. von den Driesch, G. Mussler, T. Stoica, S. Mantl, Z. Ikonic, M. Luysberg, S. Chuissi, J. M. Hartmann, H. Sigg, J. Faist, D. Buca and G. Grützmacher, Lasing in direct-bandgap GeSn alloy grown on Si, Nature Photonics, 9(2), pp. 88–92, 2015.

[2] S. Gupta, B. Vincent, B. Yang, D. Lin, F. Gencarelli, J.-Y.J. Lin, R. Chen, O. Richard, H. Bender, B. Magyari-Köpe, M. Caymax, J. Dekoster, Y. Nishi, and K.C. Saraswat, Towards high-mobility GeSn channel nMOSFETs: Improved surface passivation using novel ozone oxidation method, Electron Devices Meeting (IEDM), 2012 IEEE International, pp. 16.2.1–16.2.4, 2012.

[3] G. Han, S. Su, C. Zhan, Q. Zhou, Y. Yang, L. Wang, P. Guo, W. Wei, C.P. Wong, Z. X. Shen, B. Cheng, and Y.-C. Yeo, High-mobility Germanium-Tin (GeSn) p-channel MOSFET featureing metallic source/drain and sub-370°C process modules, Electron Devices Meeting (IEDM), 2011 IEEE International, pp. 402–404, 2011.

[4] Y. Yang, S. Su, P. Guo, W. Wang, Y. Gong, L. Wang, K. L. Low, G. Zhang, C. Xue, B. Cheng, G. Han, and Y.-C. Yeo, Towards direct band-to-band tunneling in p-channel tunneling field effect transistor (TFET): Technology enablement by Gemanium-Tin (GeSn), Electron Devices Meeting (IEDM), 2012 IEEE International, pp. 16.3.1–16.3.4, 2012.

[5] N. von den Driesch, D. Stange, S. Wirths, G. Mussler, B. Holländer, Z. Ikonic, J. M. Hartmann, T. Stoica, S. Mantl, D. Grützmacher, and D. Buca, Direct bandgap group IV epitacy on Si for laser application, Chem. Mater., 27(13), pp. 4693–4702, 2015

[6] K. Martens, C. O. Chui, G. Brammertz, B. de Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, M. E. Maes, and G. Groeseneken, On the correct extration of interface trap density of MOS devices with high-mobility semiconductor substsrates, IEEE Transactions on Electron Devices, vol 55, 547, 2008.

[7] S. Wirths, R. Troitsch, G. Mussler, J.-M Hartmann, P. Zaumseil, T. Schroeder, S. Mantl, and D. Buca, Ternary and quaternary Ni(Si)Ge(Sn) contact formation for highly strained Ge p- and n-MOSFETs, Semicond. Sci. Technol., 30(5), p. 055003, 2015.

[8] M. Mueller, Q. T. Zhao, C. Urban, C. Sandow, D. Buca, S. Lenk, S. Estévez, and S. Mantl, Schottky-barrier height tuning of NiGe/n-Ge contacts using As and P segregation, Mater. Sci. Eng. B, vol. 154–155, pp. 168–171, 2008

[9] C. Schulte-Braucks, D. Stange, N. von den Driesch, S. Blaeser, Z. Ikonic, J. M. Hartmann, S. Mantl, and D. Buca., Negative differential resistance in direct bandgap GeSn p-i-n structures, Appl. Phys. Lett.,107(4), p. 042101, 2015