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Low temperature deposition of high-k/ metal gate stacks on high-Sn content (Si)GeSn-alloys

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ABSTRACT

(Si)GeSn is an emerging, group IV alloy system, offering new exciting properties, with great potential for low power electronics due to the fundamental direct bandgap and prospects as high mobility material. In this article we present a systematic study of HfO_2/TaN high-k/metal gate stacks on (Si)GeSn ternary alloys and low temperature processes for large scale integration of Sn based alloys. Our investigations indicate that SiGeSn ternaries show enhanced thermal stability compared to GeSn binaries, allowing the use of the existing Si technology. Despite the multi-elemental interface and large Sn content of up to 14 at.%, the HfO_2/(Si)GeSn capacitors show small frequency dispersion and stretch-out. The good interface passivation is also supported by a low leakage current of $2x10^{-8}$ A/cm^2 at -1 V and a high breakdown field of ~8 MV/cm. For large Sn content SiGeSn/GeSn direct bandgap heterostructures process temperatures below 350°C are required for integration. We developed an atomic vapor deposition process for TaN metal gate on HfO_2 high-k dielectric and validated it by resistivity as well as temperature and frequency dependent capacitance-voltage measurements of capacitors on SiGeSn and GeSn. The densities of interface traps are deduced to be in the low 10^{12} cm^{-2}eV^{-1} range and do not depend on the Sn-concentration. The new processes developed here are compatible with (Si)GeSn integration in large scale applications.

INTRODUCTION

Sn-based alloys, GeSn and SiGeSn, are emerging group IV semiconductors with applications in Si-photonics[1,2], Complementary Metal Oxide Semiconductor (CMOS) nano-electronics[3] or solar cells[4]. The great application potential arises from the novel latitude of tuning group IV material properties in terms of bandgap with direct/indirect transitions[5,6], high/low effective masses[7], and mobility. Here, we focus on Sn based alloys for electronics, primarily motivated by theoretical predictions of reduced effective masses of electrons and holes[7,8], placing GeSn on the roadmap of potential high mobility channel materials for future low power CMOS devices[9]. Even though Sn based semiconductor electronics is still at the very beginning, MOS-Field Effect Transistors (MOSFETs)[10,11] and Tunneling FETs (TFETs)[12,13] have been fabricated and improvements of both, electron and hole mobilities as compared to Ge based devices have been achieved. However, so far mostly binary GeSn layers with low Sn contents under high compressive strain have been used, where the advantages over Ge are limited. Myriad of advantages are expected at Sn atomic concentration over 10%, where the bandgap becomes direct and the contribution of electrons from the Γ - valley becomes significant. The direct bandgap was recently experimentally proven by laser action in $Ge_{0.88}Sn_{0.12}$ waveguides[14]. By allowing direct band-to-band-tunneling it can serve as a booster for the tunneling current in TFETs as recently demonstrated by the observation of characteristic negative differential resistance in p-i-n $Ge_{0.89}Sn_{0.11}$ tunneling diodes[15]. A major challenge of high Sn content GeSn technology is the limited thermal processing budget[16], as a consequence of the low solid solubility of Sn in Ge (less than 1 at.%). It has been predicted that incorporation of Si in GeSn would improve the thermal

stability due to an increased mixing entropy in the ternary, as compared to a corresponding binary with the same Sn concentration[17].

SiGeSn ternaries are another class of group IV semiconductors, which complement the properties of GeSn binaries. Due to their larger and mostly indirect band gap, SiGeSn ternaries have been considered solely as cladding layers for GeSn lasers[18,19], drain material for TFETs[13,20] or as buffers for solar cells[4]. With Si, Sn and strain as tunable parameters, the bandgap, band offsets and lattice parameters can be widely varied, enabling novel heterostructures and applications. We expect substantial advantages from SiGeSn alloys in terms of process technology and device applications. This is substantiated by band structure calculations using 8x8 k.p method[21], revealing a large tunability of SiGeSn. Fig. 1a shows the evolution of the bandgap for cubic SiGeSn alloys for fixed Sn (Si) content of 4% and variable Si (Sn) content. Accordingly, alloying with Si shifts both Γ and L valleys upwards, increasing the bandgap, while the incorporation of Sn reduces it, and for certain (Si,Sn) compositions the alloy becomes a direct bandgap semiconductor[22].

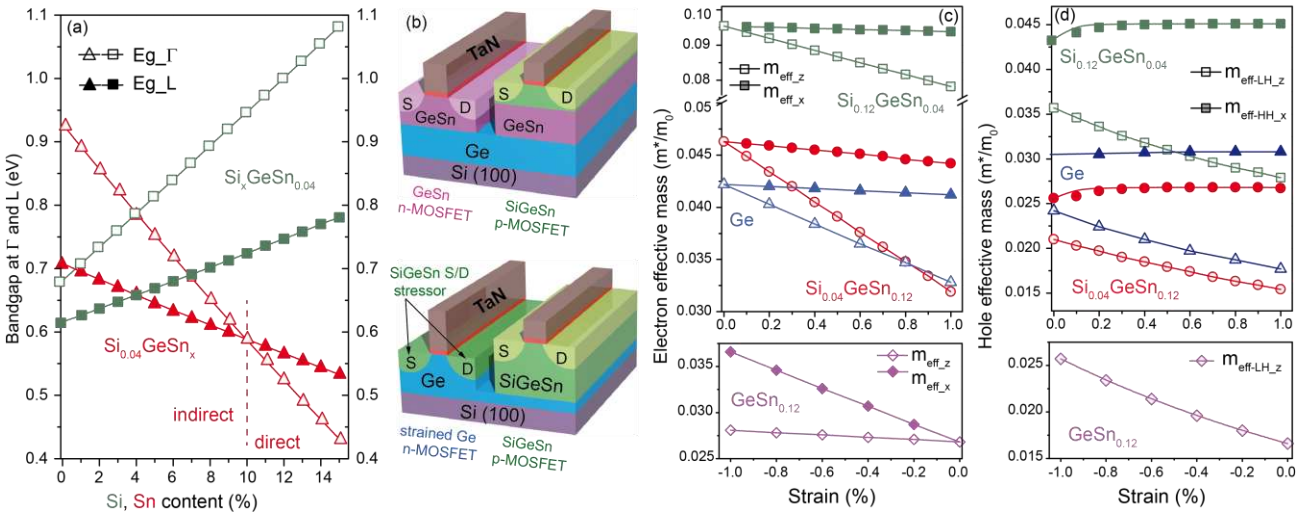

Figure 1: Bandgap at Γ and L-valley (a) for variable Si (Sn) content from 0-15% and fixed Sn (Si) content of 4 %, green (red). (b) Possible integration scheme for GeSn or Ge n-type with SiGeSn p-type MOSFET devices on the same chip. (c,d) Electron and hole effective masses vs. biaxial

tensile strain for several (Si)GeSn alloys (upper panels) and compressive strain for GeSn alloys (lower panels) demonstrating the usefulness of GeSn and SiGeSn for n- and p-type devices respectively.

High quality epitaxial growth of SiGeSn layers is performed on Ge (virtual) substrates (grown on Si(001)) or in the case of heterostructures on GeSn buffers, resulting in a tetragonal distortion of the SiGeSn lattice. The strain in SiGeSn changes from tensile to compressive, depending on the substrate and Si/Sn ratio[23]: Epitaxial $Si_{0.12}GeSn_{0.04}$ is almost strain free (ε= - 0.09 %) on Ge or highly tensile strained (ε = 1.75%) on cubic $Ge_{0.88}Sn_{0.12}$ alloy. In the higher Sn content alloy $Si_{0.04}GeSn_{0.12}$ the strain changes from large compressive ε = - 1.64% on Ge to slightly tensile ε = 0.17% on $Ge_{0.88}Sn_{0.12}$. Lattice strain influences the electronic band structure appreciably and may lead even to indirect to direct bandgap transitions[8]. $Si_{0.04}GeSn_{0.12}$ used in this work, becomes direct at a strain level of ~ 0.07%. Lattice mismatch induced strain can be used to stress Ge or GeSn channels via source/drain GeSn stressors[24,25] as indicated in Fig.1b. The high Sn content GeSn binaries, in practice mostly under compressive strain, show the lowest electron effective mass of all Ge based alloys, including tensile strained Ge (Fig 1c), the SiGeSn ternaries may exhibit lower hole effective masses as compared to Ge (Fig 1d). Thus, a practical integration scheme for drift-diffusion based MOSFETs includes GeSn for n-FETs and SiGeSn for p-FETs, as illustrated in Fig.1b. Epitaxial growth of this kind of heterostructures has been reported in the literature [13,26].

In the following we present a systematic study of (Si)GeSn MOS capacitors (MOScaps) as a key process module for (Si)GeSn devices. The surface pre-high-k cleaning and the formed high-k/(Si)GeSn interface are characterized in detail, for a large variety of GeSn binaries and SiGeSn ternaries, ranging from indirect to direct semiconductors, via physical and electrical

measurements. The novelties here are the first characterization of group IV ternaries based capacitors and the proof of their enhanced thermal stability, compared to that of binaries. In the second part we present the development of a low temperature atomic vapor deposition (AVD) metal gate process allowing to cope with the limited thermal budget of very high-Sn content direct bandgap GeSn alloys. As a major result, the complete gate stack deposition process in 300 mm wafer industrial reactors is developed and validated electrically capacitance-voltage (CV) measurements.

EXPERIMENTAL

The pseudomorphic and partially strain relaxed (Si)GeSn binary and ternary epilayers with Sn-contents from 3% to 14% and Si contents between 0% and 10% have been grown by reduced pressure chemical vapor deposition (RP-CVD) on 200 mm Ge-buffered Si(001) wafers e.g. Ge-virtual substrates (Ge-VS). The precursor gases, Si_2H_6, Ge_2H_6 and $SnCl_4$ were introduced simultaneously in the reactor via a dedicated showerhead that guaranteed a high uniformity over the 200 mm wafer. Rutherford-Backscattering-Spectrometry (RBS) was used to determine the thickness and stoichiometry of the epitaxial (Si)GeSn layers and X-ray diffraction to extract the residual compressive lattice strain. The high crystalline quality has been proven by Transmission Electron Microscopy (TEM) and ion channeling. Details on growth, physical and optical characterization of (Si)GeSn alloys can be found in Ref. [27,28].

Cleaning of (Si)GeSn prior high-k deposition

Surface preparation prior to dielectric deposition plays a crucial role in controlling the high-k/(Si)GeSn interface quality, ultimately affecting the electrostatic performance of FET-devices. The high-k/GeO_2/Ge interface, which is very different from the stable and low defect density SiO_2/Si interface, suffers from both chemical (solubility in water) and thermal instability

(formation of GeO_x sub-oxides). Great efforts have been made to achieve low densities of interface traps (D_{it}) on Ge[29–32]. (Si)GeSn alloys hold similar constraints regarding the control of the interface with high-k gate dielectrics, which includes optimization of the wet cleaning procedure prior to pre- high-k deposition[33]. Standard CMOS cleaning solutions, such as H_2O_2:H_2SO_4:H_2O (CARO), NH_4OH:H_2O_2:H_2O (SC1) or HCl:H_2O_2:H_2O (SC2), use H_2O_2 as oxidant which strongly chemically etches GeSn alloys, resulting in material loss and surface roughening. As a consequence, a modified pre-high-k deposition cleaning procedure has been used: after a pre-clean in an ultrasonic acetone bath, residual particles and organic contamination were removed in a 60°C hot ultrasonic bath of dimethyl sulfoxide (DMSO):cyclopentanone (10:3) followed by exposure to an inductively coupled oxygen plasma. Potential residual metallic contamination and native oxides were removed in HF:HCl (1% aq.) without a water rinse afterwards (called "HF:HCl-last"). The formation of an ultrathin SiO_2 or GeO_2 layer was found to be beneficial for the improvement of interface electrical properties of Si and Ge, respectively[31]. However, the formation of SnO_2 can be detrimental, as SnO_2 is known to exhibit metallic behavior[34]. Consequently, a chemically controlled surface prior to high-k deposition is of critical importance. X-ray photoelectron spectroscopy (XPS) has been used to analyze the surface (and near surface region) chemical composition before and after the cleaning procedure.

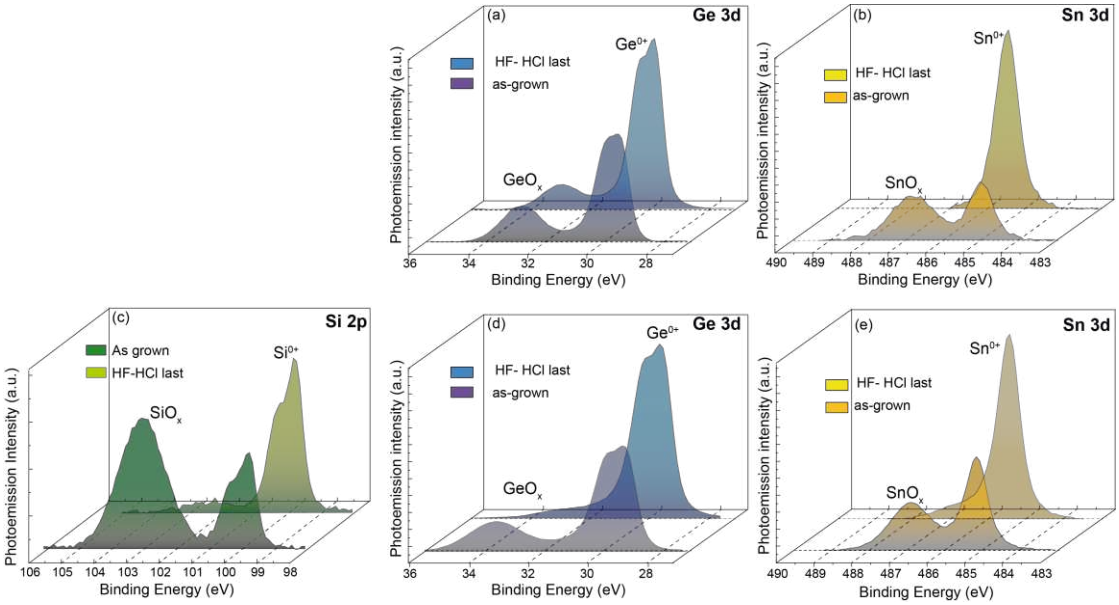

Figure 2: XPS-analysis of (a,b) $Ge_{0.875}Sn_{0.125}$ and (c-e) $Si_{0.81}Ge_{0.915}Sn_{0.09}$-surface. "HF:HCl last" cleaning significantly reduces the SiO_x, GeO_x and SnO_x peak intensities. The transfer to the XPS-tool occurred ex-situ.

XPS analysis of the core level spectra of the SiGeSn surface was performed in a PHI5000 VersaProbe II tool with monochromatic Al K_α X-rays at 1486.7 eV. As the sample transfer to the XPS-tool occurred *ex-situ*, the C1s peak at 285.0 eV served as a reference. The information of interest here is the oxidation state of the Si, Ge and Sn atoms. Fig.2 shows the Si2p, Ge3d and Sn3d peaks of $Ge_{0.875}Sn_{0.125}$ and $Si_{0.81}Ge_{0.915}Sn_{0.09}$ prior to and after cleaning. Despite the *ex-situ* sample transfer into the XPS chamber, the SiO_x and GeO_x signals were reduced significantly and SnO_x was completely removed from the (Si)GeSn-surface.

The cleaned (Si)GeSn substrates were loaded into the 300 mm ALD reactor and 5 nm HfO_2 was deposited at 300°C. The Hf precursor, liquid Tetrakis EthylMethylAmino Hafnium, (TEMAH), Hf $[N(CH_3)(C_2H_5)]_4$, was injected in pulses followed by ozone (O_3) pulses. In order to allow direct comparison with our previous study on strained Ge and GeSn MOScap results, we used the same HfO_2 deposition sequence and parameters as in Ref.[8] In the first approach the gate

stack was finalized with Pt deposition as top metal contact. In the second part of the paper, we present the optimization of low-temperature TaN AVD process which allows *in-situ* deposition of the whole gate stack (vacuum transfer between the 300 mm ALD (HfO_2) and AVD (TaN) reactors). For samples with TaN 150 nm thick Al was sputter-deposited and a lift-off process was used to fabricate electrical contact pads. Subsequently, the Al pads acted as hard masks for the metal gate etch in a SF_6:Cl_2:Ar reactive ion etching plasma. The fabrication ended with a 300°C forming gas annealing (N_2:H_2/4:1) for 10 min. The complete description of the MOS capacitors fabrication including the precursors and their injection mechanism used for the growth of the (Si)GeSn, HfO_2 and TaN, is schematically illustrated in Fig.3a-c. The cross-sectional TEM-images in Figs.3d,e show the high crystalline quality of the Ge-VS/GeSn/HfO_2/TaN heterostructure after the complete gate stack process, including the forming gas annealing. The smooth HfO_2/GeSn interface is clearly visible (Fig. 3e).

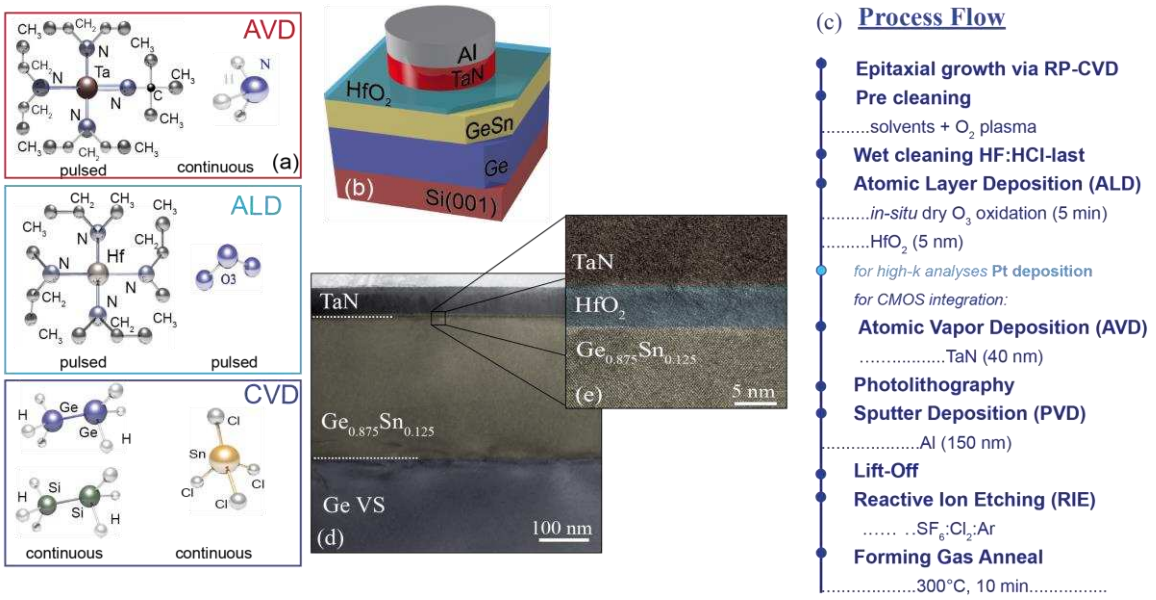

Figure 3: (a) The precursors used for layer deposition and their injection mechanism. (b) Schematic layer stack and (c) fabrication process flow. (d,e) TEM-micrograph of a

TaN/HfO_2/$Ge_{0.875}Sn_{0.125}$ stack showing the excellent crystalline quality of the GeSn layer and a smooth high-k/GeSn interface.

Electrical Characterization

The MOScap fabrication process has been applied for (Si)GeSn alloys with a broad range of Si/Sn ratios corresponding to a bandgap ranging from 0.65 eV (Ge-VS is under slight tensile strain of 0.16%) to 0.45 eV (for $Ge_{0.875}Sn_{0.125}$), as calculated by the 8-band k·p method. The current voltage (I-V) characteristics show low leakage currents of $2x10^{-8}$ A/cm^2 at -1 V and a high breakdown field of ~8 MV/cm, indicating good mesa passivation with negligible diffusion of Sn into the high-k layer. The electrical quality of the HfO_2/(Si)GeSn interface was investigated by temperature dependent capacitance - voltage (C-V) measurements. The frequency dependent C-V characteristics at 300 K of $HfO_2/Si_{0.05}Ge_{0.9}Sn_{0.05}$ and $HfO_2/Si_{0.045}Ge_{0.845}Sn_{0.11}$ MOScaps are shown as examples in Fig.4 a,b. The capacitors feature a very low frequency dispersion in accumulation and a small frequency dependent flat-band voltage shift suggesting a good interface quality. The small bandgap of the $Si_{0.045}Ge_{0.845}Sn_{0.11}$ layer translates into C-V characteristics similar to that of state-of-the-art III-V MOS-structures[35].

The variation of the alloys bandgap induces a characteristic carrier response in the C-V curves: lower bandgap semiconductors show very strong minority inversion response even at relatively high frequencies, featuring a significant so-called “weak inversion hump”. The hump stems from an enhanced interaction of mid-gap traps with the conduction and the valence bands, promoted by the low-bandgap[8,36]. In this case the weak inversion hump does not stem from a high density of interface trap states, known as the D_{it} - hump, as in larger bandgap materials such as Si. As a consequence, these effects exclude the use of the conduction method for a reliable extraction of D_{it} at room temperature, which would lead to a misinterpretation of the weak inversion as the

D_{it} contribution. Low temperature C-V measurements reduce the minority carrier response at the expense of a reduced region in the bandgap where the trap positions are sampled[8,36]. Fig.4c shows the temperature dependence of C-V characteristics between 80 K and 300 K recorded at 1 kHz for the SiGeSn MOScap of Fig.4a. The effect of temperature on the response of minority carriers is clearly evidenced: below 170 K the weak inversion hump is completely suppressed, allowing the use of the conductance method. The values of D_{it} at mid-gap, extracted for a set of GeSn binaries and SiGeSn ternary MOScaps structures with both Si and Sn-contents ranging from 0% to 14%, are plotted in Fig.4d. The D_{it} is around $2x10^{12}$ $cm^{-2}eV^{-1}$ and appears to be almost independent of the Sn-content in the investigated region.

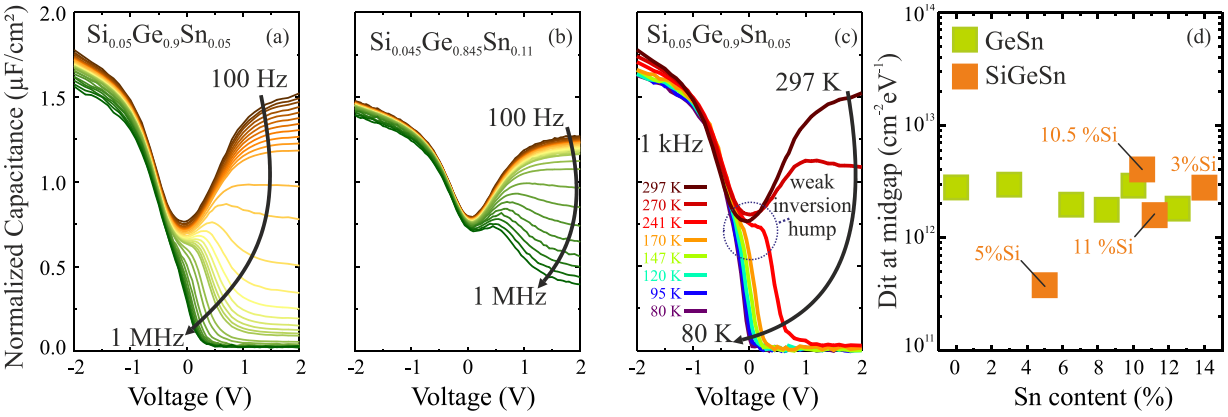

Figure 4: (a,b) C-V characteristics of 5 nm HfO_2/SiGeSn MOScaps with different Si/Sn ratios. The higher Sn-content in (b) results in a lower bandgap and an enhanced minority carrier response. (c) Temperature dependent measurements at 1 kHz. (d) Density of interface states at mid-gap for several GeSn and SiGeSn samples.

Thermal stability of GeSn and SiGeSn with large Sn contents

A commercially available industry 300 mm ALD - AVD deposition cluster enables *in-situ* wafer transfer between the reactors, highly desirable for process integration and reliability. SiGeSn and GeSn MOScaps were fabricated using 300 mm ALD - AVD deposition processes as used for Si and Ge MOSFETs. A typical Si-technology AVD metal gate process requires a deposition temperature of ≥ 450°C[37], which is much above the 350°C growth temperature used for direct bandgap (Si)GeSn alloys. However, well behaving C-V characteristics were measured for $Si_{0.1}Ge_{0.81}Sn_{0.09}$ with a stack of TaN/HfO_2 deposited at 450°C (Fig. 5a). The CV-characteristics are comparable to those of the Pt metal contacts deposited at room temperature. This is due to the higher thermal stability of the channel/gate stack compared to the $Ge_{0.9}Sn_{0.1}$ binary, as confirmed experimentally by time-of-flight secondary ion mass spectroscopy (ToF-SIMS) measurements, Fig.5b,c. In contrast, the SIMS spectra of MOScaps fabricated on $Ge_{0.9}Sn_{0.1}$ with nearly the same Sn content as for the $Si_{0.1}Ge_{0.81}Sn_{0.09}$, show strong Sn diffusion both into the high-k and into the Ge-VS when using the same metal gate process at 450°C (bright green curve in Fig.5c). Sn diffusion may lead to metallic β-Sn precipitates, degrading the gate-stack and leading to a strong increase of the leakage current[16,38]. However when reducing the metal gate deposition temperature to 350°C Sn-diffusion in $Ge_{0.9}Sn_{0.1}$ is significantly suppressed (dark-green curve in Fig.5c). Therefore, the processing of direct bandgap GeSn semiconductors requires a reduction of the AVD temperature.

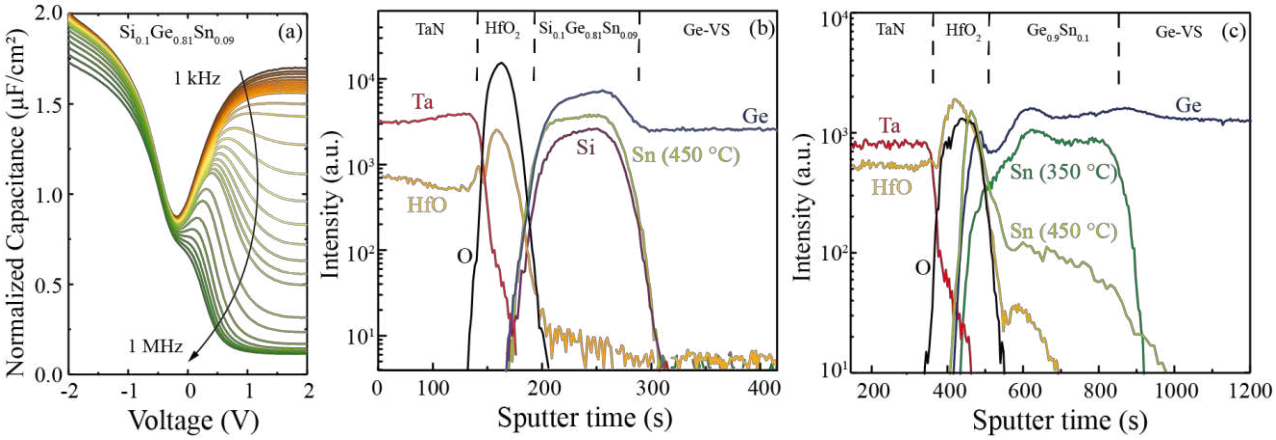

Figure 5: (a) CV-characteristics of MOScap fabricated with 450°C AVD TaN on $Si_{0.1}Ge_{0.81}Sn_{0.09}$. (b,c) ToF-SIMS analysis of MOScaps with AVD-TaN deposited on HfO_2/ $Si_{0.1}Ge_{0.81}Sn_{0.09}$ and on $HfO_2/Ge_{0.9}Sn_{0.1}$. No significant Sn-diffusion is observed for 450°C TaN deposition on SiGeSn alloys, demonstrating an enhanced thermal stability of SiGeSn alloys compared to that of binary GeSn. For GeSn the AVD deposition temperature has to be reduced to 350°C. The high HfO intensity in the TaN-layer is caused by mass interferences between HfO and TaN.

In-situ low temperature TaN deposition in an ALD/AVD cluster tool

One of the most important characteristics of the metal gate is its sheet resistance to ensure fast switching and low losses, especially for low power devices. Lowering the deposition temperature to 350°C requires process optimization in order to avoid a significant increase of the TaN resistivity for reduced deposition temperatures, as indicated by Van der Pauw measurements in Fig.6a.

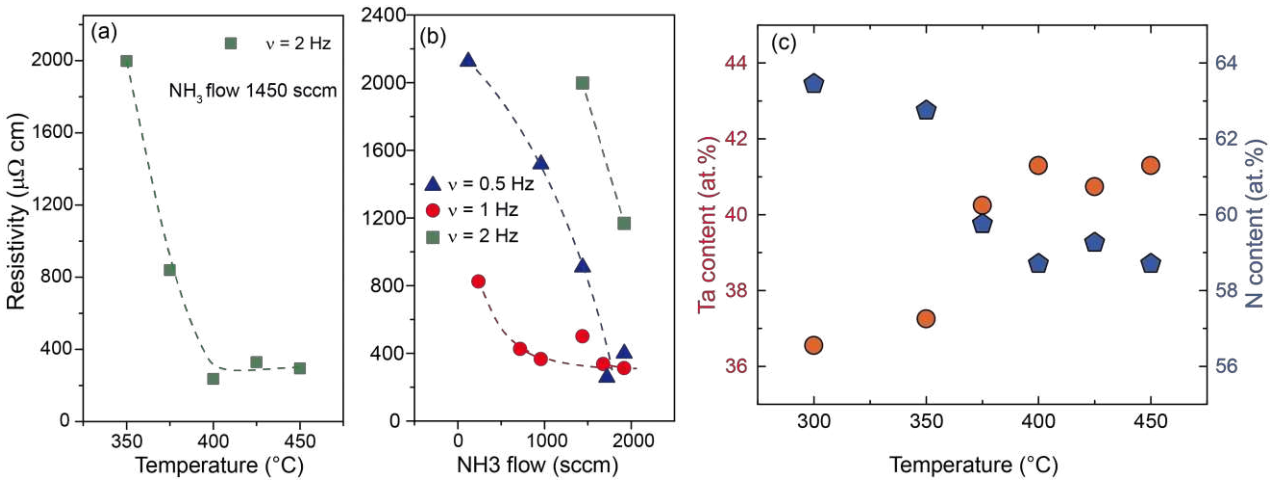

Figure 6: Resistivity of AVD deposited TaN as a function of (a) the deposition temperature and (b) the NH_3 flow as well as precursor pulse frequency at 350°C. (c) Deposition temperature dependence of TaN stoichiometry. Growth temperature reduction leads to N-rich TaN phase formation, with increased resistivity.

During the AVD process the Ta precursor, Tris(diethylamido)(Tert-butylimino)Tantalum (TBTDET), $[((C_2H_5)_2N)_3(C_4H_9N)Ta]$, is injected in pulses in reactor and the reduction agent ammonia, NH_3, is delivered continuously. At temperatures below 600°C the nitrogen in TaN is supplied in a ligand exchange reaction of both precursors[39]. Solely a reduction of the process temperature results in an incomplete reaction, leading to stoichiometry changes and contamination of the film with carbon rich by-products [40]. ALD or AVD grown TaN films typically consist of a mixture of different phases (TaN, Ta_2N, Ta_5N_6, Ta_3N_5, Ta_2O_5) and their relative fractions determine the total resistivity.[41] Generally, Ta rich phases (Ta_2N, TaN) are metallic, while the N-rich phases such as Ta_5N_6 have higher resistance or insulating /semiconducting properties (Ta_3N_5)[42,43]. The Ta/N-ratio was determined on TaN-films directly grown on Si substrates at various temperatures using RBS in channeling mode, in order to reduce the influence of the Si-substrate. The Ta/N ratio of 0.70 at 450°C decreases to only 0.57 for 300°C (see Fig.6c), suggesting

a predominance of the insulating Ta_3N_5 phase, which increases the resistivity for low deposition temperatures.

Optimization of the AVD process parameters was performed by tuning the Ta precursor injection frequency and the NH_3 flow, as both affect the chemical reactions. The resistivity of TaN films deposited at 350°C is plotted in Fig.6b as a function of the NH_3 flow for different injection frequencies, ν, at a constant injector opening time of 10 ms. The presence of NH_3 is known to be beneficial for TBTDET deposited TaN in order to form a dense film and to reduce the carbon content by formation of volatile by-products such as short-chain amines[44–46]. The reduced reactivity at lower temperatures is compensated by an increased NH_3 flow and leads to a significant decrease of the resistivity. With optimized deposition parameters the resistivity of TaN could be reduced by an order of magnitude, from 2000 μΩ·cm down to 200 μΩ·cm.

The optimized AVD TaN metal gate process has been successfully applied to a series of GeSn substrates with 5.5 % Sn, 8.5 % Sn and 12.5 % Sn, as well as to Ge-VS for comparison. The C-V characteristics for frequencies from 10 kHz to 1 MHz are plotted in Fig.7. For the AVD metal gate the HfO_2-thickness was kept at 5 nm and the leakage current remained at ~$2x10^{-8}$ A/cm^2 at -1 V indicating no significant Sn-diffusion into the high-k/metal gate stack. A continuous increase of the inversion response for increased Sn-content is noticeable, associated with decrease of the bandgap. The physics of this behavior is beyond the scope of this work and will the subject of further studies.

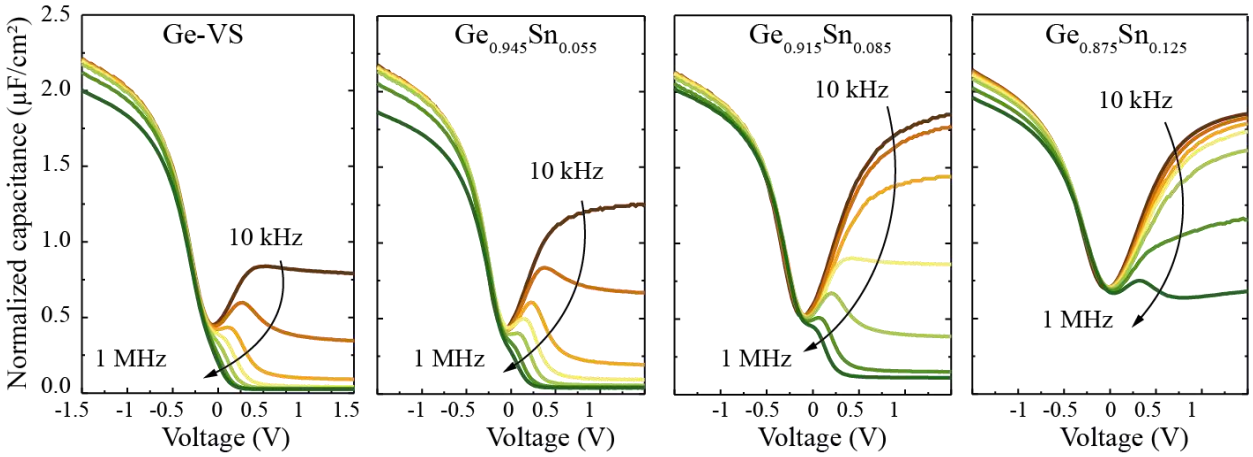

Figure 7: C-V characteristics of various GeSn capacitors fabricated using optimized 20 nm TaN/ 5 nm HfO_2 gate stacks.

SUMMARY

In summary, we have fabricated and analyzed TaN/HfO_2 high-k/metal gate stacks on low bandgap group IV GeSn and SiGeSn alloys with a large stoichiometry range. The surface treatment prior to metal gate deposition has been optimized for (Si)GeSn. Electrical as well as physical analysis confirmed the good interfacial quality of the high-k/metal gate stacks with D_{it} values ~ $2x10^{12}$ $cm^{-2}eV^{-1}$. We have presented the first study of SiGeSn MOS capacitors with an enhanced thermal stability, as compared to GeSn with Sn concentrations where it possesses a direct bandgap. With the aim of CMOS compatible device fabrication from Sn-based direct band gap group IV alloys, we have developed a low temperature atomic vapor deposition process for TaN metal gates. Our high-k/metal gate process has been validated by electrical characteristics on various high Sn contents (Si)GeSn alloys with bandgaps around ~0.45-0.70 eV. With the now available high-k/metal gate process, together with Ni(Si)GeSn metal contacts formation on high Sn content (Si)GeSn alloys[25] the fabrication of FET devices on direct band gap (Si)GeSn is in progress.

ASSOCIATED CONTENT

Supporting Information. Not available. This material is available free of charge via the Internet at http://pubs.acs.org.

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