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Design and Application of RFIC Detector: To Measure Coupled Power into IC Pin via PCB Trace

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***Abstract*—In this paper, we discuss the design of an RF IC detector with eight channels connected to the package pins, designed to determine the incident RF power on each pin. Some of these channels possess different sensitivity levels based on the amplification circuit block they use. A PCB test bench with test tracks has been designed to allow the measurement of RF power coupled to the detector IC pins when illuminated by a RF source. Our discussion will also encompass the applications of the RF IC detector in detecting stochastic EM fields in reverberant or equivalent real-world environments. The key contribution in this paper is the design of RF IC detector which has these applications.**

Keywords— Integrated Circuits, Absorption cross-section, Electromagnetic Interference, Shielding Effectiveness, Reverberation Chamber, Radio Frequency IC Detector.

I. Introduction

Printed circuit boards (PCBs), populated with many integrated circuits (ICs), are susceptible to radiated electromagnetic interference (EMI) coupled by various possible paths including direct pick-up on PCB traces. In [1], the consideration of coupled power in individual PCB traces and their attached loads are discussed. The exploration of coupled power, especially concerning known loads on lossless PCB traces and energy coupling into IC packages in [2] and [3], has been addressed. Building upon this previous work, the focus of this paper is on measurement of the coupled power into realistic loads, such as ICs in reverberant environment.

Various RF IC detectors are available on the market. The primary motivation for designing a custom RF IC detector, is that we have a comprehensive knowledge of the internal chip and package details. This information is essential to analyze its behavior and internal floor planning which is not possible with off-the-shelf RF IC detectors. The custom-designed RF IC detector plays a crucial role in validating the numerical model capable of estimating stochastic EM fields coupled into PCB traces and supports the development of an analytical model capable of predicting the probability of susceptibility of ICs to EMI.

II. Design of RF IC Detector

The RF IC detector is calibrated to measure coupled RF power at package pins via test RF PCB tracks in radiated tests. It comprises two channels (C1 and C2), each with four sub-channels (SC0, SC1, SC2, and SC3), where SC0 and SC1 handle RF amplification, SC2 connects directly to the Peak Detector, and SC3 offers dual inputs to the differential instrumentation amplifier as shown in Fig. 1. Controlled by a 3 to 8-line decoder linked to an external microcontroller, The analogue multiplexer connects channels and the detectors feature a separate shorting switch across the output capacitor whose reset controlled by a 3 to 8-line decoder operated by an external microcontroller. C1 and C2 have identical input circuits but with different series protection resistances in the IO block that connects to the external pin.

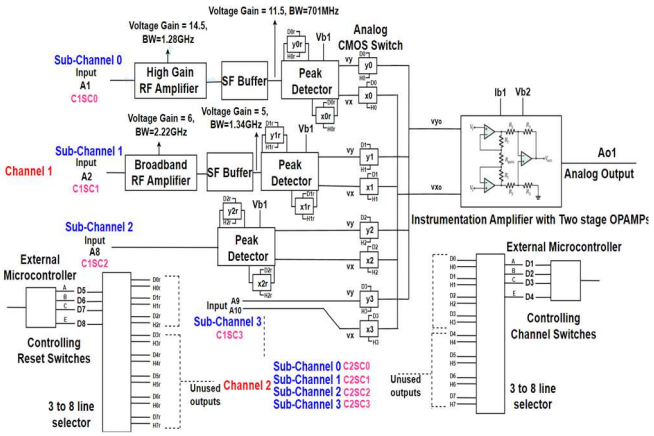

Fig. 1: Block diagram depicting RF IC detector functionality and structure.

A. RF Gain Amplifier and RF Broadband Amplifier

Both RF gain and broadband amplifier uses a cascode circuit employing the Common Source-Common Gate (CS-CG) configuration, with a PMOS current mirror serving as the high-impedance load. This combination leverages the advantages of cascode techniques, resulting in high gain, wide bandwidth, and good linearity. The initial stage employs the common source (CS) amplifier, acting as the input stage and driven by an external signal source. Conversely, the common gate (CG) amplifier serves as the output stage.

B. Source Follower Buffer and Peak Detector

The source follower (SF) amplifier shields the RF amplifier from detector loading by operating in a common-drain configuration. The simple peak detector (PD) design involves a Schottky diode, and a capacitor, with a resistor used for discharging the capacitor. However, in our application, we opt for an analog reset switch (section D) to instantly discharge the capacitor instead of using a resistor. To address a 'zero input charging' issue during simulation due to diode leakage, we integrated a dummy peak detector in the

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opposite configuration, hence we have the differential outputs Vx and Vy as shown in Fig. 1.

C. *Instrumentation Amplifier*

The Instrumentation Amplifier (IA) is constructed using two-stage Op Amps. It incorporates three Op Amps, with two functioning as input buffer amplifiers and the third serving as a differential amplifier. In the RF IC detector, two IAs are employed, one for each channel, shared across sub-channels.

D. *A 3 to 8-line decoder and Analog CMOS Switch*

Channel and sub-channel switching and capacitor reset switching of the RF IC detector are managed through analogue CMOS switches, which are controlled by two different 3-to-8-line decoders as shown in Fig. 1.

A 3-to-8-line decoder block, also termed a 3-to-8-line selector, is realized using eight four-input NAND gates. The decoder is augmented by eight inverters at the output, ensuring both high and low outputs. A simple analogue CMOS switch block is designed using NMOS and PMOS transistors.

Integrating these circuit block configurations as shown in Fig. 1 offers varying sensitivity levels across sub-channels.

E. *PAD Ring Design*

To establish the connection between the IC die and the package pins, a pad ring is essential. The pad ring serves as a platform for bonding pads, ESD protection circuits, and IO buffers for digital circuits. In this design, each side of the pad ring consists of 13 I/O cells, with five of them allocated for power supply and ground connections (VDD5, VDDR, VDDO, GNDO, and GNDR) on each side. Here, VDDR, VDDO, and VDD5 feed into a common power supply rail, while GNDO and GNDR feed into a common ground rail. This configuration results in a total of 52 I/O cells with 13 cells on each side. The pad ring measures 1.52 mm x 1.52 mm, and each I/O cell adheres to a standard size of 85 µm. The full Cadence layout with PAD ring is shown in Fig. 2.

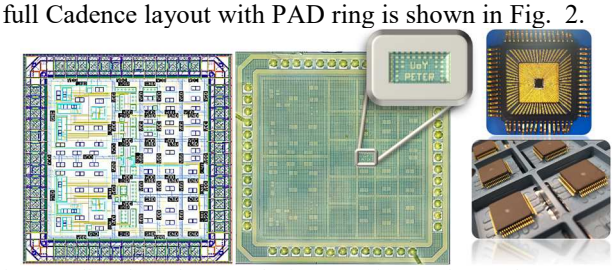

Fig. 2: Full Cadence layout and microscope image of RFIC detector.

III. PCB Test Bench for RFIC Detector

Fig. 3 shows the interconnection between the RF IC detector and subsequent blocks for digital control, voltage regulation, bias voltage provision, and output signal amplification. The right of Fig. 4 shows the physical layout of the detector (top) and control (bottom) boards. The top board houses the RF IC detector, which is connected to MCX RF connectors via PCB tracks.

The middle board serves as a connector between the top and bottom control boards, facilitating communication and data transfer via PCIe connectors. The bottom control board is centered around an Arduino Nano [4] microcontroller; a dual 12-bit digital to analogue converter (DAC) providing adjustable bias voltages; a programmable gain amplifier with an 8-channel input multiplexer which allows the Arduino to measure the detector IC channel outputs and other critical bias and operating voltages; along with a voltage regulator and other utility components.

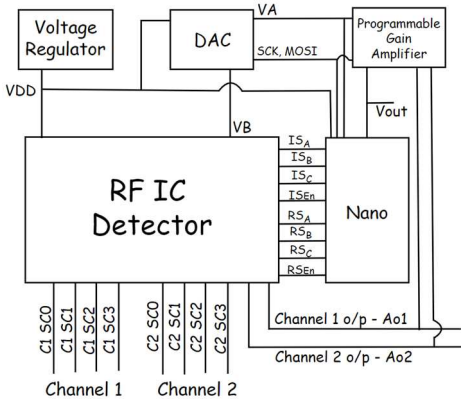

Fig. 3: Concise block diagram of the PCB test bench setup.

Two different top boards have been designed for conducted measurement and radiated measurement. This distinction is due to differences in the characteristic impedance of the RF PCB trace and the dielectric properties used in these boards, which are selected based on the testing environment. De-embedding of the RF PCB trace from conducted measurements is straightforward, as explained in the next section.

IV. Conducted Measurement of RFIC Detector

A. *S-parameter measurement of RFIC detector*

The S-parameter measurement conducted in this work aim to calculate the impedance at the package pins of the IC. This impedance information will facilitate the calibration of the RF IC detector to detect power from the voltage output.

The top board designed for conducted measurements incorporates 18 MCX connectors, each connected to a 36mm long microstrip transmission line that establish connections between the RF IC detector and the conducted board through 50 Ω RF PCB tracks. This equal length 50 Ω tracks facilitate easy de-embedding. Additionally, essential test pins are also included for functionality tests.

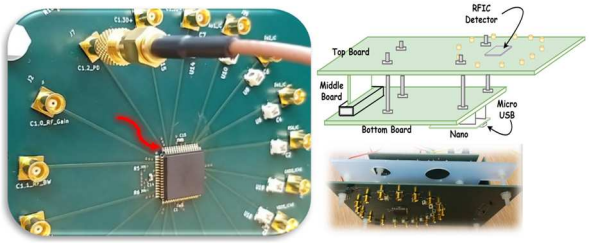

Fig. 4: In the left picture red arrow mark indicates the reference plane set for the VNA after TRL/M calibration and the right figure shows the physical layout of the detector (top) and control (bottom) boards.

The measurement setup shown in Fig. 5 includes a Rhode & Schwarz Vector Network Analyzer [VNA] ZVB20 [5], with port 1 or port 2 used to measure the S-parameters of each of the pins of the RF IC detector, while the remaining ports are left unconnected. The RF IC detector testbench and VNA are monitored by a computer.

1) Reference Plane at Package Pin after TRL/M Calibration

To eliminate the impact of 50 Ω RF PCB trace and to set the reference plane at package pin, a Thru Reflect Line/Match (TRL/M) calibration is employed. This calibration involves

employing a specially designed TRL/M calibration board with identical PCB traces and dielectric properties as the original conducted test board. This calibration enables accurate measurement of S-parameters at the package pins, facilitating impedance determination and precise power analysis for both incoming and reflected signals.

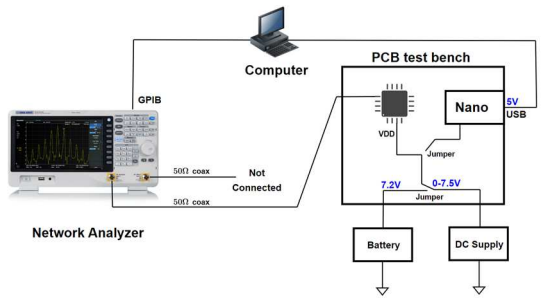

Fig. 5: Shows the S-parameter measurement setup.

After TRL/M calibration, the reference plane of the VNA is at the end of the RF PCB track connected to the RF IC detector package pin, as shown in Fig. 4, and the S-parameter measurement has been performed.

2) Impedance calculation at package pin using S-parameters after TRL calibration

From the determination of the input impedance of the RF IC detector at the package pins, we can assess the relationship between forward power, absorbed power and voltage at the package pins. This knowledge is essential to compare the simulation results with measurement data and to verify the direct power injection (DPI) measurements for calibrating the RF IC detector for radiated measurement.

After TRL/M calibration, we can determine the input impedance (Z_{in}) of the RF IC detector at package pins, using the equation given below,

$$Z_{in} = Z_0 \frac{(1+\Gamma_{11})}{(1-\Gamma_{11})} \quad (1)$$

where, Γ_{11} is the reflection co-efficient measured after calibration at the package pin, and Z_0 is the characteristic impedance of the system.

B. DPI for RFIC detector

Due to varying sensitivities among sub-channels, different input forward power levels are needed for proper detection in each of these inputs. In this section by conducting DPI measurements, we will calibrate the RF IC detector test bench for radiated measurements in the reverberation chamber and also we will observe the transient response of one of the RF IC detector's sub-channels. The measurement setup depicted in Fig. 5 for S-parameter measurement is also employed for DPI measurement.

1) Calibration of RF IC Detector Test Bench For Radiated Measurements

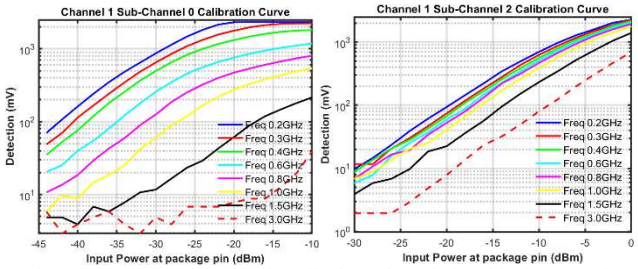

Fig. 6. Calibration curve that displays the relationship between input forward power at package pin.

Fig. 6 presents calibration curves for SC0 and SC2 of C1. The sensitivity of the detector's input was evaluated by injecting various known forward power levels across the operating frequency band. This procedure facilitated the creation of a calibration map for radiated measurements using the RF IC detector.

Integrating these calibration curves from all sub-channels into the driver software during radiated measurements enabled the measurement of the coupled forward power at the package pin.

2) Transient Analysis of SC0

In this section, we analyze the transient response of the RF IC detector for SC0 of C2. The transient analysis allows us to visually observe the behaviour of the RF IC detector over time.

To compare the measurement results with the simulation, the voltage provided at the input during the simulation is converted to forward power (P_{for}) at the respective package pin during the measurement using the following equation:

$$P_{for} = \frac{P_{ab}}{(1-|\Gamma_{IC}|^2)} = \left(\left(\frac{V_{pp}}{2\sqrt{2}}\right)^2 Re\left\{\frac{1}{Z_{in}^*}\right\}\right)/(1-|\Gamma_{IC}|^2) \quad (2)$$

where P_{ab} is the absorbed power into package pin, Γ_{IC} is the reflection coefficient at the package pin, V_{pp} is the peak to peak voltage at the bond pad of the package pin, and Z_{in}^* is the conjugate of the input impedance at the package pin of respective sub-channel under test.

Fig. 7 illustrates the measured transient response of SC0 of C2 extracted from an oscilloscope, while Fig. 8 presents the comparison of the measured and simulated transient responses.

The measurement results nearly align with post-layout simulations from Cadence in Fig. 8, falling within the expected process variation range. Slight deviations in output bias points are observed, attributed to component discrepancies, parasitic effects, or manufacturing variations. These variations do not compromise the RF IC detector's overall performance, validating the design and manufacturing processes.

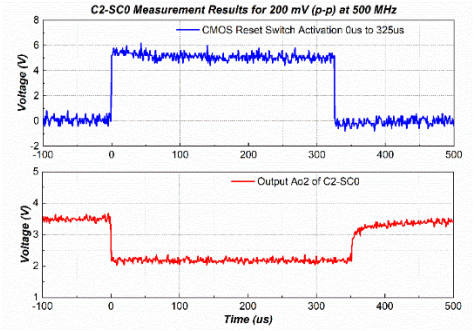

Fig. 7: Shows the transient response measurement result extracted from an oscilloscope, when -7.66 dBm (P_{ab}=-12.26 dBm, V_{pp}= 200 mV) of input forward power at package pin is given at 500 MHz for sub-channel 0 of channel 2 of the RF IC detector.

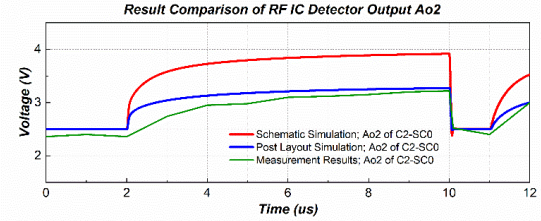

Fig. 8: Shows the transient response comparison between cadence schematic simulation, post-layout simulation and measurement of SC0 of C2 of the RF IC detector.

V. Radiated Measurement in Reverberant Environment

This section presents measurements conducted in the Reverberation Chamber to measure the coupled power at package pins of the IC via test RF PCB tracks in a reverberant environment or its equivalent. In a real-world setting, victim electronic components can receive EMI signals from multiple directions and polarizations simultaneously, originating from a single external interference source, and thus the reverberant case takes into account this multiplicity.

A. Measurement Setup

Fig. 9 shows the measurement setup used for radiated measurements within a reverberation chamber (4.7m x 3.0m x 2.37m). These measurements cover 100 stirrer positions spanning from 200 MHz to 2 GHz, with a 20 MHz frequency increment. A power signal generator drives a broadband antenna to generate the field in the chamber which is monitored by a second broadband antenna. Coupling to each detector channel is measured by the test bench and transmitted to the instrument controller by the USB interface of the Arduino processor. The measurement equipment, including the PCB test bench of the RF IC detector, is monitored using Python software.

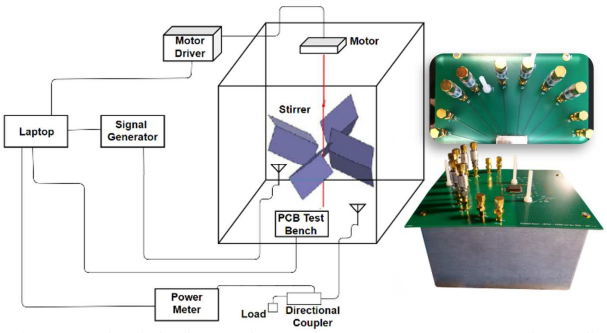

Fig. 9: The left figure shows the measurement setup for radiated measurement with pictures and the right pictures show the assembled test setup featuring the radiated PCB board (180 x 153 mm^2) at the top, with all PCB tracks terminated by 115Ω loads for accurate evaluation.

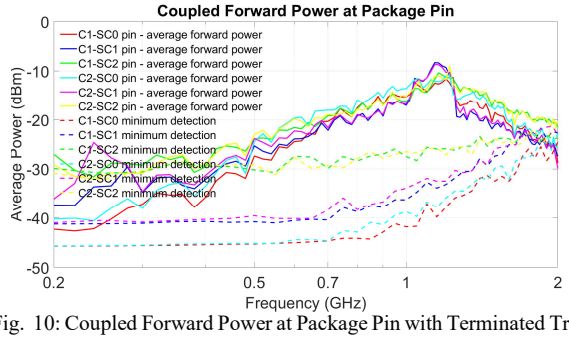

Fig. 10: Coupled Forward Power at Package Pin with Terminated Tracks: Demonstrating power coupling at the package pin with terminated tracks, using a 29dBm input power at the chamber.

The entire test bench, encompassing the bottom control board, middle board, and the underside of the radiated board, is shielded. The only part exposed to the reverberant environment is the upper side of the radiated board, as shown in Fig. 9. The RF PCB tracks have a characteristic impedance of 115 Ω, adjusted to match the external 50 Ω system by adding a 65 Ω series resistance at the track's end. To interface with the 50 Ω load, DC blocks are inserted between the PCB tracks, while the RF IC detector's sub-channels lack internal DC blocks.

B. Average Coupled Forward Power at Package Pin

The average coupled forward power at package pins for SC0 to SC2 of C1 and C2 is depicted in Fig. 10 with solid lines. The dotted lines in the figure represent the minimum forward power level required for the RF IC detector to detect at least a 10mV output voltage. Similar to the open track case, all sub-channel detection exceeds this minimum threshold at 500MHz, and thus, all the curves converge while retaining a nearly identical shape.

VI. Applications, Conclusion and Future Work

The custom-designed RF IC detector presented in this paper has been successfully responded in measuring coupled power into realistic load such as package pins of the IC via test PCB tracks in reverberant or equivalent real-world environment. The RF IC detector is capable of measuring coupled power at package pins between -44dBm and 0dBm, both in reverberant (tested) and non-reverberant environments. It contributed to the validation of the updated numerical model from [1] capable of estimating the EM field coupled into PCB traces and the analytical model capable of predicting the probability of susceptibility of ICs to EMI [6] (under review). Furthermore, it also enabled the study of the influence of stochastic EM field coupling into PCB traces and package pins of the ICs using the power balance (PWB) model.

This application of estimating the probability of susceptibility of ICs holds significant value for the EMC community. Additionally, the application of the enhanced PWB method will contribute to the development of improved shielding and PWB techniques, allowing for the assessment of the effectiveness of different components. Future work can focus on investigating package pin cross-couplings between the RF IC detector's package pins, PCB tracks, connectors, and multiple components on the PCB, which will help enhance the accuracy of the updated numerical model and the analytical model from [6] (under review).

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