Letters

Stabilization of a Cascaded DC Converter System via Adding a Virtual Adaptive Parallel Impedance to the Input of the Load Converter

Xin Zhang, *Member, IEEE*, Qing-Chang Zhong, *Senior Member, IEEE*, and Wen-Long Ming

***Abstract*—Connecting converters in cascade is a basic configuration of dc distributed power systems (DPS). The impedance interaction between individually designed converters may make the cascaded system become unstable. The previous presented stabilization approaches not only need to know the information of the regulated converter, but also have to know the characteristics of the other converters in the system, which are contradictory to the modularization characteristic of dc DPS. This letter proposes an adaptive-input-impedance-regulation (AIIR) method, which connects an adaptive virtual impedance in parallel with the input impedance of the load converter, to stabilize the cascaded system. This virtual impedance can adaptively regulate its characteristic for different source converters. Therefore, with the AIIR method, all the load converters can be designed to a fixed standard module to stably adapt various source converters. In addition, at any cases, the AIIR approach only changes the load converter's input impedance in a very small frequency range to keep the load converter's original dynamic performance. The requirements on the AIIR method are derived and the control strategies to achieve the AIIR method are proposed. Finally, considering the worst stability problem that often occurs at the system whose source converter is an *LC* filter, a load converter cascaded with two different *LC* input filters is fabricated and tested to validate the effectiveness of the proposed AIIR control method.**

***Index Terms*—Adaptive-input-impedance-regulation, cascaded system, input impedance regulator, load converter, modularization, stability, virtual impedance.**

I. Introduction

THE dc distributed power systems (DC DPS) have been widely used in space stations, shipboard, hybrid vehicles, and renewable energy systems in the last few decades, thanks to their flexible system configurations, high efficiency, and high density power delivery capability [1]–[3]. One of the DC DPS' attractive characteristics is modularity design [4], in which each subsystem is first designed individually as a module, and then all subsystems are integrated to form DC DPS. The modularization characteristic of DC DPS considerably cuts down the system's development cycles and costs.

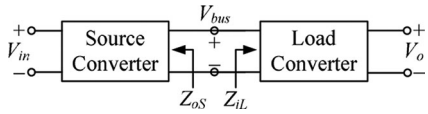

Fig. 1. Typical cascaded system.

In DC DPS, there are various ways to connect subsystems, and a typical connection style is the cascaded configuration. Fig. 1 shows a typical cascaded system, which is composed of a source converter and a load converter. Though both the source and load converters can work well individually, their interactions may cause the instability of the whole system [5]–[7]. This stability problem is not really a new problem and was first reported and researched in op-amps in 1930s [8], [9]. Generally speaking, in a cascaded system, if Z_{oS}/Z_{iL} satisfies the Nyquist criterion [10], [11], the system will be stable, where Z_{oS} is the output impedance of the source converter and Z_{iL} is the input impedance of the load converter.

In order to meet the Middlebrook criterion, various solutions have been proposed, and they can be classified into two types: passive [12], [13] and active [14]–[16] methods. For passive methods, passive components, such as resistors, capacitors, and inductors, are employed. In [12] and [13], RC and RL dampers were introduced to reduce the output impedance resonant peak of the source converter, so that Z_{oS} is less than Z_{iL} in the entire frequency range and, thus, the system stability is guaranteed. However, the adoption of passive components might lead to significant power losses. As a result, active methods, which were based on advanced control of the source converter [14] and/or the load converter [15], or adding a power buffer between the source and load converters [16], were proposed.

However, compared to the stability solutions by changing the source converter's output impedance, the methods of regulating the load converter's input impedance are more difficult. This is because the load converter's input impedance is preferred to be regulated as a negative resistor for good dynamic performance [17], but this negative resistor characteristic constitutes a major problem for the stability of a cascaded system [18]. Accordingly, it is a big challenge to regulate the load converter's input impedance when ensuring the stability of the cascaded system and good dynamic performance of the load converter simultaneously. In [19], one solution to this contradictory issue was presented by developing the regulation signal maps of the

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X. Zhang and W.-L. Ming are with the Department of Automatic Control and Systems Engineering, The University of Sheffield, Sheffield S1 3JD, U.K. (e-mail: xin.zhang@sheffield.ac.uk; wenlongming@gmail.com).

Q.-C. Zhong is with the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL 60616 USA, and also with the Department of Automatic Control and Systems Engineering, The University of Sheffield, Sheffield S1 3JD, U.K. (e-mail: zhongqc@ieee.org).

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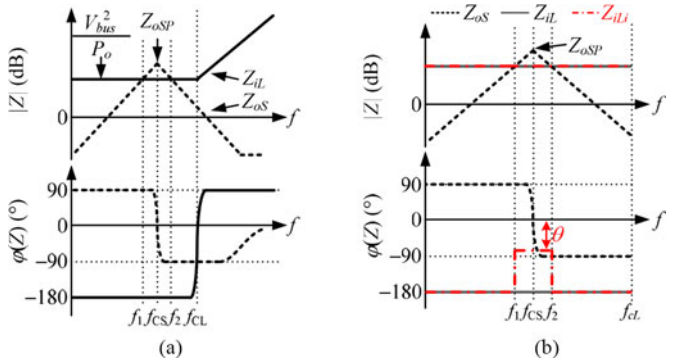

Fig. 2. Load converter's: (a) instability reason, (b) improvement.

source converter into the regulation loop of the load converter. However, this method may be unachievable in some applications. For instance, if the source converter is a simple *LC* filter, there do not exist regulation signals of the source converter, and as a result, the load converter's input impedance cannot be regulated to stabilize the cascaded system. Moreover, if the source converter is an *LC* filter, its output impedance is higher than that of other types of source converters and the system's stability problem is more likely to appear [20]. In order to overcome this shortage, a more general stability solution was proposed in [21] to improve the stability of the cascaded system via shaping the input impedance of the load converter with a parallel or series virtual impedance.

In addition, all the above-mentioned solutions not only need to know the information of the regulated converter, but also have to know the characteristics of the other converters in the system, leading to the redesign of the regulated converters with different source/load converters. This contradicts with the objective of the modularity design of DC DPS and, hence, increases the system's development cycles.

This letter introduces an AIIR method to connect a self-regulated virtual impedance in parallel with the load converter's input impedance. Thanks to this virtual impedance, the load converter can change its input impedance adaptively with different source converters to stabilize the whole system. Therefore, the AIIR method can help all the load converters to achieve modularization stably in different DC DPS. Furthermore, the proposed method only modifies the load converter's input impedance in a very small frequency range to keep the original dynamic performance of the load converter.

The other parts of this letter are organized as follows: In Section II, the instability reason of the cascaded system is reviewed and the improvement of the load converter's input impedance is discussed. Then, the AIIR control strategy is presented in Section III. After that, two different cascaded systems as numerical examples, which are composed of two different *LC* input filters and the same load converter, are designed and experimentally implemented to verify the effectiveness of the proposed AIIR method in Section IV. Finally, Section V concludes this letter.

II. Instability Reason and Improvement of the Input Impedance of the Load Converter

Fig. 2(a) shows the bode plots of Z_{oS} and Z_{iL} at a typical instability case. Here, if the source converter is a switching-mode power supply, $f_{\rm CS}$ is the cutoff frequency of its voltage loop; if the source converter is an LC input filter, $f_{\rm CS}$ is the filter's resonant frequency. Besides, $f_{\rm CL}$ is the cutoff frequency of the load converter's voltage loop. Z_{oSP} is defined as the peak value of Z_{oS}. According to Fig. 2(a), the cause of the instability can be summarized as follows. If Z_{oS} is intersected with Z_{iL}, and if $f_{\rm CS}$ is less than $f_{\rm CL}$, the cascaded system is unstable even if the subsystems can work well individually [22]. The -180° phase resulted by the load converter's negative resistor characteristic is the main factor that causes the instability of the cascaded system [23]. According to Fig. 2(a), the worst case of instability problem of a cascaded system occurs at full load and with an LC filter as the source converter.

According to Fig. 2(a), there is nothing more desirable than changing Z_{iL} only in the vicinity of the intersection frequencies (f_1 and f_2) of $|Z_{oS}|$ and $|Z_{iL}|$, to stabilize the cascaded system while keeping a better dynamic performance of the load converter. Therefore, as shown in Fig. 2(b), this letter only compensates the phase of Z_{iL} during $[f_1,\ f_2]$, which can ensure $|\varphi(Z_{oS}) - \varphi(Z_{iL})| < 180^\circ$ at the intersection frequency range. Here, the improved input impedance of the load converter Z_{iLi} can be expressed as

$$Z_{iLi} = \begin{cases} -|Z_{iL1}|\, e^{j\theta} & f \in [f_1,\ f_2] \\ Z_{iL} & f \notin [f_1,\ f_2] \end{cases} \tag{1}$$

where Z_{iL} is the original input impedance of the load converter, $|Z_{iL1}|$ and θ are the magnitude and phase of the improved input impedance of the load converter within $[f_1,\ f_2]$, respectively. In order to ensure $|\varphi(Z_{oS}) - \varphi(Z_{iLi})| < 180^\circ$, θ should meet $\theta \in (-90^\circ,\ 90^\circ)$. Since $|\varphi(Z_{oS}) - \varphi(Z_{iLi})| < 180^\circ$ at $[f_1,\ f_2]$, $|Z_{iL1}|$ can be any values. In order to minimize the resulting effect on the load converter, $|Z_{iL1}|$ is designed to be equal to $|Z_{iL}|$ [see Fig. 2(b)].

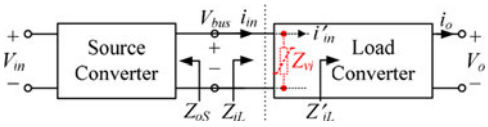

Fig. 3. Cascaded system with parallel-connected virtual impedance.

III. AIIR Control Strategy

A. Adaptively Regulated Virtual Impedance $Z_{\rm via}$

As shown in Fig. 3, if a virtual impedance Z_{vi} is added in parallel with the input port of the load converter, the load converter's input impedance is changed to

$$Z_{iL} = Z'_{iL} \parallel Z_{vi} = \left(Z'_{iL} \cdot Z_{vi}\right) / \left(Z'_{iL} + Z_{vi}\right) \tag{2}$$

where Z'_{iL} is the original input impedance of the load converter and if $f < f_{cL}$ its expression is $-V_{\rm bus}^2/P_o$.

According to (1) and (2), if $Z_{iL} = Z_{iLi}$, Z_{vi} can be selected as

$$Z_{vi} = \begin{cases} \left(V_{\rm bus}^2/P_o\right) \cdot \left[e^{j\theta}/(1+e^{j\theta})\right] & f \in [f_1,\ f_2] \\ +\infty & f \notin [f_1,\ f_2]. \end{cases} \tag{3}$$

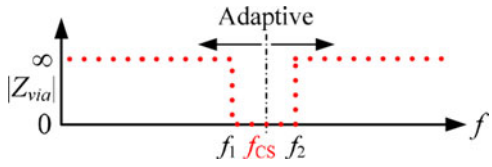

Fig. 4. Adaptively regulated virtual impedance $Z_{\rm via}$.

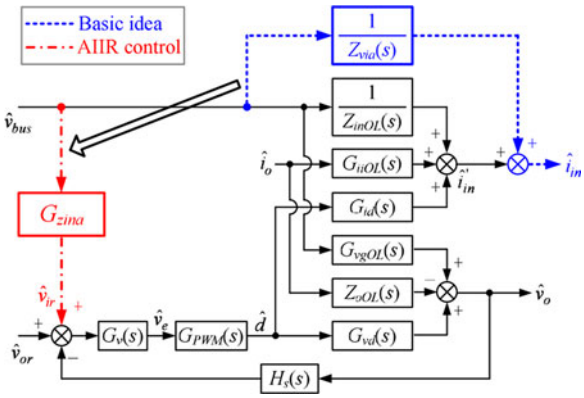

Fig. 5. Concept of AIIR control strategy.

As seen from (3), within $[f_1, f_2]$, Z_{vi} is a constant value, which is determined by the load converter, otherwise, $Z_{vi} = +\infty$. Since f_1 and f_2 are very close to $f_{\rm CS}$ [see Fig. 2(a)], the frequency characteristics of Z_{vi} are also affected by the source converter. In other words, for a particular load converter, if its source converter is changed, its Z_{vi}'s frequency characteristics are needed to be accordingly changed. However, if Z_{vi} can be changed according to the source converter adaptively, as shown in Fig. 4, the load converter is not required to be changed anymore. Therefore, the adaptively regulated virtual impedance $Z_{\rm via}$ is the main aim of the proposed AIIR control strategy.

B. Concept of AIIR Control Strategy

Fig. 5 shows the small-signal control block of the original load converter. Its variables and transfer functions are described in Table I. If $Z_{\rm via}$ is required to be added in parallel with the input port of the load converter, one intuitive way is to introduce $1/Z_{\rm via}$ to the control block between the input voltage and input current (as shown with dashed lines in Fig. 5). However, this method cannot be achieved by control directly. In order to address this issue, the output of $1/Z_{\rm via}$ is moved to the output voltage reference and, hence, the transfer function to $G_{\rm zina}(s)$ can be equivalently adjusted, as shown with the dot-dashed lines. Fig. 5 is the concept of the proposed AIIR control strategy, and $G_{\rm zina}(s)$ is expressed as

$$G_{\rm Zina}(s) = \frac{1}{Z_{\rm via}(s)} \cdot \frac{1 + T_v(s)}{G_v(s) \cdot G_{\rm PWM}(s) \cdot G_{id}(s)} \tag{4}$$

where $T_v(s) = H_s(s)G_v(s)G_{\rm PWM}(s)G_{vd}(s)$ is the loop gain of the voltage closed-loop of the load converter.

TABLE I
VARIABLES AND TRANSFER FUNCTIONS OF LOAD CONVERTER

$\hat{v}_{bus}$	Disturbance of the bus voltage	$\hat{i}_{ino}$	Disturbance of the input current
$\hat{v}_o$	Disturbance of the output voltage	$\hat{i}_o$	Disturbance of the output current
$\hat{d}$	Disturbance of the duty cycle	$\hat{v}_{or}$	Disturbance of the output voltage reference
$G_{PWM}(s)$	Transfer function of the modulator	$H_s(s)$	Sampling coefficient of the output voltage
$G_v(s)$	Transfer function of the voltage regulator	$Z_{inOL}(s)$	Open-loop input impedance
$Z_{oOL}(s)$	Open-loop output impedance	$G_{id}(s)$	Control to input current transfer function
$G_{vd}(s)$	Control to output voltage transfer function	$G_{iiOL}(s)$	Open-loop load to input current transfer function
$G_{vgOL}(s)$	Open-loop input to output voltage transfer function		

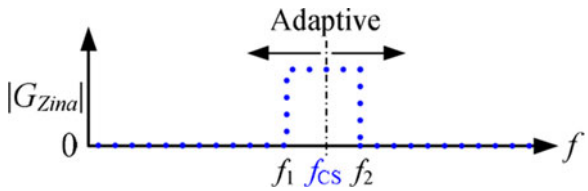

Fig. 6. Adaptive characteristic of $|G_{\rm zina}(s)|$.

C. Realization of $G_{\rm zina}(s)$

Substituting (3) into (4), the adaptive regulator $G_{\rm zina}(s)$ can be further derived as

$$G_{\rm Zina}(s) = \begin{cases} \dfrac{P_o(1+e^{-j\theta})\left[1+T_v(s)\right]}{V_{\rm bus}^2 G_v(s) G_{\rm PWM}(s) G_{id}(s)} & f \in [f_1, f_2] \\ 0 & f \notin [f_1, f_2]. \end{cases} \tag{5}$$

As seen from (5), $G_{\rm zina}(s)$ is an adaptive frequency-based piecewise function, which is shown in Fig. 6, where $|G_{\rm zina}(s)|$ is a nonzero value within $[f_1,\ f_2]$ and zero outside$[f_1,\ f_2]$. Since f_1 and f_2 are very close to $f_{\rm CS}$, an adaptive bandpass filter $G_{\rm BPFa}(s)$, whose center frequency is $f_{\rm CS}$, can be used to realize $G_{\rm zina}(s)$, i.e.

$$G_{\rm Zina}(s) = G_{\rm Zin1}(s) \cdot G_{\rm BPFa}(s) \tag{6}$$

where

$$G_{\rm Zin1}(s) = \frac{P_o}{V_{\rm bus}^2} \frac{(1+e^{-j\theta})\left[1+T_v(s)\right]}{G_v(s) G_{\rm PWM}(s) G_{id}(s)} \tag{7}$$

$$G_{\rm BPFa}(s) = -\frac{s\left(2\pi f_{\rm CS}/Q\right)}{s^2 + s\left(2\pi f_{\rm CS}/Q\right) + \left(2\pi f_{\rm CS}\right)^2} \tag{8}$$

where Q is the quality factor of the bandpass filter, whose initial value is recommended as 0.707 and can be changed manually if needed; $f_{\rm CS}$ is changed adaptively according to different source converters. By [24], the numerator degree of $G_{\rm zina}(s)$ is always lower than its denominator degree for all dc/dc converters. As a result, $G_{\rm zina}(s)$ is a proper transfer function that can be fully implemented by digital processors.

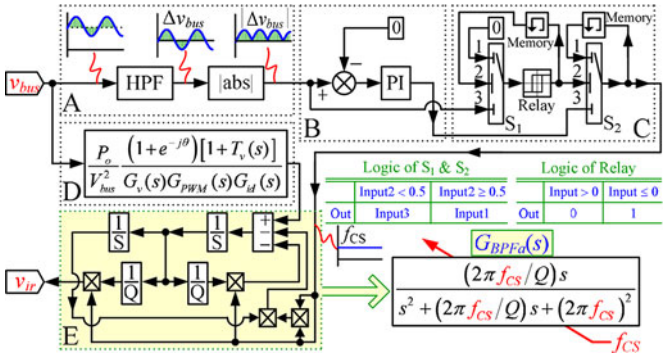

Fig. 7. Realization of the adaptive input impedance regulator $G_{\mathrm{zina}}(s)$.

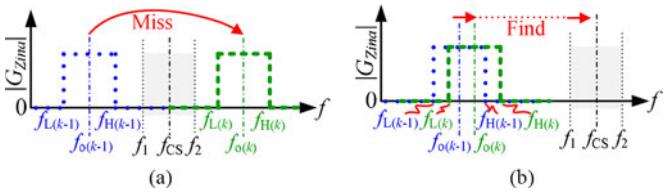

Fig. 8. Impact of K_p and K_i on $G_{\mathrm{zina}}(s)$: (a) large K_p and K_i, (b) small K_p and K_i.

According to (7), (8) and the dot-dashed line in Fig. 5, $G_{\mathrm{zina}}(s)$ can be realized by Fig. 7. As shown in Fig. 7, in subcircuit A, v_{bus} first goes through a high-pass filter $\frac{s}{s+10}$ to remove the dc component and to extract $\triangle v_{\mathrm{bus}}$, and then $|\triangle v_{\mathrm{bus}}|$ is obtained by an absolute value block. After that, this is compared with zero, and the error is amplified by a PI controller. If the system is unstable, the output of the controller would be increased from zero and regulate the center frequency of $G_{\mathrm{BPF}a}(s)$. Besides, if the output of the controller arrives at f_{CS}, Z_{via} would find its right frequency characteristics, stabilize the cascaded system, and make $|\triangle v_{\mathrm{bus}}| = 0$. At this moment, S_1 and S_2 would lock f_{CS} as the final center frequency of $G_{\mathrm{BPF}a}(s)$ immediately and not change it during the left running time. After that, any disturbances in the v_{bus} voltage level do not affect the parameters of $G_{\mathrm{zina}}(s)$. Here, the logic of S_1, S_2, and $Relay$ is given in Fig. 7. In addition, v_{bus} is also sent to subcircuit D to realize the function of $G_{\mathrm{zin1}}(s)$ in (7). The output of subcircuit D is sent to the adaptive bandpass filter $G_{\mathrm{BPF}a}(s)$ (see subcircuit E), whose center frequency is determined by the output of subcircuit C, to obtain the output of $G_{\mathrm{zina}}(s)$ in (6). Fig. 7 is the realization method of the adaptive input impedance regulator $G_{\mathrm{zina}}(s)$.

Note, though $G_{\mathrm{zina}}(s)$ can lock f_{CS} as the final center frequency of $G_{\mathrm{BPF}a}(s)$ after finding it, too large K_p and K_i parameters should be avoided in the design of the PI controller in the Section B of Fig. 7. As shown in Fig. 8(a), it is because, if K_p and K_i are too large, it may make the output of the PI controller increase so much during the first sampling period after the system is started and, hence, f_{CS} is skipped. As a result, small K_p and K_i are preferred for the PI controller [see Fig. 8(b)]. The only compromise is that the $G_{\mathrm{zina}}(s)$ may spend a slightly longer time before the right f_{CS} is found. However, if the AIIR controller finds the right f_{CS}, the PI controller will be disabled and the K_p and K_i do not affect any steady or dynamic performance of the load converter. Therefore, small K_p and K_i can be accepted practically.

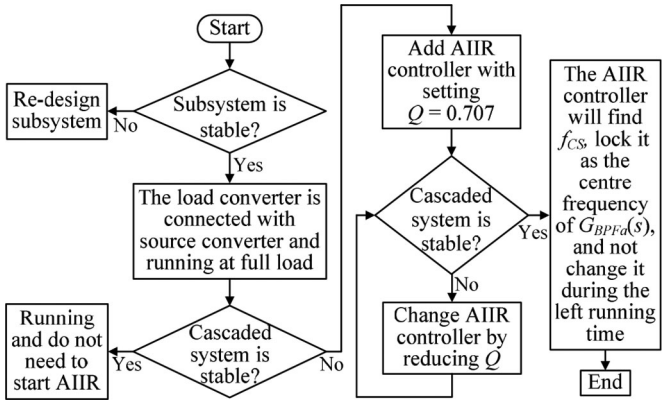

Fig. 9. Operation flow of the AIIR control method.

D. Operation Flow of the AIIR Control Method

Fig. 9 gives the operation flow of the AIIR control method. First, check both source and load converters to make sure they can work well individually. Then, if the cascaded system is unstable, the AIIR controller will be utilized. For the AIIR controller, the initial value of Q is set as 0.707. It is because $Q = 0.707$ can ensure a relatively narrow passband for $G_{\mathrm{BPF}a}(s)$, and if 0.707 is also suitable for Q, the AIIR controller not only can stabilize the cascaded system, but also can keep the original dynamic performance of the load converter. However, if the system is still unstable, it means that 0.707 is too larger than Q and the bandwidth of $G_{\mathrm{BPF}a}(s)$ is smaller than $(f_2 - f_1)$, then, Q should be reduced and the above procedures should be done again until the suitable Q is found.

It is worth pointing out that, though the type of the typical input voltage feed-forward control loop seems similar with the proposed AIIR control block, they are totally different. The purpose of the typical input voltage feed-forward control loop is to regulate the input impedance of the load converter as a pure negative resistor within the whole frequency range. However, the purpose of the AIIR control method is to remove the negative resistor characteristic out of the input impedance of the load converter. As a result, the proposed AIIR control method can stabilize the cascaded system, but the typical input voltage feed-forward method cannot.

IV. Experimental Verification

Since the worst instability phenomenon is most likely to happen at the cascaded system whose source converter is an *LC* filter, the AIIR control strategy is applied into two such unstable 100-W cascaded systems. As shown in Fig. 10, the two cascaded systems utilize the same load stage, which is a 48–24 V buck converter with 20-kHz switching frequency. If the load stage is connected to the source stage 1, which is an input filter formed

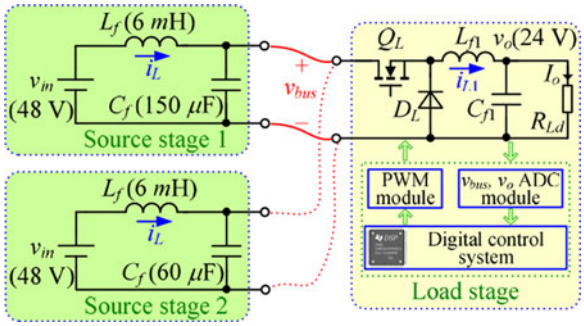

Fig. 10. Example cascaded systems.

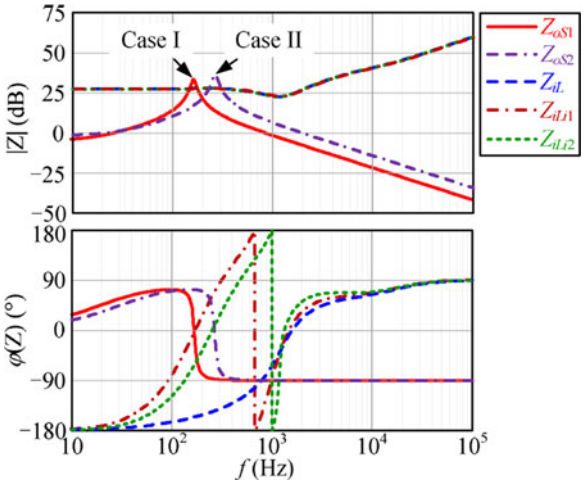

Fig. 11. Bode plots of example systems at full load.

by a 6-mH inductor and a 150-μF capacitor, the first unstable system is formed. On the other hand, if the load converter is connected to the source stage 2, which is an input filter whose inductor and capacitor are 6 mH and 60 μF, respectively, the second unstable system is then formed.

Fig. 11 shows the bode plots of the example systems, where Z_{oS1}, Z_{oS2}, and Z_{iL} are the output impedance of source stage 1, source stage 2, and the input impedance of the load converter at full load, respectively. It can be seen that both the cascaded systems are unstable.

According to Figs. 5 and 7, an adaptive input impedance regulator $G_{\rm zina}(s)$ is introduced to the load converter. Here, θ is selected as 0. Then, as shown in Fig. 11, Z_{iL} is modified into Z_{iLi1} in the first cascaded system and Z_{iLi2} in the second cascaded system adaptively. In this case, $|\varphi(Z_{oS}) - \varphi(Z_{iLi})| < 180^\circ$ at the intersection frequencies in both cases. Therefore, the modified cascaded system with the AIIR control method is stable and the design of $G_{\rm zina}(s)$ is appropriate. In addition, Fig. 11 also shows that $G_{\rm zina}(s)$ can achieve the modified input impedance in Fig. 2(b), i.e., only changing the input impedance's phase without changing its magnitude, which can minimize the resulting effect on the load converter.

The experimental results of the first example system are given in Fig. 12, where the waveforms of $v_{\rm bus}$ and v_o are their ac components to clearly show the oscillation (i_L, $v_{\rm bus}$, i_{L1}, and v_o are illustrated in Fig. 10). As seen from Fig. 12(a), this cascaded system is unstable without the AIIR control strategy. After the AIIR control strategy was applied, it spent about 45.56 ms to adjust the parameters of $G_{\rm zina}(s)$ and to stabilize the cascaded

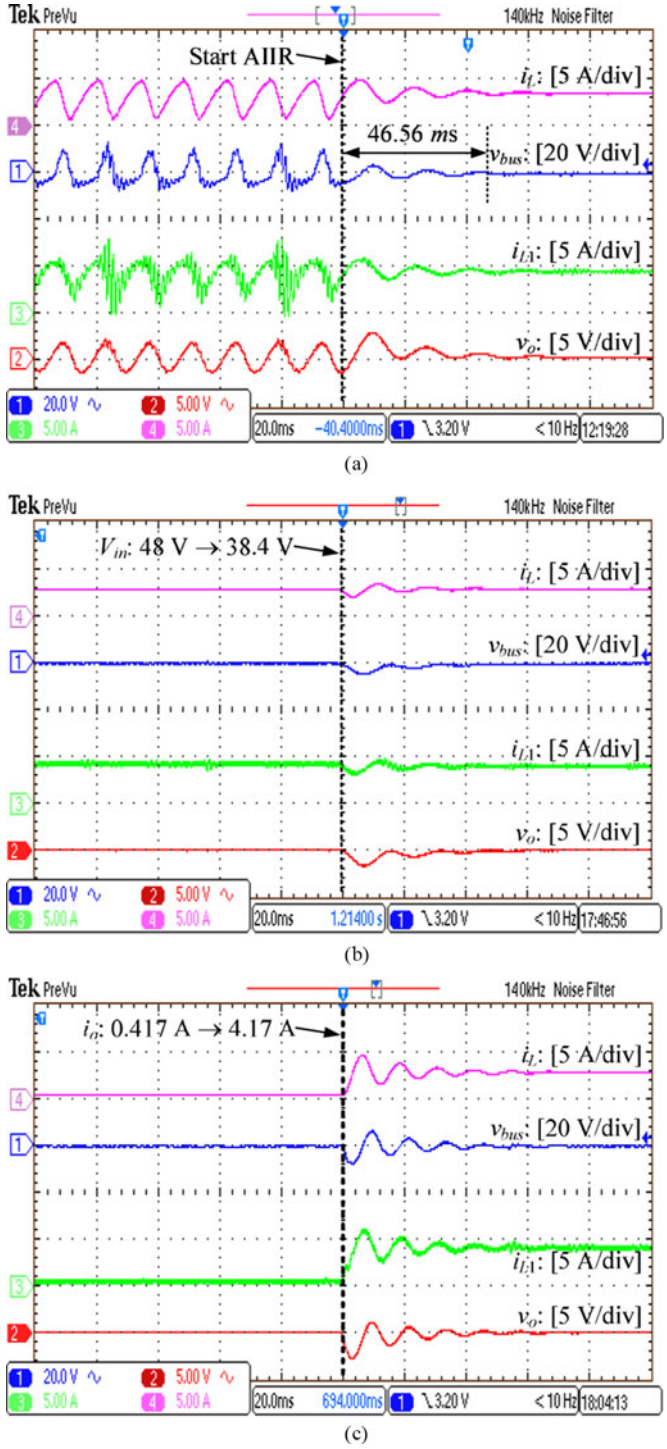

Fig. 12. Experimental waveforms with the source stage 1: (a) steady-state waveforms with rated input voltage and rated load, (b) dynamic waveforms when the input voltage stepped down from 100% rated to 80% rated voltage at full load, (c) dynamic waveforms when the load increased from 10% rated to 100% rated load at rated input voltage.

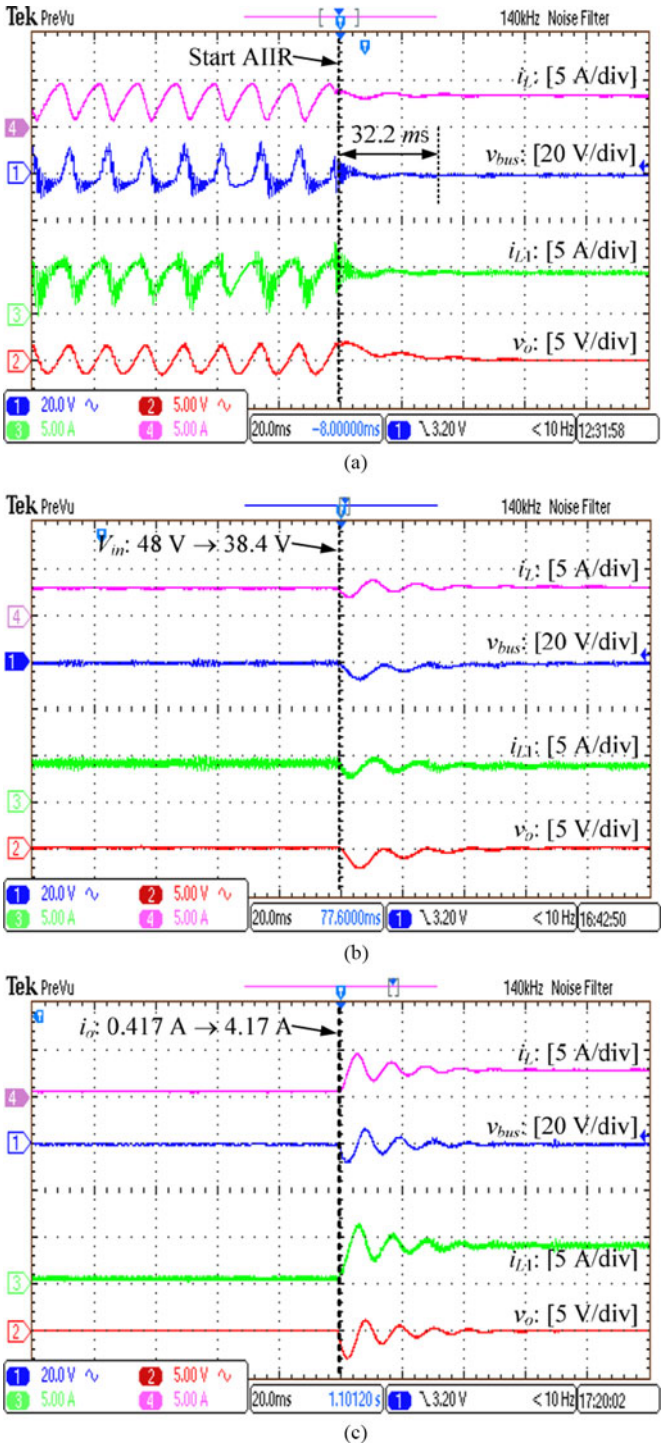

Fig. 13. Experimental waveforms with the source stage 2: (a) steady-state waveforms with rated input voltage and rated load, (b) dynamic waveforms when the input voltage stepped down from 100% rated to 80% rated voltage at full load, (c) dynamic waveforms when the load increased from 10% rated to 100% rated load at rated input voltage.

system automatically. Fig. 12(b) shows dynamic waveforms of the modified system with the AIIR control strategy when its input voltage stepped down from 100% rated to 80% rated voltage at the full load. It is clear that the AIIR control strategy can work well during an input voltage change. Fig. 12(c) shows dynamic waveforms of the modified system with the AIIR control strategy when its load increased from 10% rated to 100% rated load at the rated input voltage. It is demonstrated that the AIIR control strategy can also work well during a load change.

Similarly, Fig. 13(a)–(c) gives the steady-state waveforms, input voltage, and load dynamic waveforms of the second example system. Again, it is verified that the AIIR control strategy not only can adaptively solve the instability problem of the cascaded system, but also can work well during dynamic process.

V. Conclusion

In order to solve the instability problem of the cascaded system, and also to facilitate the modularization of DC DPS, AIIR control strategy has been proposed in this letter. It has been theoretically demonstrated that the proposed strategy can adaptively regulate the input impedance of the load converter for different source converters. Therefore, the load converter can be designed as a standard module connected to any source converters. Additionally, since the AIIR method only modifies the input impedance of the load converter in a small range of frequencies, the original dynamic performance of the load converter is well maintained. Finally, the AIIR control strategy has been experimentally verified on two cascaded systems.

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