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Voltage Synchronisation Techniques for Grid-Connected Power Converters

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Abstract

Standard synchronisation scheme for grid-connected power converters has been known to fail to correctly estimate the instantaneous phase angle of the grid voltages which are unbalanced and corrupted with harmonics. There are other advanced schemes which have been proposed to address this issue but a thorough comparison among the schemes is lacking. This paper presents a detailed review on five advanced grid voltage synchronisation schemes. A coherent investigation is performed to compare their merits and limitations considering a wide range of voltage distortions. This is verified through simulation and practical results.

1 Introduction

Grid synchronisation is one of the key issues for distributed power generation systems connected to the utility network through power electronic converters. It is also important for devices such as flexible AC transmission systems (FACTs), active power filters, and HVDC converters [1,2]. Among various methods, the synchronous reference frame phase-locked-loop (SRF-PLL), is widely known and the simplest. However, it is sensitive to grid voltage distortion and corruption by harmonics and cannot work for unbalanced voltages without additional filtering [3].

Practical systems involve various single phase loads with unequal loading of feeders, loads being continuously connected or disconnected, and loads which are nonlinear, unbalanced and distort the voltage at the point of common coupling (PCC). Accurate knowledge of phase and frequency of grid voltage under these conditions is hard to obtain but crucial for converter operation and control. Several new schemes have been reported to address the stated requirements and comparative studies of some of them have been carried out [4]. However analysis of their characteristics in terms of dynamic response speed and tracking precision, computational simplicity, capability in distortion rejection, and unbalanced robustness as a whole is lacking.

Five advanced synchronisation schemes are investigated in this paper including Decoupled Double Synchronous Reference Frame (DDSRF), Symmetrical Component Measurement using Energy Operator (EO), Double Second Order Generalised Integrator (DSOGI), Fourier Series + Moving Average (FS+MVA) Comb Filter and Cascaded Delayed Signal Cancellation (CDSC). All these have been well-studied by either the researchers who introduced the schemes or those who have worked on these schemes for their applications [3,5-7]. In this paper, a coherent investigation is performed for these schemes and this leads to a comparative study which has been done according to the aforementioned criteria using both MATLAB-SIMULINK simulation results and practical on-line tests. For the latter all these methods are implemented using a microcontroller and tested on an emulated three-phase voltage source which can be distorted with harmonics and/or magnitudes made to be unbalanced.

2 General Principles in Voltage Synchronisation Schemes

Figure 1(a) shows an example system where the control of the power electronic converter is based on the phase angles of the voltages at the PCC nodes. The latter can be estimated using the SRF-PLL which is illustrated in Figure 1(b). This consists of two parts and the first implements the Clarke-Park transformation through which the synchronous-reference-frame based components for the measured PCC voltages are obtained. The second is the feedback based control system and for this case, a Proportional+Integral (P+I) controller is applied. To correctly achieve phase estimation, these two parts are working in unison where the controller output is taken as the feedback signal for the Clarke-Park transformation while the in-quadrature component from the transformation is used as the input for the controller.

In advanced voltage synchronisation schemes as mentioned in Section 1, the fundamental positive sequence components (PSCs) of the PCC voltages are instead extracted before the phase estimation is performed. This extraction technique employed by each of these schemes is the main feature which makes it distinctive from the others. Nevertheless, there is a similarity among them as some may apply the same reference frame on which fundamental PSCs are extracted. For example, EO and FS+MVA are based on the instantaneous three phase voltages (A-B-C) while others follow the two dimensional reference frames; DSOGI and CDSC are based on the stationary reference frame ($\alpha\beta$) and DDSRF follows the synchronous reference frame (dq). The implementation details of each scheme will be discussed in the following sections.

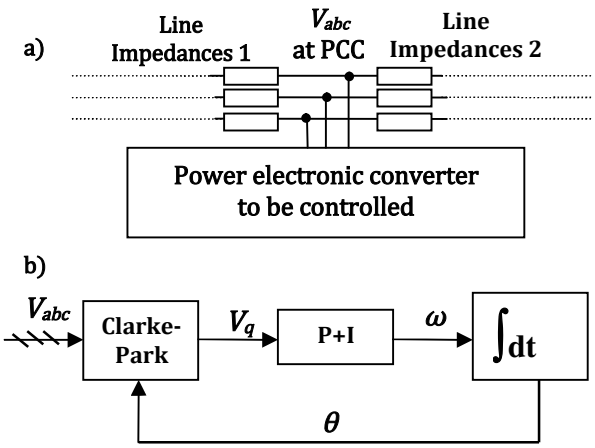

Figure 1: (a) Definition of PCC and (b) Block diagram for SRF-PLL synchronisation scheme

3 Comparative Study on Various Advanced Voltage Synchronisation Schemes

This section reviews the principles of the advanced synchronisation schemes mentioned in Section 1. Each of these schemes is simulated in MATLAB-SIMULINK and when various distortions are introduced in the three-phase PCC voltages, their performances are analysed.

3.1. Decoupled Double Synchronous Reference Frame (DDSRF)

DDSRF is the extension of the standard SRF-PLL and has been developed mainly for unbalanced grid voltage synchronisation [3]. Its distinctive feature is the two Clarke-Park transformations employed to obtain the *dq* components of the PCC voltages as shown in Figure 2. Respectively they are based on two reference frames, one rotating directly and the other oppositely with the grid frequency. Thus two voltage vectors are generated and they are respectively expressed as

$$\mathbf{V}_{dq}^{+} = V^{+}\begin{bmatrix}\cos(\theta^{+})\\ \sin(\theta^{+})\end{bmatrix} + V^{-}\cos(\theta^{-})\begin{bmatrix}-\cos(2\omega t)\\ \sin(2\omega t)\end{bmatrix} + V^{-}\sin(\theta^{-})\begin{bmatrix}\sin(2\omega t)\\ \cos(2\omega t)\end{bmatrix} \quad (1)$$

and

$$\mathbf{V}_{dq}^{-} = V^{-}\begin{bmatrix}\cos(\theta^{-})\\ \sin(\theta^{-})\end{bmatrix} + V^{+}\cos(\theta^{+})\begin{bmatrix}-\cos(2\omega t)\\ -\sin(2\omega t)\end{bmatrix} + V^{+}\sin(\theta^{+})\begin{bmatrix}-\sin(2\omega t)\\ \cos(2\omega t)\end{bmatrix} \quad (2)$$

where V^{+} and V^{-} are magnitudes of positive and negative sequence components for an unbalanced voltage set while θ^{+} and θ^{-} are their phase angles.

DDSRF is actually an improvement to its predecessor through adding a decoupling network, indicated by the shaded blocks in Figure 2. This is aimed to simultaneously cancel the AC components present in Equations (1) and (2). Together with the low pass filters which are used to stabilise the overall closed loop system, the PSCs in the *dq* form are extracted before the phase angle of PCC voltages can be estimated using a P+I controller similar to that of the SRF-PLL.

As shown in Figure 3, this scheme only works well when the PCC voltages become unbalanced. The estimated phase angle becomes erroneous when the scheme is applied to voltages with high order harmonic components.

3.2. Symmetrical Component Measurement using Energy Operator (EO)

EO is aimed at achieving separate synchronisation for individual PCC phase voltages. This is done firstly by applying the energy operator method proposed by [5] to estimate the instantaneous amplitude and angle of each phase

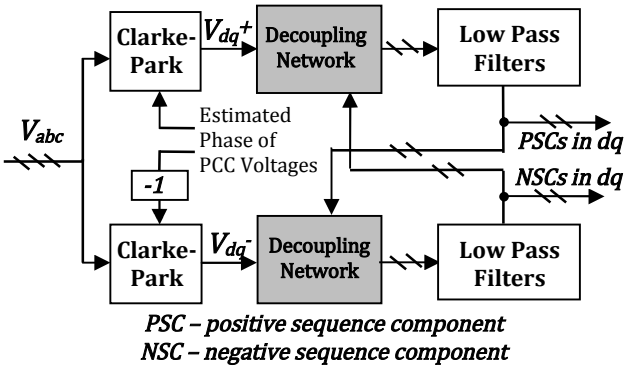

Figure 2: Configuration of a DDSRF Scheme

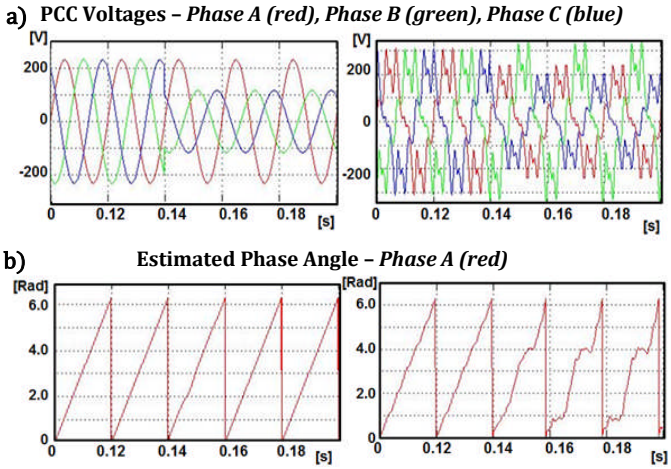

Figure 3: MATLAB-SIMULINK simulation results for DDSRF based synchronisation scheme:
(a) Three phase PCC voltages which are unbalanced and corrupted with harmonics
(b) Estimated phase angle of Phase A PCC voltage

voltage which respectively can be expressed as

$$V_x = \frac{\sqrt{v_x - \left(v_x^-\right)\left(v_x^+\right)}}{\sin(\alpha)} \quad (3)$$

and $$\theta_x = \sin^{-1}\left(\frac{v_x}{V_x}\right) \quad (4)$$

where v_x is the instantaneous measurement for any of phase voltages while v_x^- and v_x^+ are their delayed versions respectively by α and $(2\pi - \alpha)$ radians.

After applying Equations (3) and (4) to all three phase PCC voltages (v_a, v_b, v_c), the instantaneous values for the PSCs can be calculated using Fortescue's operator; these are in the *A-B-C* domain. Phase estimation based on SRF-PLL is then applied using the extracted PSCs.

As shown in Figure 4, the scheme is suitable for three phase voltages which are no longer 120° apart from each other. Nevertheless, the estimated phase becomes highly inaccurate when the phase voltages become corrupted with harmonics.

3.3 Double Second Order Generalised Integrator (DSOGI)

Based on the adaptive notch filtering technique, DSOGI based technique estimates the phase angle through the extracted PSCs in the $\alpha\beta$ domain which are in general written as

$$\mathbf{V}_{\alpha\beta}^+ = \begin{bmatrix} v_\alpha^+ \\ v_\beta^+ \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & q \\ -q & 1 \end{bmatrix}\mathbf{V}_{\alpha\beta} \quad (5)$$

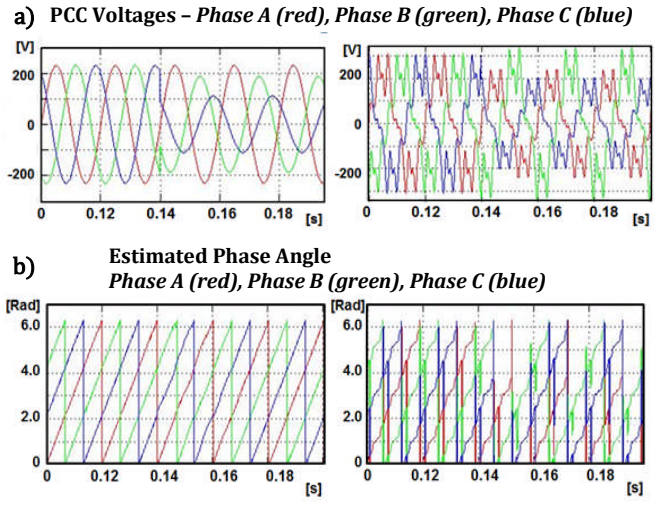

Figure 4: MATLAB-SIMULINK simulation results for EO based synchronisation scheme:
(a) Three phase PCC voltages which are unbalanced, corrupted with harmonics, and are not 120° apart from each other.
(b) Estimated phase angles of three-phase PCC voltages

where $\mathbf{V}_{\alpha\beta}$ is the stationary reference frame based voltage vector for the measured three phase PCC voltages while $q = e^{-j\pi/2}$ is a delay operator by 90°. The latter is produced by applying a second order generalised integration (SOGI) on each element in $\mathbf{V}_{\alpha\beta}$. The general configuration of a DSOGI is illustrated in Figure 5(a) while the operation in Equation (5) is illustrated within the shaded box. The detailed structure of a SOGI is shown in Figure 5(b).

The estimated phase is then directly calculated using the following expression

$$\theta = \tan^{-1}\left(\frac{v_\alpha^+}{v_\beta^+}\right) \quad (6)$$

It is worthy to note that the information about the grid frequency (instead of phase) is required by the overall DSOGI network. To generate this information, frequency locked-loop

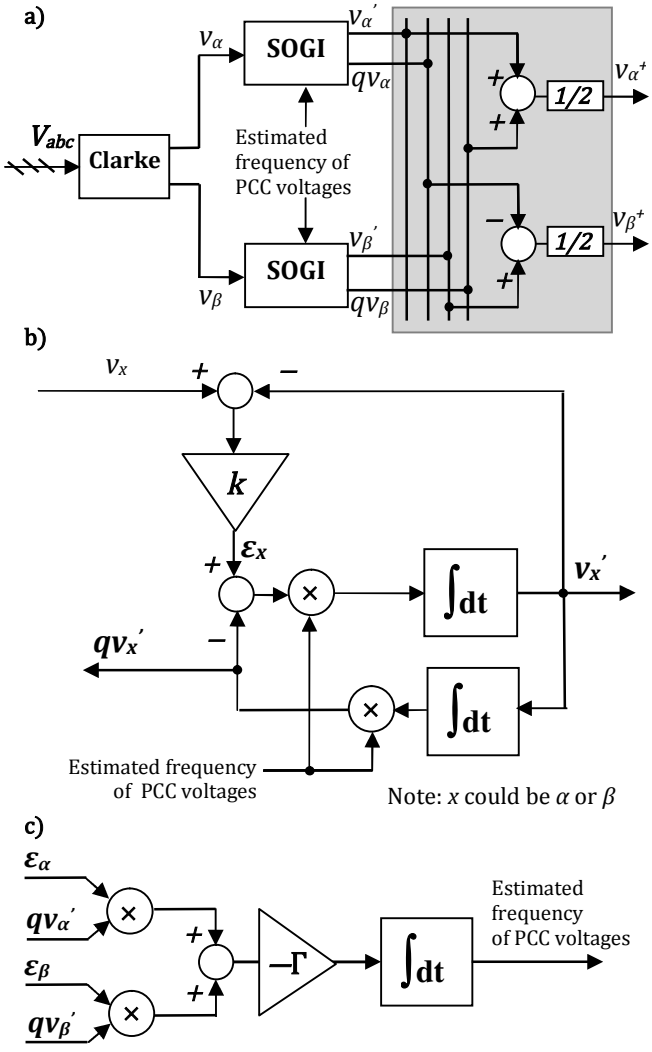

Figure 5: Overall of implementation DSOGI synchronisation scheme:
(a) Configuration of DSOGI
(b) Detailed structure of SOGI operator
(c) Block diagram of FLL for frequency estimation

(FLL) is introduced as shown in Figure 5(c), instead of using SRF-PLL. This is due to the fact that the grid frequency is relatively constant while the grid phase is continuously changing over time, thus the control for FLL would be easier to design.

From Figure 6, it can be observed that the estimated phase is relatively correct even when the PCC voltages become corrupted with harmonics and contain DC component.

3.4 Fourier Series + Moving Average (FS + MA)

Recently, the authors in [6] applied the digital approach of a moving average comb filter (MVA) in processing the PCC voltage measurements to obtain the fundamental PSCs, which will be used to compute the phase angle directly. These are achieved firstly by multiplying each phase voltage with two sinusoidal signals, ($v_m = \sin(\omega_1 t + \theta_o)$ and $v_n = \cos(\omega_1 t + \theta_o)$), which are orthogonal to each other. They are also function of the fundamental frequency (ω_1) and have an arbitrary phase shift of θ_o.

For example when a phase voltage (v_x) contains a fundamental and odd non-triplen harmonics (ω_1, ω_5, ω_7, ω_{11}, ….), the above described products may be written as

$$v_x \sin(\omega_1 t + \theta_o) = \frac{1}{2}[A_1 \cos(\theta_{i1} - \theta_0) + A_1 \cos(2\omega_1 t + \theta_{i1} + \theta_0) + A_3 \cos(2\omega_1 t + \theta_{i3} - \theta_0) \ldots.] \quad (7)$$

and

$$v_x \cos(\omega_1 t + \theta_o) = \frac{1}{2}[A_1 \sin(\theta_{i1} - \theta_0) + A_1 \sin(2\omega_1 t + \theta_{i1} + \theta_0) + A_3 \sin(2\omega_1 t + \theta_{i3} - \theta_0) \ldots.] \quad (8)$$

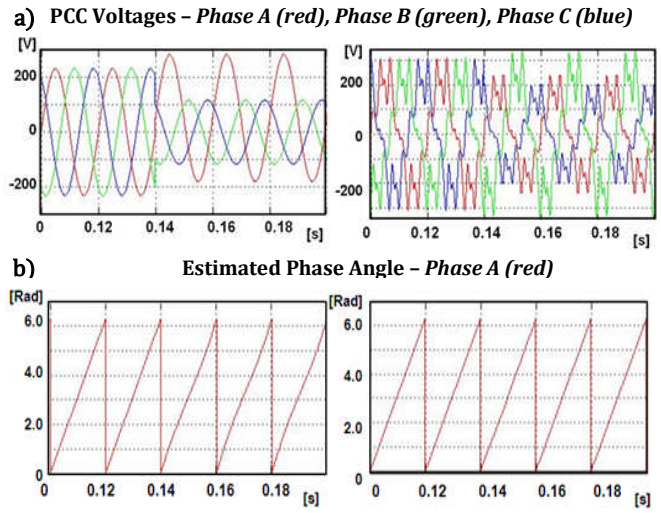

Figure 6: MATLAB-SIMULINK simulation results for DSOGI based synchronisation scheme:
(a) Three phase PCC voltages which are unbalanced, corrupted with DC component and high order harmonics
(b) Estimated phase angle of Phase A PCC voltage

where A_n is the magnitude and θ_{in} is the phase angles for n-th order harmonic of v_x. Each of the products is sent through an MVA filter whose discrete time transfer function is written as

$$H(z) = \frac{2}{n}\frac{1 - z^{-n}}{1 - z^{-1}} \quad (9)$$

where $n = \dfrac{sampling\ \ frequency}{\omega_1}$ and therefore, Equations (7) and (8) contain only the DC component. The filtered output are respectively multiplied by ($2 \times v_m$) and ($2 \times v_n$) before summing them together to extract the fundamental component as $v_{\sin x} = A_1 \sin(\omega_1 t + \theta_{i1})$. Similar process can be carried out to obtain $v_{\cos x} = A_1 \cos(\omega_1 t + \theta_{i1})$ through swapping around the orthogonal signals. The two resulting signals are then used to obtain phase angle of the fundamental PSCs.

Besides having the capability of synchronising individual PCC phase voltages, this scheme works well when they become distorted, unbalanced and are no longer 120° degrees from each other, as shown in Figure 7.

3.5 Cascaded Delayed Signal Cancellation (CDSC)

Similar to FS+MA, CDSC is aimed to remove a group of harmonics from the measured PCC voltage signals before the fundamental PSCs and the phase are estimated. However unlike FS+MA, the harmonics that can be removed do not have to be, for example, only the multiple of even harmonics. This is so because the harmonics removal is actually performed by CDSC operators which are based on the following expression [7]:

$$DSC_n = \frac{1}{2}\left[v_x(t) + v_x\left(t - \frac{T}{n}\right)\right] \quad (10)$$

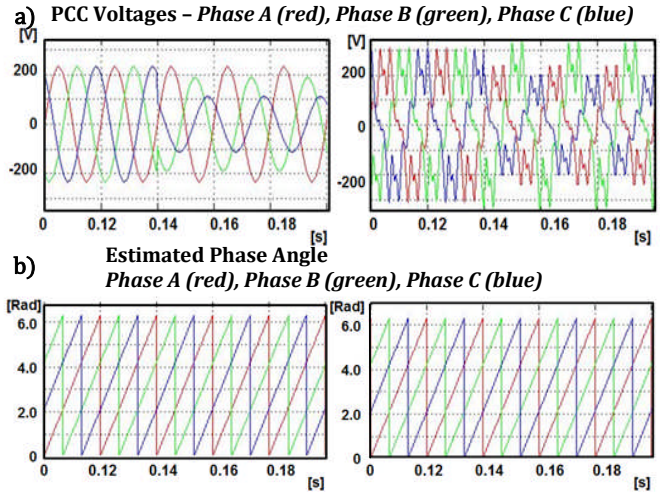

Figure 7: MATLAB-SIMULINK simulation results for FS+MA based synchronisation scheme:
(a) Three phase PCC voltages which are unbalanced, corrupted with harmonics, and are not 120° apart from each other.
(b) Estimated phase angles of three-phase PCC voltages

where $v_x(t)$ is the instantaneous measured signal and T/n is the time delay with $1/T$ = grid frequency and n is a positive integer. For a value of n, several harmonics can be removed simultaneously and if the measured signal is processed in several stages by DSC_n operations with different n values, a combination of several harmonics can be eliminated.

Thus, this scheme could have quite a number of variants depending on the combination of DSC_n operators. One example of CDSC scheme is shown in Figure 8 and the combination of DSC_n operators, having n = 2, 4, 8 and 16, is able to remove almost all even and odd harmonics up to 30th order. The output of the last DSC_n operator will mostly contain the fundamental PSCs. Note that SRF-PLL is needed employed for phase angle estimation. The harmonic elimination takes places in $\alpha\beta$ domain rather than in dq, and this potentially prevents the stability margin of the SRF-PLL being degraded owing to the dynamical characteristics of the DSC_n operators. In addition, the information about the frequency is continuously needed and this can be readily obtained from SRF-PLL as shown in Figure 8.

As shown in Figure 9, this scheme also works well with PCC voltages having different voltage distortions.

3.6 Further Discussions

The capabilities of all the schemes discussed above, for synchronising PCC voltages of different distortions are listed in Table 1. Based on the implementation of the SIMULINK models used in the above investigations, the complexity of each scheme is summarized in Table 2. In addition, each scheme has been tested with a step response to evaluate its transient performance and the settling time of the response is listed under the last column of Table 2.

It can be observed that EO and FS+MA allow independent synchronisation of individual phase voltages but EO only works well with unbalanced voltages, whether they are still 120^o apart from each other or not. FS+MA has the fastest response among all the schemes investigated so far. Application of DDSRF is limited only to unbalanced conditions and DSOGI does not work well for all distortion types. Nevertheless DDSRF and DSOGI can be extended to increase their functions but this improvement requires larger system architecture, as demonstrated in [3].

CDSC and FS+MA appear to be desirable synchronisation techniques as they work well with voltages which are unbalanced and corrupted with harmonics and DC offsets. However, the design for the latter has only considered the removal of odd and non-triplen harmonics. Its design has to be extended also to remove other harmonics (for example, even and triplens). These have been considered in the current CDSC design investigated in this paper though it involves a more complicated system architecture. Simpler variant of CDSC, which only removes odd harmonics, can be implemented and potentially, the settling time through this approach can be halved [7].

4 Practical Verifications

To verify the above schemes practically, a Java SE GUI based three phase source emulator was created through which a set of analogue three phase voltages can be generated with the desired magnitudes of the fundamental and harmonic components. The voltages can also be made unbalanced. These analogue signals are then measured by a dsPIC30F4011 microcontroller which is used to extract the fundamental PSCs of the analogue signals and obtain their phase angle.

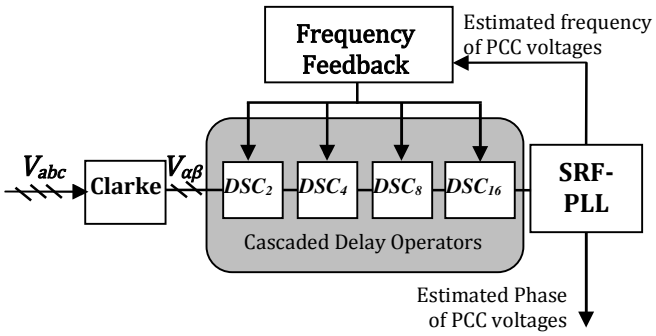

Figure 8: Synchronisation scheme based on CDSC having DSC_2, DSC_4, DSC_8 and DSC_{16} operators.

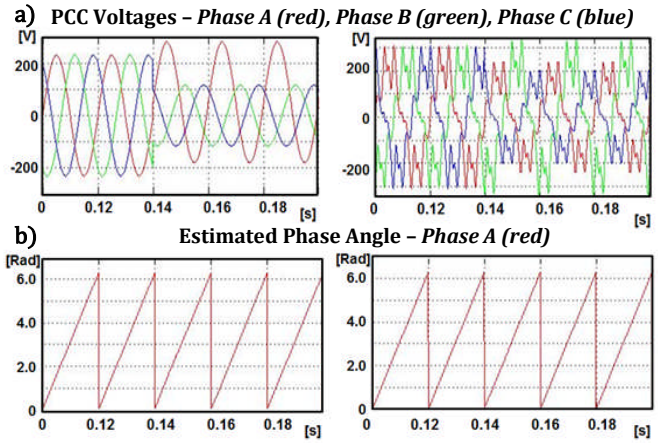

Figure 9: MATLAB-SIMULINK simulation results for CDSC based synchronisation scheme:
(a) Three phase PCC voltages which are unbalanced, corrupted with DC component and high order harmonics
(b) Estimated phase angle of Phase A PCC voltage

Schemes	Ability to synchronise			
	Unbalanced Voltage	Unbalanced Voltage & Phase Displaced	Unbalanced Voltage & With Harmonics	Unbalanced Voltage & With DC Offset
DDSRF	Yes	No	No	No
EO	Yes	Yes	No	No
DSOGI	Yes	Yes	No	No
FS+MA	Yes	Yes	Yes	Yes
CDSC	Yes	Yes	Yes	Yes

Table 1: Ability of various schemes for synchronisation

Type of frame	Method	Number of Operators				Settling Time (in cycle)
		Arithmetic	Cos & Sin	Buffer	Filter	
A-B-C frame	EO	28	8	10	0	1.5 cycle
	FS+MA	33	6	6	6	≈ 0.3 cycle
dq frame	DDSRF	17	8	0	4	0.5 cycle
αβ frame	CDSC	76	16	8	0	1 cycle
	DSOGI	22	0	0	0	1.5 cycle

Table 2: Complexity of the schemes and their transient performance

For each of the schemes discussed in Section 3, the algorithms implemented in the microcontroller are real-time processed and the synchronisation signals are generated. In this paper, two sets of synchronisation results are presented. As shown in Figures 10(a) and (b), the first set is based on the standard SRF-PLL where the performance can be used as reference for other advanced schemes. As expected, there is a continuous oscillation in the estimated phase angle when the voltages are either unbalanced or corrupted with harmonics. Using the CDSC scheme, the second set of results is obtained and shown in Figures 11(a) and (b) where one can observe that the estimated phase angle of the fundamental PSC is accurate and experiences no oscillation.

5 Conclusions

A detailed review and a coherent comparison for PCC voltages synchronisation have been performed on five different schemes. Several operating conditions under which the voltages may experience have been considered and these include unbalance in their amplitudes, corruptions with high order harmonics and DC components. In addition, all schemes have been tested if they could be used to independently synchronise PCC voltages and those which are no longer 120° apart from each other.

All these schemes have been tested and the comparison has been verified through simulation and practical results. The common trait in these schemes is that they all aim to extract the fundamental PSCs from the measured PCC voltages signals. The phases of the latter are estimated either directly from the extracted PSCs or by applying the standard SRF-PLL based synchronisation scheme. What distinguishes one scheme from the other is the technique based on which the PSCs are extracted. Nevertheless, the designs of some schemes assume that certain voltage distortions are not present in the measured signals. Every scheme has its own merits and its application should depend on the severity of the distortions and the resources available (i.e. hardware or software) for the implementation. Regardless of the latter, CDSC offers a relatively definitive solution for synchronisation of PCC voltages having the above-mentioned distortions.

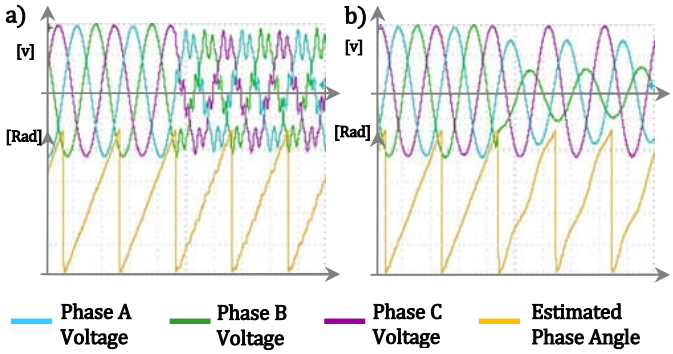

Figure 10: Practical verification results for SRF-PLL scheme:
(a) Three phase voltages corrupted with harmonics and the estimated phase angle
(b) Unbalanced three phase voltages & estimated phase

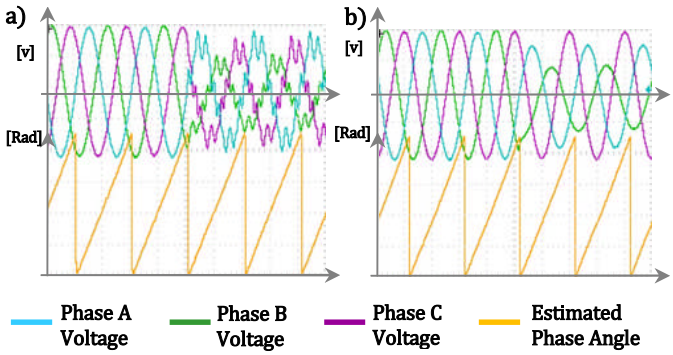

Figure 11: Practical verification results for CDSC scheme:
(a) Three phase voltages which are unbalanced & corrupted with harmonics, and the estimated phase angle
(b) Unbalanced three phase voltages & estimated phase

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