Analysis and Control of Dual-Output $LCLC$ Resonant Converters With Significant Leakage Inductance

Christopher M. Bingham, Yong Ann Ang, Martin P. Foster, and David A. Stone

***Abstract*—The analysis, design and control of fourth-order $LCLC$ voltage-output series-parallel resonant converters for the provision of multiple regulated outputs, is described. Specifically, state-variable concepts are developed to establish operating mode boundaries with which to describe the internal behavior and the impact of output leakage inductance. The resulting models are compared with those obtained from SPICE simulations and measurements from a prototype power supply under closed loop control to verify the analysis, modeling, and control predictions.**

***Index Terms*—Series-parallel resonant converters (SPRCs).**

I. Introduction

TO-DATE, several approaches have been explored to address cross-regulation, complexity, and overall circuit performance issues of multioutput converters, the solutions being divided into three distinct categories. The first regulates a single primary output using closed-loop feedback, with the auxiliary outputs being semi-regulated and, therefore, subject to cross-regulation error. The second category achieves precise post-regulation of each output by using either linear regulators or hard-switched dc–dc converters. However, such circuits are rarely used in practice due to cost constraints. The third category is specific to applications which require only two regulated outputs, as is commonly found in signal processing and microprocessor based systems. They avoid the need for post-regulation by utilizing two closed-loop feedback configurations. A third-order LLC converter [1], [2] with two independently controlled outputs has been previously reported in [1]. However, optimum performance characteristics were not forthcoming, primarily due to the significant complexity associated with the highly nonlinear behavior between the various outputs as a function of load. Nevertheless, it is a solution that broadly falls within this third category that is the subject of this paper. Specifically, dual-output resonant $LCLC$ converters [3]–[8], are considered, with control of each output being achieved by switching the power devices asymmetrically over each half switching cycle using a combination of pulsewidth modulation (PWM) and frequency control.

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II. Dual O/P $LCLC$-SPRC Model

A half-bridge $LCLC$-SPRC with two outputs is shown in Fig. 1(a). To achieve zero-voltage switching, the converter is assumed to operate on the negative gradient of the input-output frequency characteristic, above the primary resonant peak. When operating in this region, the resulting waveforms can be sub-divided into three distinct modes per half cycle viz. M1, M2, and M3, depicted in Fig. 1(c)–(e).

In the analysis that follows in this section it is assumed that 1) output filter capacitors C_{f1} and C_{f2} are infinite in value and therefore $V_{\rm out1}$ and $V_{\rm out2}$ are ripple free, 2) the resonant circuit input current (also shown in Fig. 1(b) as $i_{\rm in}$) can be conveniently represented as a sinusoid owing to the band-pass filter characteristics of the tank circuit, 3) all switches (inc. diodes) are ideal and thus commutate instantaneously and possess zero on-state voltage drop, 4) the transformer leakages are negligible (i.e., $L_{lp} = L_{ls} = 0$), and 5) the parallel resonant capacitors are equal in value.

Circuit Mode M1 $(t_0 \leq t < t_1)$. At the start of M1, SW2 is turned off at t_0 and SW1 turned on. The series inductor current, i_{Ls} [shown as $i_{\rm in}$ in Fig. 1(b)], is negative and flows through the internal diode of SW1, thereby facilitating ZVS of SW1. Also during this period, i_{Ls} allows D2 to conduct and transfer energy to support $V_{\rm out2}$, while the voltage on C_{p2} is clamped to $V_{\rm out2}$. All the rectifier current, therefore, flows to the load. At the end of M1, the rectifier current i_{R2} has decayed to zero, and both the high side and low side diodes, and the output filter, are effectively decoupled from the resonant tank.

Circuit Mode M2 $(t_1 \leq t < t_2)$. Here, the series resonant inductor current i_{Ls} becomes positive. Since SW1 is turned on during M1, current flow is now through SW1. Initial conditions for this mode are that $i_{Ls}(t_1) = 0$ and $v_{cp2}(t_1) = V_{\rm out2}$. The inductor current i_{Ls} and parallel resonant capacitor voltages take on a sinusoidal characteristic. Since the outputs are effectively disconnected from the tank, both C_{p1} and C_{p2} contribute to resonant behavior. Both rectifier currents are zero, and the converter outputs are in an 'idle' state, with energy being supplied solely by the charge on the filter capacitors. By initially neglecting the rectifier on-state voltage, and noting that the effective parallel resonant capacitance C_p is the sum of the parallel resonant capacitors C_{p1} and C_{p2}, v_{Cp1} during the capacitor charging period is described by

$$v_{Cp1}(t) = v_{Cp1}(t_1) + \frac{1}{C_p}\int_{t_1}^{t_2} \hat{i}_{\rm in}\sin(2\pi f_s t)dt \qquad (1)$$

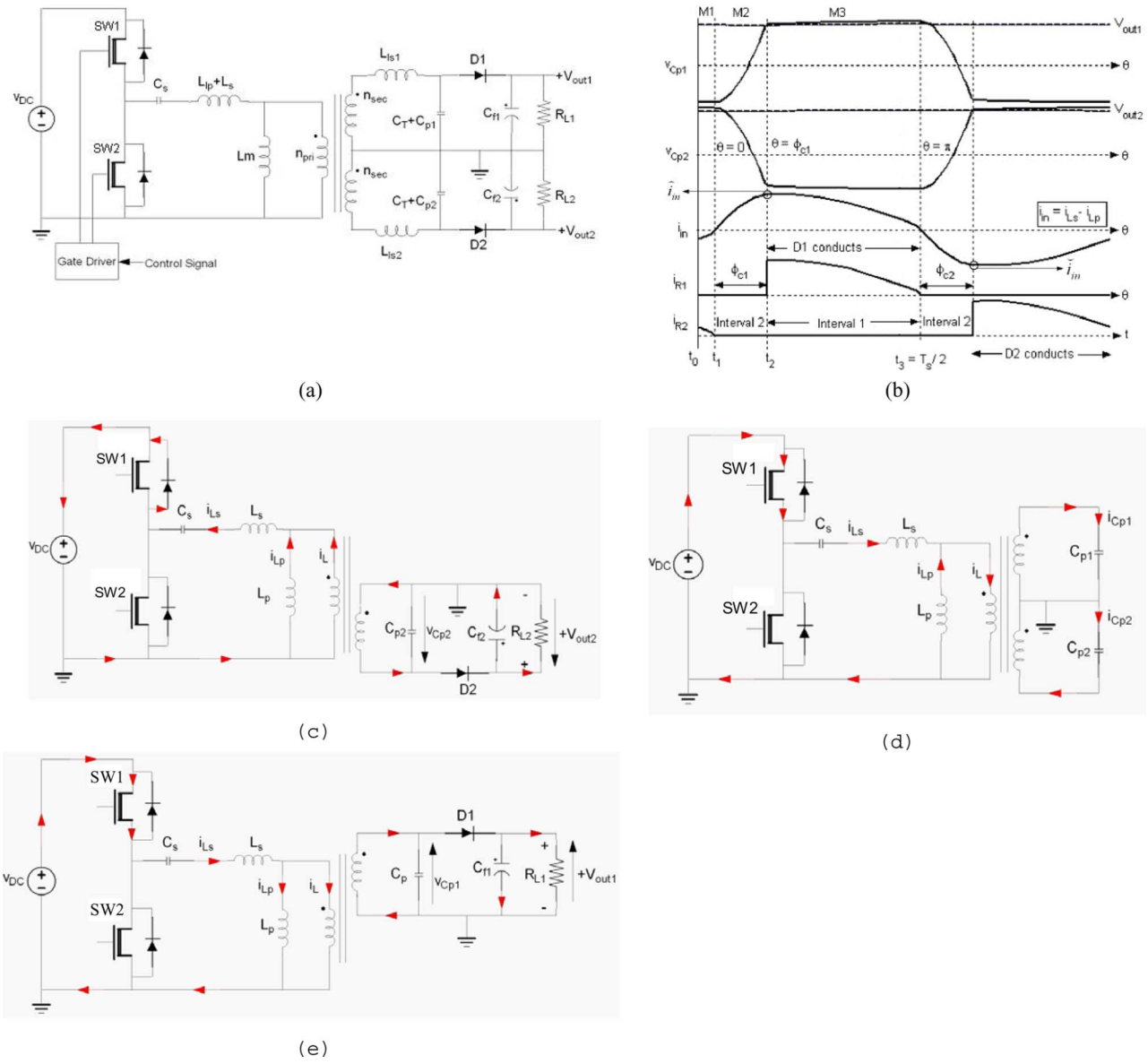

Fig. 1. Dual-load fourth-order resonant converter: (a) schematic, (b) typical operating waveforms, (c) M1, (d) M2, and (e) M3.

where $\hat{i}_{\text{in}} = -(i_{Ls} - i_{Lp})$. Evaluating (1) with initial conditions $v_R(t_1) = v_{Cp1}(t_1) = -V_{\text{out2}}$ yields

$$v_{Cp1}(t_2) = -V_{\text{out2}} + \hat{i}_{\text{in}} \times \frac{1 - \cos\left(2\pi f_s\left(t_2 - t_1\right)\right)}{2\pi f_s C_p}. \quad (2)$$

The boundary for the end of the capacitor charging period is $v_{Cp1}(t_2) = +V_{\text{out1}}$, which yields the rectifier nonconduction angle, ϕ_{c1}, associated with a positive polarity of current, i_R, through the high side rectifier

$$\begin{aligned} t_2 - t_1 &= \frac{1}{2\pi f_s} \times \cos^{-1}\left(\phi_{c1}\right) \\ \phi_{c1} &= \cos^{-1}\left(1 - \frac{2\pi f_s C_p v_{tot}}{\hat{i}_{\text{in}}}\right) \\ v_{tot} &= V_{\text{out1}} + V_{\text{out2}}. \end{aligned} \quad (3)$$

Circuit Mode M3 $(t_2 \le t < T_s/2)$. At $t = t_2$ D1 becomes forward biased, since $V_{cp1} \ge V_{\text{out1}}$ and D2 is still reverse biased. The rectifier diode current i_{R2} remains zero throughout the duration of M3, and D1 clamps the capacitor voltage v_{cp1} to $+V_{\text{out1}}$ until i_{Ls} decays to zero, at which time the second half cycle of operation commences.

For 50% duty-cycle excitation, the second half-cycle of operation is the mirror image of the first. However, for asymmetrical excitation, the output rectifier diode (D2) nonconduction angle, associated with the series resonant inductor current being of negative polarity, is given by

$$\phi_{c2} = \cos^{-1}\left(1 - \frac{2\pi f_s C_p v_{tot}}{\breve{i}_{\text{in}}}\right) \quad (4)$$

where $\breve{i}_{\text{in}} = i_{Ls} - i_{Lp}$. The voltage, v_{cp1}, across the parallel resonant capacitor can, therefore, be expressed as a function of the angle θ [see Fig. 1(b)], see (5), shown at the bottom of the next page.

Under steady-state conditions, the mean output current i_{out1}, flowing through D1 towards the output filter and load, can be determined from the mean current flowing through the rectifier when it is of positive polarity. Since this occurs during the interval $\phi_{c1} \leq \theta < \pi$, i_{out1} is given by

$$i_{\text{out1}} = \frac{1}{2\pi} \times \int_{\phi_{c1}}^{\pi} \hat{i}_{\text{in}} \sin(\theta) d\theta. \tag{6}$$

Substituting (3) into (6) and evaluating the integral provides the solution for i_{out1}

$$i_{\text{out1}} = \frac{\hat{i}_{\text{in}}}{2\pi} \times (1 + \cos(\phi_{c1})) = \frac{\hat{i}_{\text{in}} - \pi f_s C_p v_{tot}}{\pi}. \tag{7}$$

Simple mathematical manipulation of (7) then gives the corresponding rectifier nonconduction angle ϕ_{c1}

$$\phi_{c1} = \cos^{-1}\left(\frac{\pi i_{\text{out1}} - \pi f_s C_p v_{tot}}{\pi i_{\text{out1}} + \pi f_s C_p v_{tot}}\right) \tag{8}$$

where V_{out1} is determined by assuming the output filter capacitance C_f is sufficiently large to impart negligible output voltage ripple. In this case

$$\begin{aligned} V_{\text{out1}} &= i_{\text{out1}} R_{L1} = \frac{\hat{i}_{\text{in}} R_{L1}}{2\pi} \times (1 + \cos(\phi_{c1})) \\ &= \frac{R_{L1}\left(\hat{i}_{\text{in}} - \pi f_s C_p v_{tot}\right)}{\pi} \\ &= \frac{R_{L1}}{\pi} \times \frac{\hat{i}_{\text{in}} - \pi f_s C_p V_{\text{out2}}}{1 + R_L f_s C_p}. \end{aligned} \tag{9}$$

Equations (6)–(9) can be further manipulated to provide the complementary D2 nonconduction angle, ϕ_{c2}, and the output current, i_{out2}, and output voltage V_{out2}, as follows:

$$\begin{aligned} i_{\text{out2}} &= \frac{\breve{i}_{\text{in}}}{2\pi} \times (1 + \cos(\phi_{c2})) \\ V_{\text{out2}} &= \frac{R_{L2}}{\pi} \times \frac{\hat{i}_{\text{in}} - \pi f_s C_p V_{\text{out1}}}{1 + R_L f_s C_p}. \end{aligned} \tag{10}$$

III. State-Variable Analysis

In this section a state-variable model of the dual-output converter is derived which is suitable for both steady-state and transient analysis of the converter. To commence the analysis the dynamics of the converters are separated into "fast" and "slow" sub-systems, with their interaction related by a set of coupling equations. The fast sub-system is considered to describe the dynamics of the resonant tank and power switches

$$\begin{aligned} \frac{dv_{Cs}}{dt} &= \frac{i_{Ls}}{C_s}, \quad \frac{di_{Ls}}{dt} = \frac{V_{\text{in}} - v_{Cs} - v_{Lp}}{L_s} \\ \frac{di_{Lp}}{dt} &= \frac{v_{Lp}}{L_p} \\ \frac{dv_{Cp1}}{dt} &= \frac{i_{Ls} - i_{Lp} - i_{R1} - i_{Cp2} - i_{R2}}{C_{p1}} \\ \frac{dv_{Cp2}}{dt} &= \frac{i_{Ls} - i_{Lp} - i_{R2} - i_{Cp1} - i_{R1}}{C_{p2}} \end{aligned} \tag{11}$$

with the slow sub-system describing the output filter dynamics

$$\frac{dv_{cf1}}{dt} = \frac{i_{R1}}{C_{f1}} - \frac{v_{cf1}}{C_{f1}R_{L1}}, \quad \frac{dv_{cf2}}{dt} = \frac{i_{R2}}{C_{f2}} - \frac{v_{cf2}}{C_{f2}R_{L2}}. \tag{12}$$

As discussed, during interval $t_1 \rightarrow t_2$ [see Fig. 1(b) and (d)] v_{cp1} is clamped to v_{cf1} during the positive half-cycle, and conversely, to $-v_{cf2}$ during the negative half-cycle, due to the action of the diodes. By noting that there will be negligible current flowing through C_p during these periods, the rectifier input voltage is dependent on the direction of the current leaving the resonant tank inductances, i.e., $i_L = i_{Ls} - i_{Lp}$. The relevant coupling terms are, therefore, obtained by equating voltages at either side of the rectifier for each respective half-cycle

$$\begin{aligned} v_{Cp1} &= \text{sgn}(i_L)(V_{\text{out1}} + v_{\text{diode}}) = \text{sgn}(i_L)(v_{cf1} + v_{\text{diode}}) \\ v_{Cp2} &= \text{sgn}(i_L)(V_{\text{out2}} + v_{\text{diode}}) = \text{sgn}(i_L)(v_{cf2} + v_{\text{diode}}). \end{aligned} \tag{13}$$

Assuming a constant rectifier voltage drop, (12) can be manipulated to give

$$\frac{dv_{Cp1}}{dt} = \text{sgn}(i_L)\frac{dv_{cf1}}{dt}, \quad \frac{dv_{Cp2}}{dt} = \text{sgn}(i_L)\frac{dv_{cf2}}{dt}. \tag{14}$$

Considering the rectifier current, i_{R2}, to be zero during the positive half-cycle of the parallel capacitor voltage, the rectifier current i_{R1}, is given from

$$\begin{aligned} &\frac{i_L - i_{R1} - i_{Cp2} - i_{R2}}{C_{p1}} \\ &\quad = \text{sgn}(i_L)\left(\frac{i_{R1}}{C_{f1}} - \frac{v_{cf1}}{C_{f1}R_{L1}}\right) \\ &\therefore i_{R1} = \frac{C_{p1}C_{f1}}{\text{sgn}(i_L)C_{p1} + C_{f1}} \\ &\qquad \times \left(\frac{i_L - i_{Cp2} - i_{R2}}{C_{p1}} + \frac{\text{sgn}(i_L)v_{cf1}}{C_{f1}R_{L1}}\right). \end{aligned} \tag{15}$$

$$v_{Cp1}(\theta) = \begin{cases} -V_{\text{out2}} + \frac{\hat{i}_{\text{in}}}{2\pi f_s C_p} \times (1 - \cos(\theta)), & \text{for } \theta = 0K\phi_{c1} \\ +V_{\text{out1}}, & \text{for } \theta = \phi_{c1}\lambda\pi \\ V_{\text{out1}} - \frac{\hat{i}_{\text{in}}}{2\pi f_s C_p} \times (1 - \cos(\theta)), & \text{for } \theta = \pi K\pi + \phi_{c2} \\ -V_{\text{out2}}, & \text{for } \theta = \pi + \phi_{c2}K2\pi \end{cases} \tag{5}$$

This leads to the following coupling equations which describe the rectifier currents within each half of a switching cycle, see (16), shown at the bottom of the page.

Notably, the voltage across L_p can be considered a reflection of the voltages across C_{p1} and C_{p2}, and the state vector for the parallel inductor current in the fast sub-system [see (11)] simplifies to $v_{Lp} = v_{Cp}$. The state-variable equations for the parallel resonant capacitor voltage (11) can be simplified to

$$\frac{dv_{Cp1}}{dt} = \frac{i_{Ls} - i_{Lp} - i_R}{2C_{p1}}, \quad \frac{dv_{Cp2}}{dt} = \frac{i_{Ls} - i_{Lp} - i_R}{2C_{p2}}. \tag{17}$$

The complete state-variable model of the dual load converter is, therefore, given by

$$\dot{\mathbf{x}} = \begin{bmatrix} 0^{3\times3} & \mathrm{A}_1 & 0^{2\times3} \\ \mathrm{A}_2 & 0^{2\times2} & 0^{2\times2} \\ 0^{2\times3} & 0^{2\times2} & \mathbf{A}_3 \end{bmatrix} \mathbf{x} + \mathbf{B} \tag{18}$$

where

$$\mathbf{x} = \begin{bmatrix} v_{Cp1} & v_{Cp2} & v_{Cs} & i_{Lp} & i_{Ls} & v_{Cf1} & v_{Cf2} \end{bmatrix}^{\mathrm{T}}$$

$$\mathrm{A}_1 = \begin{bmatrix} -\frac{1}{2C_{p1}} & \frac{1}{2C_{p1}} \\ -\frac{1}{2C_{p2}} & \frac{1}{2C_{p2}} \\ 0 & \frac{1}{C_s} \end{bmatrix}, \quad \mathrm{A}_2 = \begin{bmatrix} \frac{1}{L_p} & 0 & 0 \\ -\frac{1}{L_s} & 0 & -\frac{1}{L_s} \end{bmatrix}$$

$$\mathrm{A}_3 = \begin{bmatrix} -\frac{1}{C_f R_{L1}} & 0 \\ 0 & -\frac{1}{C_{f2} R_{L2}} \end{bmatrix}$$

$$\mathrm{B} = \begin{bmatrix} -\frac{i_R}{2C_{p1}} & -\frac{i_R}{2C_{p2}} & 0^{1\times2} & \frac{V_{\mathrm{in}}}{L_s} & \frac{i_{R1}}{C_{f1}} & \frac{i_{R2}}{C_{f2}} \end{bmatrix}^{\mathrm{T}}. \tag{19}$$

By way of example, the aforementioned model has been implemented in the Matlab/Simulink simulation environment and employed to generate steady-state control to output voltage response for the candidate converter given in Table I with a 30 V dc-link voltage. A plot of the resulting steady-state output voltage characteristics of the converter, V_{out1} and V_{out2}, as a function of switching frequency and duty-cycle ratio is given in Fig. 2. It is evident that for operation above resonance, the sum of the output voltages applied to the loads increases as the operating frequency tends to the effective resonant frequency, for fixed values of duty-cycle ratio. Furthermore, for a 50% duty-cycle, giving symmetric square-wave excitation of the tank, the converter delivers identical voltages to both the high side and low side outputs, for a fixed operating frequency, as expected. For a given operating frequency, a decrease in the duty-cycle ratio, from 50%, is seen to deliver more energy from the resonant tank to energize output V_{out1}, thereby yielding a correspondingly higher output voltage and power, and vice-versa. It is, therefore, clear that for balanced loads,

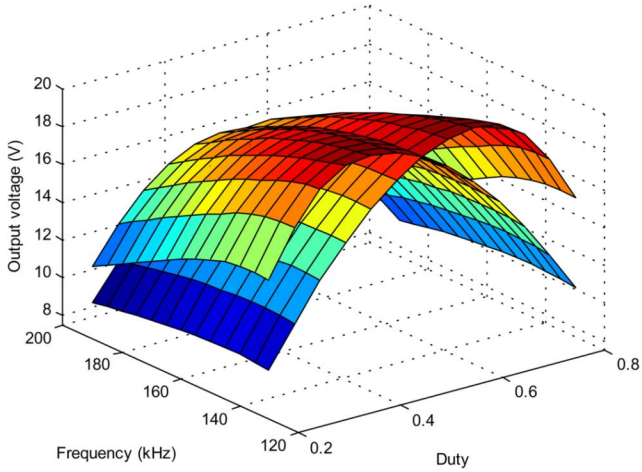

Fig. 2. Variation of output voltage distribution with switching frequency and duty-cycle ratio.

TABLE I
CONVERTER MODEL PARAMETERS

Parameters	*Value*
Characteristic impedance (Ω)	2.5
Resonant inductance ratio, L_n	0.01
Resonant frequency, f_o (kHz)	130
Resonant capacitance ratio, C_n	0.03
Series load quality factor, Q_{op1}	6

where the characteristic impedance $Z_0 = \omega_0 L_s$, $\omega_{op} = \frac{R_{load}}{Q_{op1} L_s}$, $C_s = \frac{1}{L_s}\left(\frac{Q_{op1} L_s}{R_{load}}\right)^2$, $R_L = 2R_{load}$

the voltage and power distribution to each output can be independently influenced by a suitable choice of duty ratio and switching frequency.

Fig. 3(a) also shows the ratio of the two output voltages, as a function of duty and load quality factor, Q_{op1}. It can be seen that the slope of the characteristic is relatively independent of the quality factor, for high Q_{op1}, although the attainable difference between the output voltages is seen to be greater for low values of load quality factor. Hence, operation with a low Q_{op1} should be chosen to facilitate large output voltage differences, as opposed to the use of high Q_{op1} to facilitate sinusoidal tank currents and voltages.

Since it is instructive to show the impact of converter parameters on the attainable output voltage ratio, Fig. 3(b) demonstrates how the output voltage ratio varies, as a function of duty ratio, as the resonant capacitance ratio C_n is varied. It can be seen, in particular, that the slope of the characteristic is greater for low values of C_n. Hence, it is usual to choose a low value for C_n during the design phase. However, such a choice means the input-output voltage characteristic exhibits a reduced resonant peak, and consequently, the voltage boosting capability of the

$$i_{R1} = \begin{cases} \frac{C_{p1}C_{f1}}{\mathrm{sgn}(i_L)C_{p1}+C_{f1}} \left(\frac{i_L - i_{Cp2} - i_{R2}}{C_{p1}} + \frac{\mathrm{sgn}(i_L) v_{cf1}}{C_{f1} R_{L1}} \right), & \text{for } v_{Cp1} = V_{\mathrm{out1}} + v_{\mathrm{diode}} \\ 0, & \text{for } v_{Cp1} < V_{\mathrm{out1}} + v_{\mathrm{diode}} \end{cases}$$

$$i_{R2} = \begin{cases} \frac{C_{p2}C_{f2}}{\mathrm{sgn}(i_L)C_{p2}+C_{f2}} \left(\frac{i_L - i_{Cp1} - i_{R1}}{C_{p2}} + \frac{\mathrm{sgn}(i_L) v_{cf2}}{C_{f2} R_{L2}} \right), & \text{for } v_{Cp2} = V_{\mathrm{out2}} + v_{\mathrm{diode}} \\ 0, & \text{for } v_{Cp2} < V_{\mathrm{out2}} + v_{\mathrm{diode}} \end{cases}. \tag{16}$$

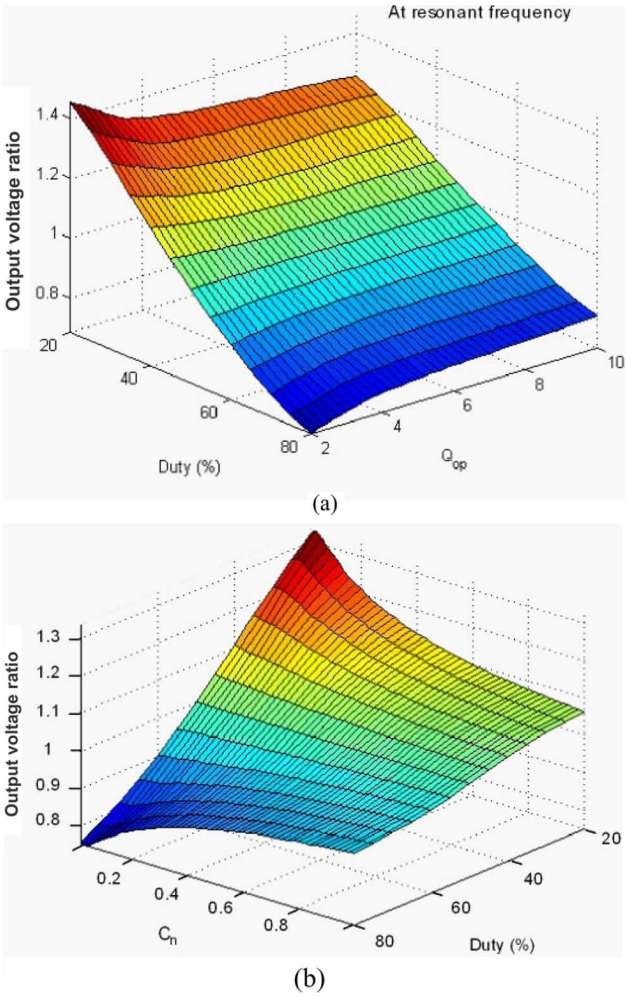

Fig. 3. Dual output converter characteristics as a function of (a) duty-cycle ratio and Q_{op1} as design parameters and (b) duty-cycle ratio and C_n as design parameters.

converter is limited [2], [9]–[13]. Furthermore, the input-output voltage conversion ratio at the effective resonant frequency of the tank, is consequently lower. Such converters, therefore, are more suitable for step-down dc–dc applications.

Again, by way of example, Fig. 4 shows the variation of the phase difference, $\Delta\beta_{\rm in}$, between the input voltage and input current for the converter whose parameters are given in Table I, with the normalized switching frequency $\omega_n = \omega_s/\omega_o$ (where $\omega_o = \sqrt{(L_s C_s)}$) and the input voltage duty-cycle ratio. It can be seen that, at frequencies less than the tank resonant frequency, the input impedance of the tank network $Z_{\rm in}$ is dominated by the tank capacitance. Hence, the fundamental component of the input switch current leads the input voltage, and the resonant tank presents a load which is effectively capacitive. This provides zero current switching (ZCS) for $\Delta\beta_{\rm in}$ <0. However, when the resonant converter is operated above resonance the tank effectively presents an inductive load to the power devices, and the switch current lags the switch voltage, thereby facilitating zero voltage switching (ZVS).

The boundary condition i.e., the minimum phase angle that provides ZVS needs to be determined to constrain the excitation of the converter. At the effective resonant frequency,

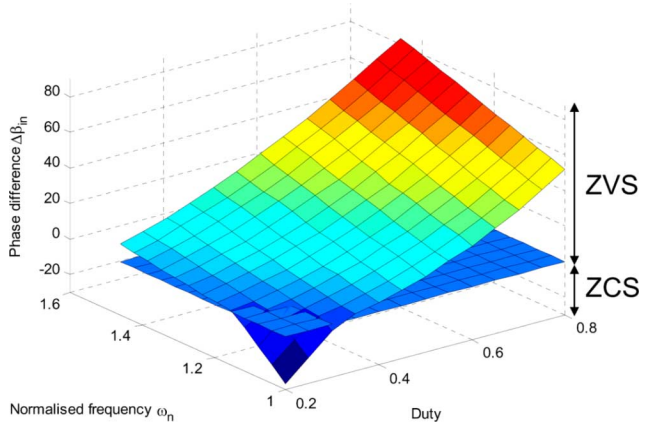

Fig. 4. Phase difference $\Delta\beta_{\rm in}$ versus normalized switching frequency and duty-cycle ratio.

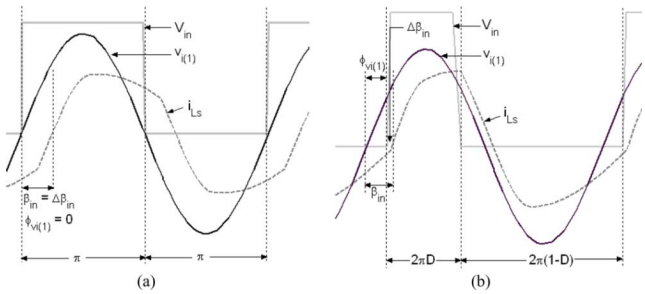

Fig. 5. Waveforms of input voltage $V_{\rm in}$, resonant circuit fundamental input voltage $v_{i(1)}$, and series inductor current i_{Ls} at (a) $D = 0.5(\Delta\beta_{\rm in} = \beta_{\rm in})$ and (b) $D = 0.3(\Delta\beta_{\rm in} < \beta_{\rm in})$.

under asymmetric square-wave input voltage excitation, the input voltage lags the fundamental of the input current, i.e., $\Delta\beta_{\rm in}$ <0 when the duty-cycle falls below 50%, as will be seen in Fig. 5. The condition for inductive mode conduction, under asymmetric conditions, can, therefore, be expressed as

$$\Delta\beta_{\rm in} = \beta_{\rm in} - \phi_{vi(1)} \geq 0 \tag{20}$$

where $\Delta\beta_{\rm in}$ is the phase angle between the actual square input voltage waveform and fundamental of the input current; $\beta_{\rm in}$ is the phase lag between the first harmonic of the input voltage and current; and $\phi_{vi(1)}$ is the phase of the fundamental frequency component of the input voltage, $v_i(1)$. It will be noted that $\beta_{\rm in} =$ 0 at resonance, and $\beta_{\rm in}$ >0 above resonance, which implies that the fundamental of the input voltage leads that of the current.

For asymmetric operation of the converter, the duties of SW1 and SW2 are now denoted, respectively, by D and 1-D, where D is the ratio of the turn-on period with respect to the switching period. Asymmetric switching therefore provides an asymmetrical voltage, $V_{\rm in}$, to excite the tank, of amplitude $v_{\rm dc}$:

$$V_{\rm in} = \begin{cases} v_{\rm DC} & \theta = 0 \ldots 2\pi{\rm D} \\ 0 & \theta = 2\pi{\rm D} \ldots 2\pi \end{cases}. \tag{21}$$

Assuming that only the fundamental component excites the resonant tank, and applying the relationship $\tan^{-1}(\cos(\theta)/\sin(\theta)) = \pi/2 + \theta$, the fundamental of the input voltage, $v_{\rm in}(1)$, and its phase angle, $\phi_{vi(1)}$ are given

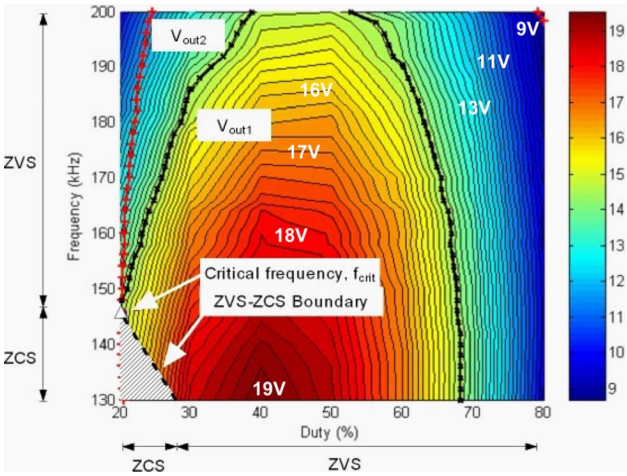

Fig. 6. Boundary condition and critical frequency to preserve ZVS.

by

$$v_{i(1)} = \frac{2v_{\mathrm{DC}}}{\pi}\sqrt{1-\cos(2\pi \mathrm{D})} \times \sin\left(\omega t + \phi_{vi(1)}\right)$$
$$\phi_{vi(1)} = \frac{\pi}{2} - \pi \mathrm{D}. \tag{22}$$

The condition for inductive switching can now be re-written as $\beta_{\mathrm{in}} \geq \pi(0.5-\mathrm{D})$, which is obtained by increasing the switching frequency. However, this imparts higher circulating currents that increase conduction losses contributing to thermal problems. Increasing the switching frequency also compromises the ability of the converter to deliver large differences in the dual output voltages. Ideally, therefore, the converter should be operated at the minimum switching frequency, above resonance, that can achieve ZVS. The minimum frequency which is allowed is referred to as the critical frequency, f_{crit}. To preserve ZVS, as D is decreased, the required critical frequency moves away from the resonant frequency, as illustrated in Fig. 6.

IV. Impact of Output Leakage Inductance

Although resonant converters are often designed to operate at relatively high frequencies, typically in the 200–500 kHz range, designers must still consider the impact of low levels of leakage inductance on converter performance. This is particularly evident for converters with multiple outputs, where the presence of such effects significantly complicates the analysis, particularly when determining the state of the parallel resonant inductor current, i_{Lp}, since the voltage seen across L_p cannot be assumed to be directly related to v_{Cp}, as a result of the voltages across the leakage inductances, L_{ls1} and L_{ls2} that are inherently present in the transformer. To predict how L_{ls1} and L_{ls2} will affect the operation of the converter, the model must be augmented with v_{Lp} to allow a solution for i_{Lp}. Once again, the converter can be partitioned into fast and slow sub-systems, Fig. 7 showing a model of the resonant converter "fast" sub-system. While the rectifier is omitted in the state-variable representation, its influence on the fast sub-system is accommodated through the addition of current sources, as shown in Fig. 7. This step is justified by noting that the interaction between the fast and slow sub-systems is solely based on coupling equations consisting of

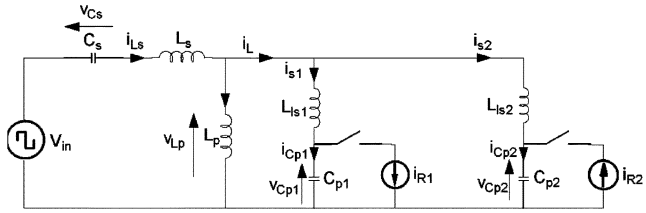

Fig. 7. State-variable representation of the fast sub-system.

TABLE II
Prototype Dual Output Converter Component Values

Parameter	Value
DC link input voltage, v_{DC} (V)	15
Series resonant inductances, L_s (μH)	0.85
Series resonant capacitances, C_s (μF)	1.5
High side parallel resonant capacitances, C_{p1} (μF)	0.116
Low side parallel resonant capacitances, C_{p2} (μF)	0.116
Load resistance, R_L (Ω)	5
Filter capacitance, C_f (μF)	100
Magnetising inductance, L_m (μH)	109
Transformer turns ratio	1
Transformer output leakage inductance, L_{ls} (μH)	0.1
Transformer primary leakage inductance, L_{lp} (μH)	0.7

the characteristics of the rectifier output currents i_{R1} and i_{R2}. The slow sub-system describes the behavior of the high side and low side rectifier outputs and the capacitive output filters and loads, v_{Cp1} and v_{Cp2} being considered to be the inputs to the high side and low side output sub-systems, respectively. The current sources i_{R1} and i_{R2}, represent the respective currents that flow into the filter capacitors during the rectifier conduction periods [Interval 1 in Fig. 1(b)]. These are necessary to replenish each filter capacitor's stored energy that is dissipated during the diode nonconduction periods [Interval 2 in Fig. 1(b)].

The dynamics of the fast sub-system, therefore, consist of a set of state-variables whose value at time $t = t_0$, together with the input for all $t > t_0$, completely determines the behavior of the system for any time $t > t_0$. An observable canonical state-space realization is, therefore, considered, as it allows the impact of parasitic elements to be readily included in the formulation, albeit at the expense of losing some of the physical significance of the state-variables. The equivalent circuit in Fig. 7 is analyzed by considering each voltage and current source independently and using the principal of superposition to obtain the effective dynamic description for i_{Lp}

$$\frac{di_{Lp}}{dt} = \frac{v_{Lp}}{L_p} = \frac{v_{Lp\_vi} + v_{Lp\_iR1} + v_{Lp\_iR2}}{L_p} = \frac{y_1 + y_2 - y_3}{L_p} \tag{23}$$

$$\begin{aligned} \dot{x}_1 &= s\mathrm{A}_o\mathrm{x}_1 + \mathrm{B}_{o1}V_{\mathrm{in}} \quad & y_1 &= v_{Lp\_vi} = C_o\mathrm{x}_1 + \mathrm{D}_{o1}V_{\mathrm{in}} \\ \dot{x}_2 &= \mathrm{A}_o\mathrm{x}_2 + \mathrm{B}_{o2}i_{R2} \quad & y_2 &= v_{Lp\_iR1} = C_o\mathrm{x}_2 + \mathrm{D}_{o2}i_{R2} \\ \dot{x}_3 &= \mathrm{A}_o\mathrm{x}_3 + \mathrm{B}_{o2}i_{R2} \quad & y_3 &= v_{Lp\_iR2} = C_o\mathrm{x}_3 + \mathrm{D}_{o3}i_{R2} \end{aligned} \tag{24}$$

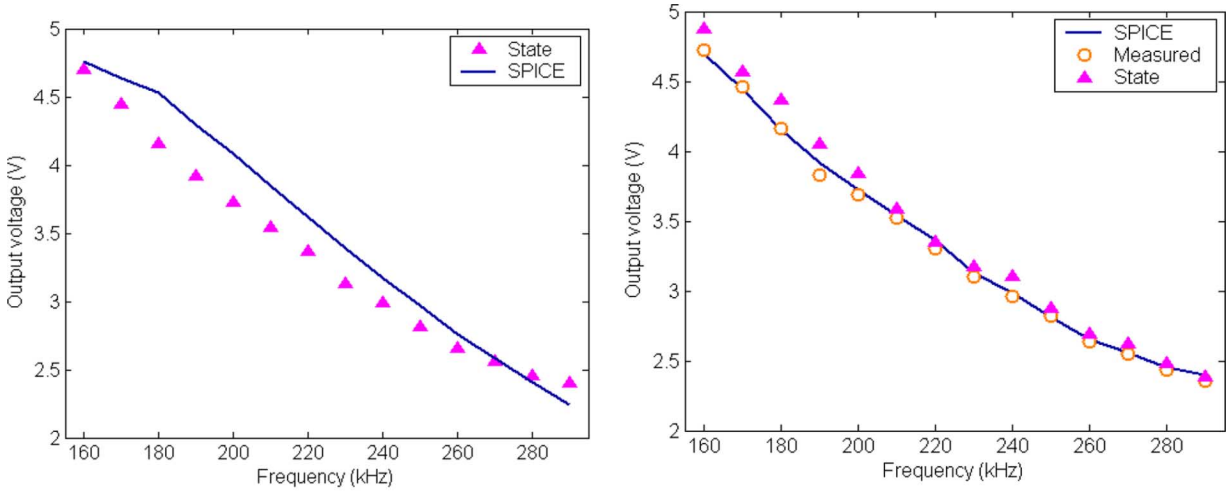

Fig. 8. Output voltage versus switching frequency: (a) without leakage and (b) with leakage included in state-variable model.

where

$$A_o = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & -\frac{a_{13}}{a_{10}} \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -\frac{a_{12}}{a_{10}} \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & -\frac{a_{11}}{a_{10}} \\ 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

$$B_{c1} = \begin{bmatrix} -\frac{b_{10}}{a_{10}} \times \frac{a_{13}}{a_{10}} \\ 0 \\ -\frac{b_{10}}{a_{10}} \times \frac{a_{12}}{a_{10}} + \frac{b_{11}}{a_{10}} \\ 0 \\ -\frac{b_{10}}{a_{10}} \times \frac{a_{11}}{a_{10}} + \frac{b_{12}}{a_{10}} \\ 0 \end{bmatrix}; \quad B_{c2} = \begin{bmatrix} \frac{b_{22}}{a_{10}} \\ 0 \\ \frac{b_{21}}{a_{10}} \\ 0 \\ \frac{b_{20}}{a_{10}} \\ 0 \end{bmatrix};$$

$$B_{c3} = -B_{c2} \quad C_o = [0^{5\times 1} \quad 1]; \quad D_{c1} = [1]$$

$$D_{c2} = D_{c3} = [0]$$

$$b_{10} = L_p L_{ls1} L_{ls2} \quad b_{11} = \frac{L_p L_{ls1}}{C_{p2}} + \frac{L_p L_{ls2}}{C_{p1}}$$

$$b_{12} = \frac{L_p}{C_{p1} C_{p2}}$$

$$b_{20} = L_s L_p L_{ls2} \quad b_{21} = \frac{L_p L_{ls2}}{C_s} + \frac{L_s L_p}{C_{p2}}$$

$$b_{22} = \frac{L_s}{C_s C_{p2}}$$

$$a_{10} = L_p L_{ls1} L_{ls2} + L_s L_p L_{ls2} + L_s L_p L_{ls1} + L_s L_p L_{ls2}$$

$$a_{11} = \frac{L_s L_{ls1}}{C_{p2}} + \frac{L_s L_{ls1}}{C_{p1}} + \frac{L_s L_p}{C_{p2}} + \frac{L_s L_p}{C_{p1}} + \frac{L_{ls1} L_{ls2}}{C_s} + \frac{L_p L_{ls2}}{C_s} + \frac{L_p L_{ls1}}{C_s} + \frac{L_p L_{ls1}}{C_{p2}} + \frac{L_p L_{ls2}}{C_{p1}}$$

$$a_{12} = \frac{L_s}{C_{p1} C_{p2}} + \frac{L_{ls1}}{C_s C_{p2}} + \frac{L_{ls1}}{C_s C_{p1}} + \frac{L_p}{C_s C_{p2}} + \frac{L_p}{C_s C_{p1}} + \frac{L_p}{C_{p1} C_{p2}}$$

$$a_{13} = \frac{1}{C_s C_{p1} C_{p2}}.$$

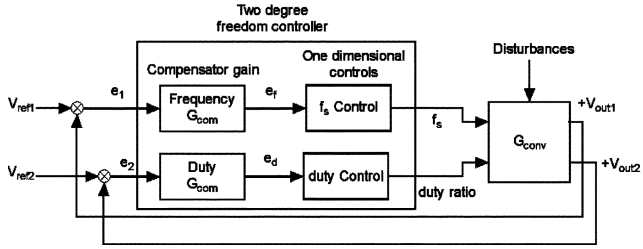

Fig. 9. Closed-loop control of the dual-load converter.

Fig. 10. Digital control of dual-output converter.

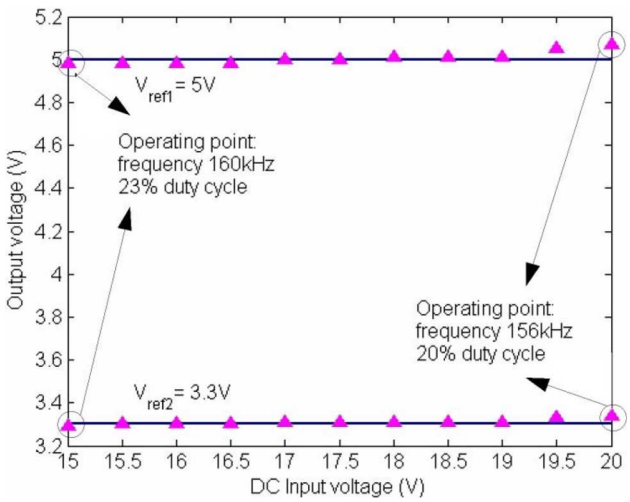

Fig. 11. Output voltage regulation versus input voltage.

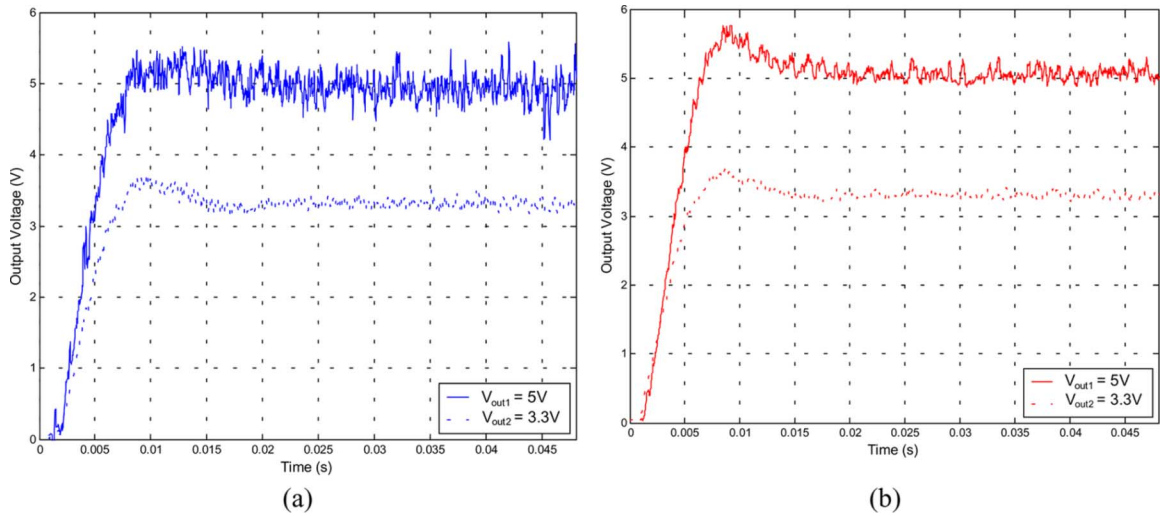

Fig. 12. Startup transient response for various dual output voltage ratios and dc-link input voltages (a) $v_{\rm DC} = 15$ V, $V_{\rm out1} = 5$ V, $V_{\rm out2} = 3.3$ V; (b) $v_{\rm dc} = 20$ V, $V_{\rm out1} = 5$ V, $V_{\rm out2} = 3.3$ V.

Adding the state vectors yields

$$\begin{aligned}\dot{x}_1+\dot{x}_2+\dot{x}_3 &= \mathrm{A}_o\left(\mathrm{x}_1+\mathrm{x}_2+\mathrm{x}_3\right)\\ &\quad+\left[\mathrm{B}_{o1}\quad \mathrm{B}_{o2}\quad \mathrm{B}_{o3}\right]\begin{bmatrix}V_{\rm in}\\ i_{R1}\\ i_{R2}\end{bmatrix}\\ y_1+y_3+y_3 &= v_{Lp\_vi}+v_{Lp\_iR1}+v_{Lp\_iR2}\\ &= C_o\left(\mathrm{x}_1+\mathrm{x}_2+\mathrm{x}_3\right)+\left[D_{o1}\quad 0\quad 0\right]\begin{bmatrix}V_{\rm in}\\ i_{R1}\\ i_{R2}\end{bmatrix}.\end{aligned} \tag{25}$$

Now, by defining

$$\begin{aligned}\mathrm{x} &= \mathrm{x}_1+\mathrm{x}_2+\mathrm{x}_3\\ y &= y_1+y_3+y_3=v_{Lp}\end{aligned}$$

the observable canonical state-space equation simplifies to

$$\begin{aligned}\dot{x} &= \mathrm{A}_o\left(\mathrm{x}_1+\mathrm{x}_2+\mathrm{x}_3\right)+\left[\mathrm{B}_{o1}\quad \mathrm{B}_{o2}\quad \mathrm{B}_{o3}\right]\begin{bmatrix}V_{\rm in}\\ i_{R1}\\ i_{R2}\end{bmatrix}\\ y=v_{Lp} &= C_o\left(\mathrm{x}_1+\mathrm{x}_2+\mathrm{x}_3\right)+\left[D_{o1}\quad 0\quad 0\right]\begin{bmatrix}V_{\rm in}\\ i_{R1}\\ i_{R2}\end{bmatrix}.\end{aligned} \tag{26}$$

Substituting the output state, together with the coupling equations, leads to a steady-state solution of the model. The fast and slow sub-system models can also be combined and used for implementation in simulation environments, e.g., MATLAB/SIMULINK.

V. Experimental Results

Measured results have been obtained on an experimental converter with a step-down capability, the measured component values being given in Table II. A ferrite core, 3F3, suitable for high frequency applications, was used for both the transformer core and the resonant inductor. Since the transformer leakage inductances are dependent on the winding arrangement, the secondaries were bifilar wound adjacent to the core, beneath the primary winding, so as to reduce secondary leakage flux.

The parallel resonant inductor is designed to be on the transformer primary side, such that L_p utilizes the magnetizing inductance, L_m, of the transformer. The effective series inductance comprises of the series inductor, L_s, and the primary leakage inductance, L_{lp}, and was measured as 1.55 μH. A comparison of the output voltage obtained from the state variable model, simulated to steady-state, with SPICE simulation results and measurements, is given in Fig. 8. As can clearly be seen from a comparison of Fig. 8(a) and (b), the correlation between the theoretical predictions and the experimental data is significantly improved when the effect of leakage inductance is incorporated within the model.

VI. Closed-Loop Control

The structure of the control methodology, which employs two decoupled feedback loops for independent control of frequency and duty-cycle ratio, is shown in Fig. 9. Parameters for the decoupled SISO controllers are chosen for good transient response and disturbance rejection. The digital compensator is tuned to respond quickly to variations of $V_{\rm out1}$ using frequency control, while the controller reacting to variations of $V_{\rm out2}$ (duty control) acts relatively slowly, thereby allowing an effective decoupling of the control loops, for simplicity. The prototype converter controller is shown in Fig. 10. The converter (see Table II for parameters) is required to provide regulated +5 V and +3.3 V outputs from a dc link input voltage in the range 15 to 20 V. Fig. 11 shows the steady-state error between the reference voltages, $V_{\rm ref1}$ and $V_{\rm ref2}$, and the resulting measured output voltages of the converter, over the specified range of dc link input voltages (15 to 20 V) with a 5Ω load connected to each output. It can be seen that the maximum regulation error for both outputs is $< 5\%$.

Finally, Fig. 12 shows the response of the converter resulting from transient startup conditions, for a range of applied input

voltages and dual output voltage ratios. It can be seen that the converter voltages converge rapidly to the reference values, with an initial overshoot of $\sim 10\%$, corresponding to an equivalent second-order damping ratio of $\zeta \approx 0.6$.

VII. Conclusion

The characteristics of dual-load, fourth-order $LCLC$ voltage-output resonant converters, have been explored. From the output voltage distribution derived from an example converter, the impact of the converter design parameters, and output leakage inductance, on the attainable output voltage ratio, has been investigated. A comparison of measurements from an experimental converter, capable of delivering 5 V and 3.3 V, with predictions from the derived state-variable model and SPICE simulations, shows that the state-variable model provides accurate predictions of output voltage under steady-state conditions. Moreover, a basic control scheme to allow reliable regulation of both outputs, has been realized, with steady-state measurements showing independent regulation using a combination of duty-cycle and frequency control, and good startup transient behavior on both outputs under a range of operating conditions.

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