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Design, fabrication and testing of Al/p-Si Schottky and pn junctions for radiation studies

E. Giulio Villani,^{a,*} Dengfeng Zhang,^{b,*} Adnan Malik,^c Trevor Vickey,^b Yebo Chen,^{d,e} Matthew G. Kurth,^d Peilian Liu,^d Hongbo Zhu,^h Thomas Koffas,^f Christoph Thomas Klein,^f Robert Vandusen,^g Rodney Aiton,^g Angela McCormick^g and Garry Tarr^g

^aSTFC Rutherford Appleton Laboratory Particle Physics Department, Harwell, Didcot, OX110QX, U.K.

^bDepartment of Physics and Astronomy, The University of Sheffield, Western Bank, Sheffield, S10 2TN, U.K.

^cSTFC Rutherford Appleton Laboratory, Innovations Technology Access Centre, Harwell, Didcot, OX110QX, U.K.

^dInstitute of High Energy Physics, Chinese Academy of Sciences, Beijing 100049, China

^eUniversity of Chinese Academy of Sciences, Beijing, 100049, China

^fDepartment of Physics, Carleton University, Ottawa, Ontario, K1S 5B6, Canada

^gDepartment of Electronics, Carleton University, Ottawa, Ontario, K1S 5B6, Canada

^hSchool of Physics, Zhejiang University, Hangzhou, 310058, China

E-mail: giulio.villani@stfc.ac.uk, dengfeng.zhang@cern.ch

ABSTRACT: Strip and pixels sensors, fabricated on high resistivity silicon substrate, normally of *p*-type, are used in detectors for High Energy Physics (HEP) typically in a hybrid detector assembly. Furthermore, and owing to their inherent advantages over hybrid sensors, Monolithic Active Pixel Sensors (MAPS) fabricated in CMOS technology have been increasingly implemented in HEP experiments. In all cases, their use in higher radiation areas (HL-LHC and beyond) will require options to improve their radiation hardness and time resolution. These aspects demand a deep understanding of their radiation damage and reliable models to predict their behaviours at high fluences. As a first step, we fabricated several Schottky and *n-on-p* diodes, to allow a comparison of results and provide a backup solution for test devices, on 6 or 4-inch *p*-type silicon wafers with 50 µm epitaxial thickness and of doping concentration as they are normally used in HEP detectors and CMOS MAPS devices. In this paper, details of the design and fabrication process, along with test results of the fabricated devices before irradiation, will be provided. Additional test results on irradiated devices will be provided in subsequent publications.

KEYWORDS: Radiation-hard detectors; Si microstrip and pad detectors; Solid state detectors

*Corresponding author.



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1 Introduction

In the High Energy Physics (HEP) community the topic of radiation hardness of detectors and related electronics has been and will continue to be, of crucial importance. The integrated luminosity of colliders has seen an almost constant increase by a factor of 10 per decade over the last 50 years [1]. As a consequence, the required radiation hardness of the sensors and electronics for the operation on the modern HEP detectors, like ATLAS and CMS on Large Hadron Collider (LHC) at CERN, has increased accordingly [2].

The technology usually implemented on HEP is hybrid detectors making use of high resistivity silicon [3], normally p -type. Another technology, which has received much attention owing to its inherent advantages over hybrid sensors, is the Monolithic Active Pixel Sensors (MAPS) fabricated in CMOS technology [4], which has already been applied in several HEP experiments [5–7]. Typically, the silicon used for the CMOS MAPS fabrication is p -type and consists of a medium-high resistivity epitaxially grown layer on top of a low doping substrate [8]. Significant performance degradation

is usually observed after fluences of $1 \times 10^{13} \text{ n}_{\text{eq}}/\text{cm}^2$ [2], as a result of bulk damage to the crystal structure. Despite various modifications having been proposed and implemented to improve radiation hardness [9, 10], a wider use of CMOS MAPS in higher radiation areas (e.g., the High-Luminosity LHC and beyond) will require an even deeper understanding of the mechanism of radiation bulk damage and mitigation methods, along with reliable models to predict their behaviors after high fluences. To investigate radiation bulk damage, we fabricated a number of Schottky and n -on- p junction diodes on p -type epitaxial silicon wafers, with doping concentrations typically used in CMOS MAPS devices. The purpose is to gain a deeper understanding of radiation damage in such structures with a view to develop reliable damage models that can be implemented in TCAD device simulators, like Synopsys TCAD [11].

In this paper, section 2 will give a description of the Schottky and pn junction diode device layouts. In section 3, a description of the fabrication process of the devices will be given. Section 4 will present test results, including Current-Voltage (IV), Capacitance-Voltage (CV), Charge Collection Efficiency (CCE) and defects obtained using the Deep-Level Transient Spectroscopy (DLTS) technique. Finally, in section 5, preliminary conclusions and a description of the next steps for this project will be given.

2 Schottky diode and pn junction design

In this research project several layouts of different device sizes were used. Bigger devices were designed to facilitate the measurements of capacitance and leakage current (CV and IV), whilst smaller devices, of enhanced signal-to-noise ratio (S/N) due to their smaller capacitance, were designed to investigate the charge collection efficiency (CCE) when injecting charge via minimum ionizing particle (MIP) or laser pulse. The Schottky diodes were fabricated on 6'' silicon wafers at Innovations Technology Access Centre (ITAC) at Rutherford Appleton Laboratory (RAL). The pn junctions were fabricated at the Carleton University MicroFabrication Facility (CUMFF) on 4'' silicon wafers sized down using laser dicing. And these silicon wafers were purchased from PlutoSemi [12].

2.1 Schottky diode device layout

The full wafer map along with the four device layouts are shown in figure 1. As the fabrication process of the Schottky diode is relatively simple, only two sets of 7'' masks were used, one for the metal and the other for the oxide. The different device layouts implemented differ in the cathode diameter and guard ring size as reported in table 1, there are four layouts in total (Layout 1-T1, Layout 2-T2, Layout 3-T3, Layout 4-T4). The layout 1 and layout 2 devices have a cathode of 2 mm and 1 mm diameter respectively, with a central hole in the metal to allow charge injection via a laser pulse for the charge collection investigation. The other two smaller devices have cathodes of 0.5 mm and 0.1 mm diameter respectively, and do not have a central hole. In all devices, the metal cathode slightly overlaps with the dielectric to reduce the effect of early breakdown [13].

2.2 pn junction device layout

The pn junction devices share the same geometry and layout as the Schottky diodes of figure 1, the only difference being in the guard ring implementation. The metal layer of the guard ring of the pn junction device either contacts the epitaxial layer directly (non-isolated guard ring/REG-GR) or is isolated from it by a layer of oxide (isolated guard ring/ISO-GR) to mitigate the formation of an inversion layer at

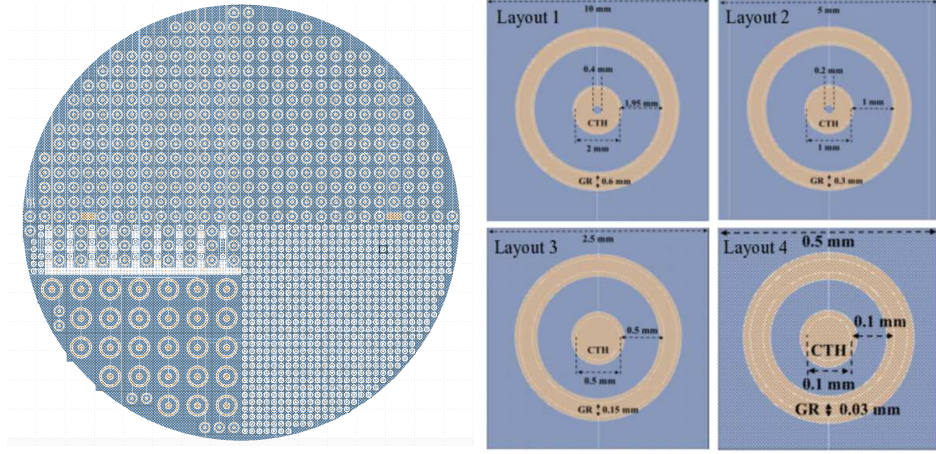


Figure 1. Left: the Schottky device map on the 6'' wafer. Right: four layouts of the Schottky diode devices.

Table 1. Layout details of Schottky devices. \varnothing : the diameter of the cathode or the central hole.

Size [mm]	Layout 1 (T1)	Layout 2 (T2)	Layout 3 (T3)	Layout 4 (T4)
Cathode \varnothing^*	2	1	0.5	0.1
Guard ring width	0.6	0.3	0.15	0.03
Central hole \varnothing	0.4	0.2	N/A	N/A

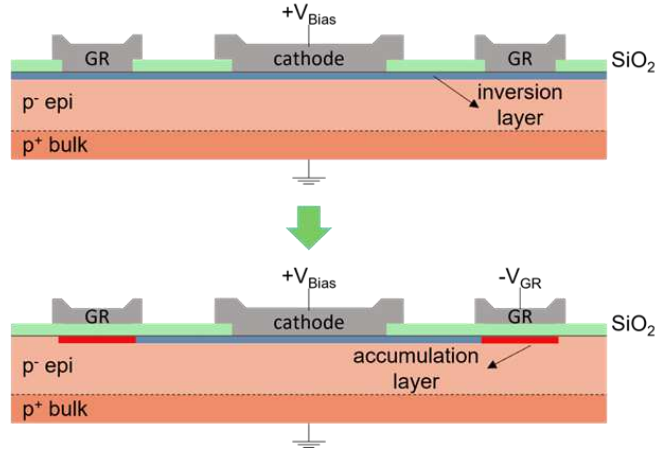


Figure 2. Schematic of the pn junction devices with REG-GR (top) and ISO-GR (bottom) guard ring.

the Si/SiO₂ interface. Cross-sections of the two types of the pn junction devices are shown in figure 2. An additional device flavour includes a p -stop implemented in the epitaxial layer under the guard ring.

3 Details of device fabrication

For this project, a total of 125 silicon wafers were purchased from PlutoSemi [12], consisting of 5 groups of 25 wafers each. All wafers have a 50 μ m thick epitaxial p -type layer. The 5 groups of wafers

have epitaxial resistivity of $1 \text{ k}\Omega/\text{cm}$, $100 \Omega/\text{cm}$, $10 \Omega/\text{cm}$, $1 \Omega/\text{cm}$ and $0.1 \Omega/\text{cm}$ respectively. The epitaxial layer is grown on a p -type substrate with a thickness of $575 \mu\text{m}$ and resistivity $0.005 \Omega/\text{cm}$. Subsets of the wafers were used for the fabrication of the Schottky diodes and pn junctions. The fabrication of the Schottky diode devices was performed by ITAC at Rutherford Appleton Laboratory, the pn junction devices were fabricated at CUMFF at Carleton University.

3.1 Fabrication of the Schottky diode devices

For the fabrication of Schottky diodes, only two masks were required. Full technical details of the fabrication, along with synopsis of the manufacturing process flow, are reported in appendix A. Examples of final fabricated devices and during the various stages of fabrication are shown in figures 3 and 4.

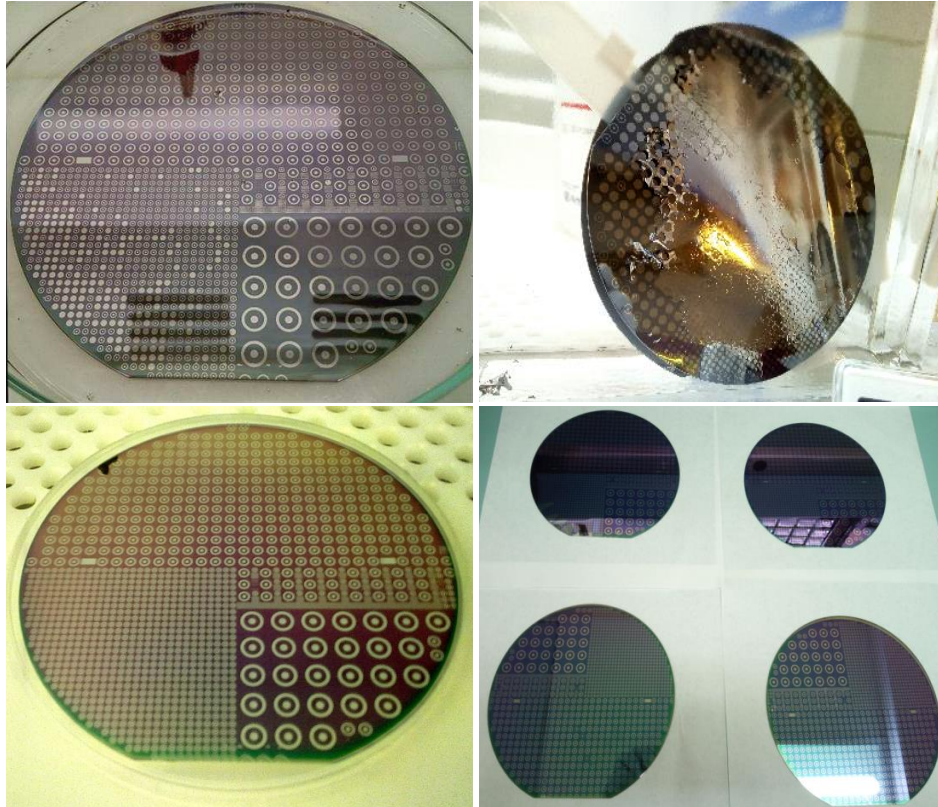


Figure 3. Top Left: wafer during resist ashing. Top Right: example of the lift-off process, showing the top metal peeling off the surface of the wafer. Bottom Left: the first completed wafer with Schottky diode devices on a high resistivity epi layer (doping concentration: 10^{13} cm^{-3}). Bottom Right: the first four completed wafers, two on high resistivity epi layer (doping concentration: 10^{13} cm^{-3}) and the other two on medium resistivity epi layer (doping concentration: $10^{14} - 10^{15} \text{ cm}^{-3}$).

3.2 Fabrication of the pn junction diode devices

The fabrication of pn junction diode required two masks of smaller size, as the fabrication took place on $4''$ wafers. The layout of the individual devices was the same as used for the Schottky diodes. Full technical details of the fabrication are reported in appendix A. Figure 5 shows an example of a processed pn junction wafer and diced device.

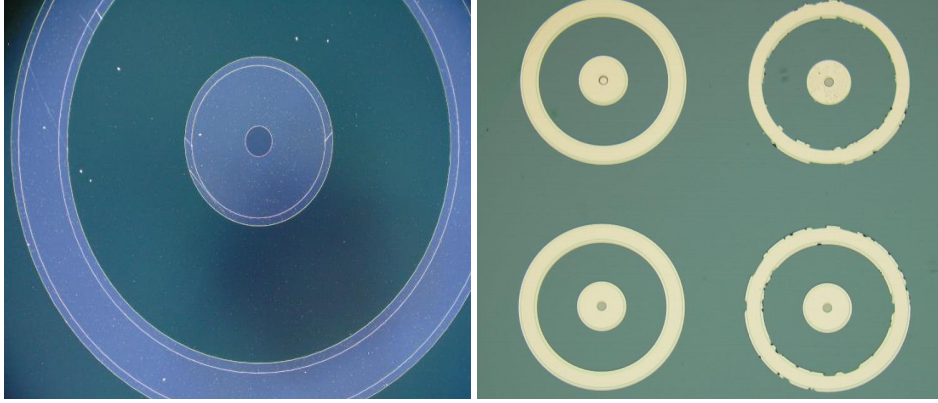


Figure 4. Left: microphotographs shows the fabricated Schottky diodes after the correct lift-off process. Right: results of non-uniform metal erosion following attempts to increase the process speed by increasing the bath temperature. The optimal temperature, which avoided the non-uniform rate of lift-off, was found to be 40 °C, as reported in appendix A.

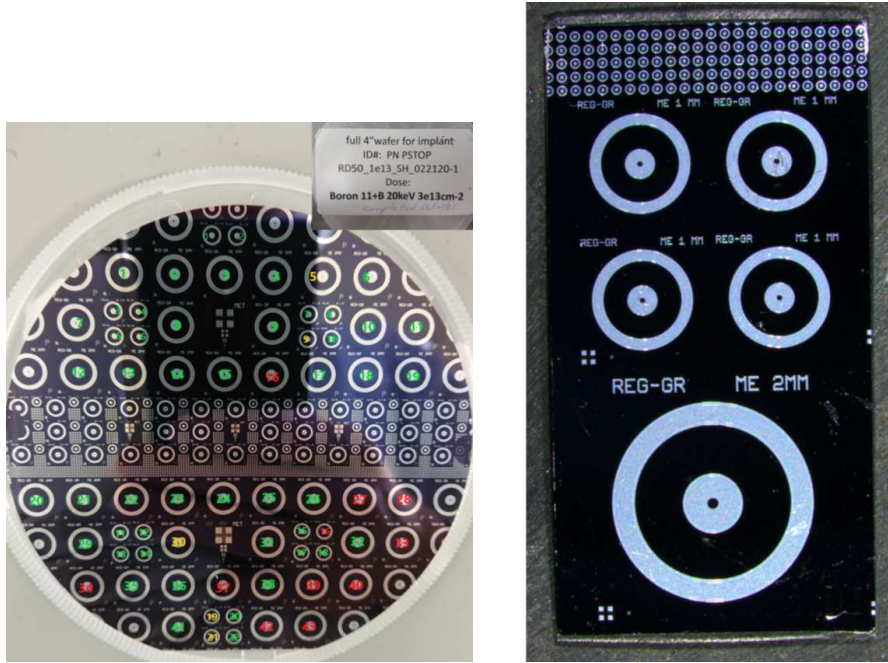


Figure 5. Left: processed pn junction wafer. Right: diced pn junction die.

4 Test results

The Current-Voltage (IV) and Capacitance-Voltage (CV) characteristics of the fabricated Schottky diodes and pn junctions were measured independently at Rutherford Appleton Laboratory (RAL), Oxford Physics Microstructure Detector (OPMD) laboratory and at Carleton University. The charge collection efficiencies were measured at RAL. Defect characteristics were measured at Carleton University using a Deep-Level Transient Spectroscopy (DLTS) setup.

4.1 Test setups

Test setups at RAL and OPMD. The setup for the measurement of IV and CV characteristics at RAL consists of a Keithley CS4200 Semiconductor analyzer coupled to a Micromanipulator probe station and Keithley Power interface 8020. The setup for the IV characteristics test at OPMD consists of a Keithley 4200A-SCS Semiconductor parameter analyzer coupled to a SEMIPROBE probe station (SA-12), Keithley interface 8020 and Keithley 2657A High Power System SourceMeter. The devices were tested at room temperature ($\sim 20^\circ\text{C}$) in a clean room both at RAL and OPMD. The charge collection efficiency was measured using a custom infrared (IR) laser injection system at RAL, built around a modified QuickLaze Trilite Laser. Figure 6 shows the whole setup consisting of a control PC, a LeCroy WaveRunner 6100A Oscilloscope, a Keithley 2410 HV Power Supply and a dark box where the laser header, stage, Coldbox, Amptek A250CF amplifier with a gain of 4 mV/fC are housed. The device under test was placed in the ColdBox, shown in figure 7, which is supplied with dry air and uses a chiller together with a Peltier element to adjust the temperature and humidity. The lowest temperature used for the test is -20°C , with relative humidity controlled down to 0.1%. The IR laser beam ($\lambda = 1064\text{ nm}$) is shaped, via electrically controlled collimators, to a rectangle of $\sim 5\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ and the beam energy was set to $23.44 \pm 2.2\text{ pJ}$. A custom-written LabVIEW program was developed to perform the full automatic tests and 1-D and 2-D scans of the DUT.

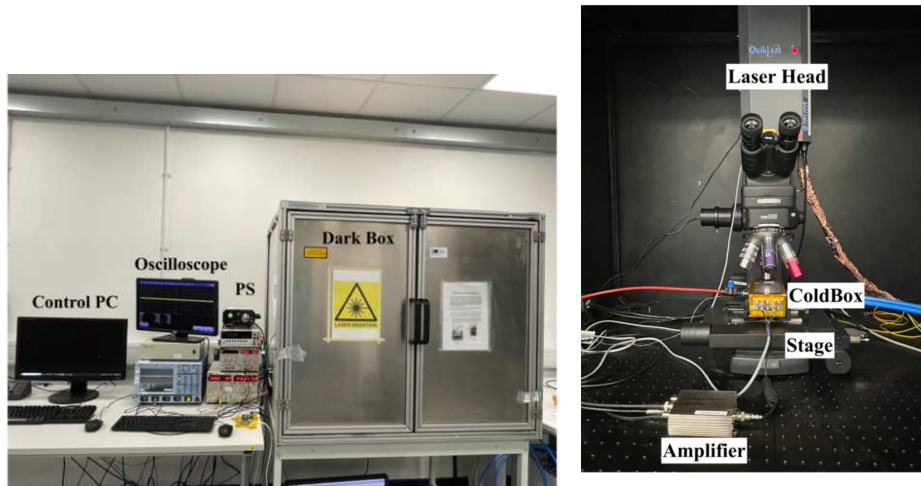


Figure 6. Setup for the charge collection test at RAL. Left: dark box housing the Trilite Laser. Right: detail of the Trilite Laser with a cold box on the stage and the charge amplifier.

Test setups at Carleton University. For the IV characteristics measurements at Carleton, a Keithley 2410 HV PS and 6517 SMUs were used for the biasing of the device and current measurements. A WayneKerr 6440B LCR meter was used for the CV measurement. All instruments are coupled to a SemiProbe PS4L automatic probe system which allows measuring the devices on wafers after dicing. Defect characteristics were measured using a SEMETROL DLTS system [14], shown in figure 8. This system uses a sample holder connected to a liquid helium cryostat, allowing it to lower the sample temperature to below 40 K or heat the sample above room temperature. Aside from standard DLTS measurements [15] and temperature-dependent IV and CV scans, the SEMETROL DLTS system can also employ a wide range of spectroscopic measurements to characterise charge

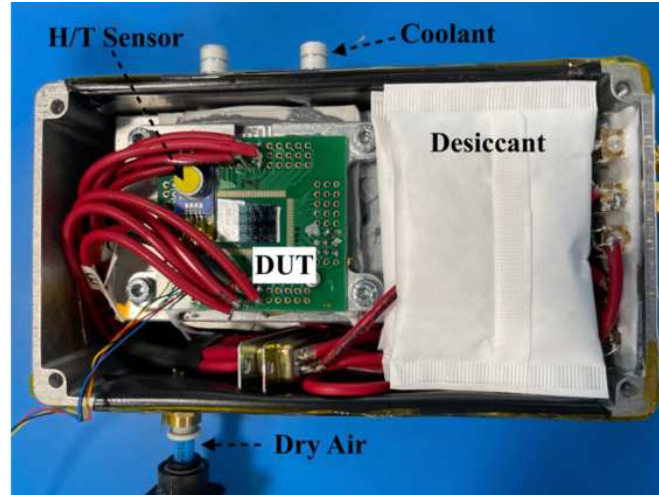


Figure 7. Coldbox housing the Schottky diode and *pn* junction devices for test. H/T means Humidity and Temperature.

traps: current DLTS (I-DLTS) to analyse traps based on transients in diode current rather than capacitance; double-pulse DLTS (DDLTS) to determine the trap spatial profile and to determine the field dependence of the trap by varying the filling pulse; optical DLTS where the electrical filling pulse is replaced by an optical filling pulse from a pulsed LED; Thermal Admittance Spectroscopy (TAS) more appropriate for samples with high resistivity [16].

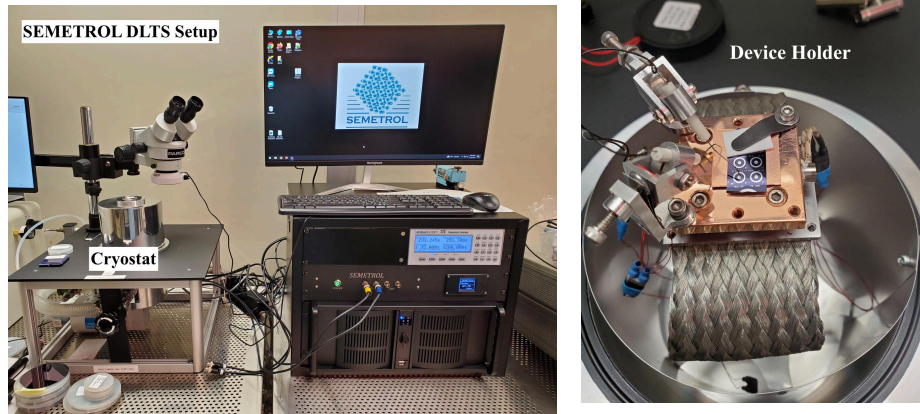


Figure 8. SEMETROL DLTS system at Carleton for the measurement of the defects.

4.2 IV test results

Schottky diode. The IV characteristics, in reverse and forward biasing mode at $T = 20^\circ\text{C}$, of Schottky diodes of Layout 3 were measured at OPMD and RAL using the setup described in section 4.1 and are shown in figure 9. In the reverse biasing mode with the guard ring (GR) floating (FLT), the electrical breakdown occurs above 650 V, and the leakage current is less than 100 nA before breakdown. Grounding (GND) the guard ring further reduces the leakage by a factor of around 3. In the forward biasing

mode, the current reaches around 1 mA before ohmic drop saturation becomes noticeable. The rectification ratio is close to 10^4 with respect to the current at the forward bias of 3 V. As described in appendix C, the ideality factors $n(V)$ and density of interface states $D_{is}(E)$ are extracted from the forward IV characteristics, and are shown in figure 10. To calculate $D_{is}(E)$, the assumed thickness δ of the interface layer was 2 nm, compatible with the expected value of the thickness of native oxide in silicon [17].

The IV characteristics of several non-irradiated Schottky diodes of Layout 1 are shown in figure 11.

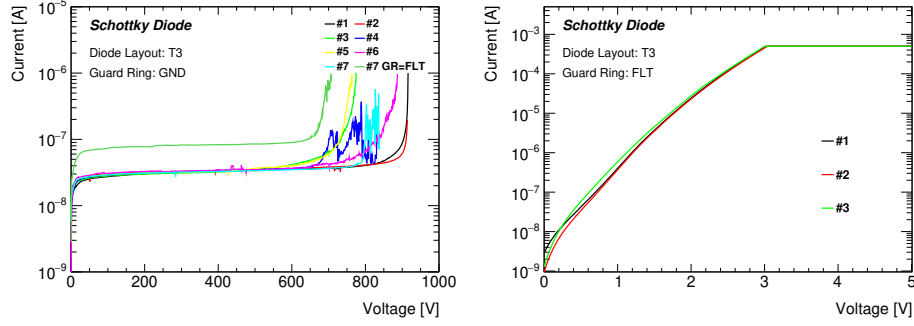


Figure 9. IV characteristics of Schottky diodes of Layout 3 measured at room temperature ($T = 20^\circ\text{C}$). Left: reverse IV. Right: forward IV.

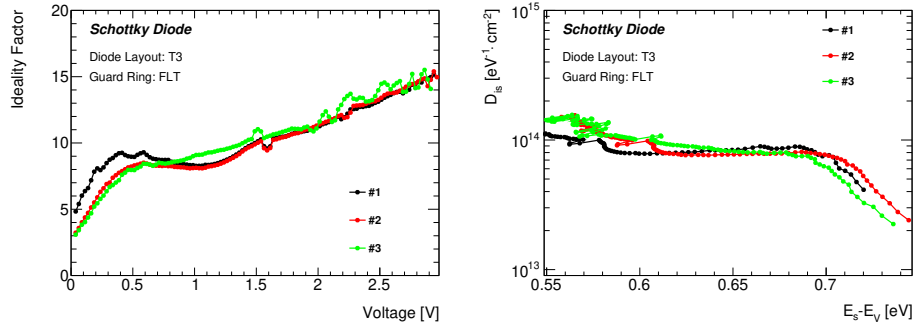


Figure 10. Left: the ideality factors $n(V)$. Right: the energy distribution profile of interface state densities $D_{is}(E)$.

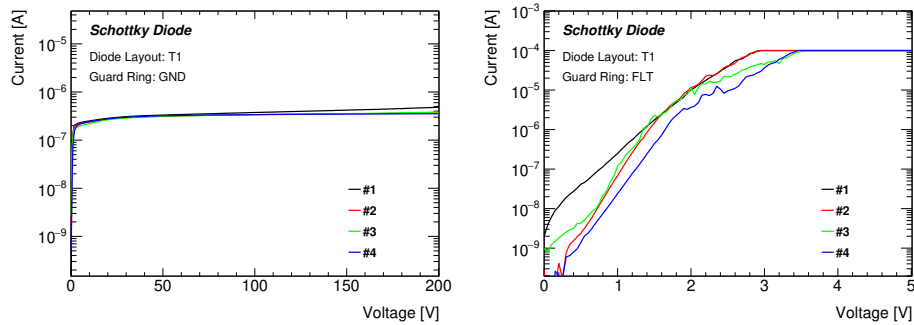


Figure 11. IV characteristics of Schottky diodes of Layout 1 measured at room temperature ($T = 20^\circ\text{C}$). Left: reverse IV. Right: forward IV.

pn junction. The reverse IV characteristics of *pn* junction devices of Layout 2 and 3 with regular guard ring (RGR) and *p*-stop guard ring (PGR) are shown in figure 12. The leakage current of the *pn* junction of Layout 3 with regular guard ring is less than 10 nA and the leakage current of the *pn* junction of Layout 2 is ~ 15 nA up to 30 V. For the devices with *p*-stop guard ring, the leakage current is highly suppressed. The cause of increase in leakage current starting at around 30 V is currently being investigated. Figure 13 shows the forward IV characteristics and the ideality factor $n(V)$ of an example *pn* junction of Layout 1.

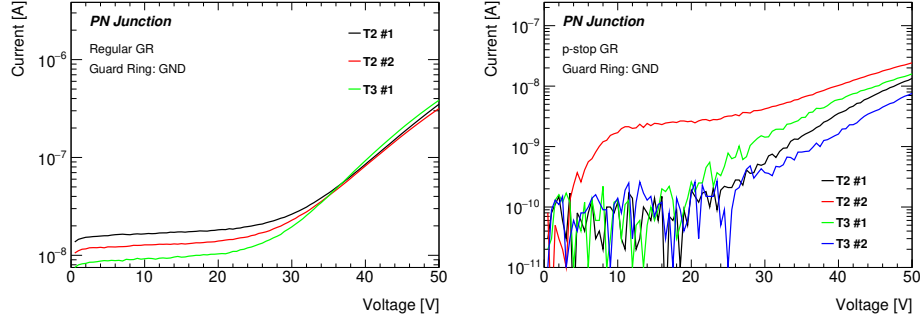


Figure 12. Reverse IV characteristics of *pn* junctions of Layout 2 and 3 measured at $T = 22^\circ\text{C}$. Left: regular guard ring. Right: guard ring with *p*-stop.

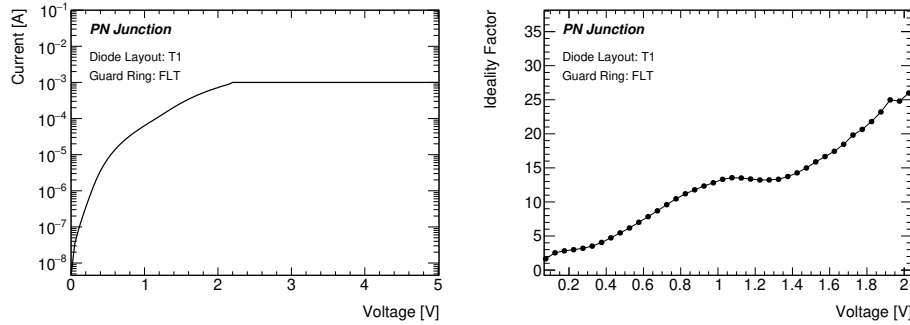


Figure 13. Left: forward IV characteristics of a *pn* junction of Layout 1 at $T = 22^\circ\text{C}$. Right: the ideality factor $n(V)$.

4.3 CV test results

Schottky diode. In the CV measurement of Schottky diodes, the AC signal amplitude was 100 mV and its frequency ranged from 10 kHz to 2 MHz. All measurements were performed at 20°C . Figure 14 shows the CV curves of the Schottky diode of Layout 3 under reverse biasing, the left figure shows the CV curves of 8 devices measured at the signal frequency of 100 kHz and the right figure shows the CV curves of one device measured at various frequencies. The cleanest CV characteristics were obtained at 100 kHz, therefore next CV plots are shown at this frequency. Due to the smaller error introduced by the lateral extension of the depletion region beyond the cathode electrode in calculating the effective area of the capacitor, here only the devices of the Layout 1 are used to extrapolate the full depletion voltage. Figure 15 shows the CV curves of the Schottky diodes of Layout 1 and an

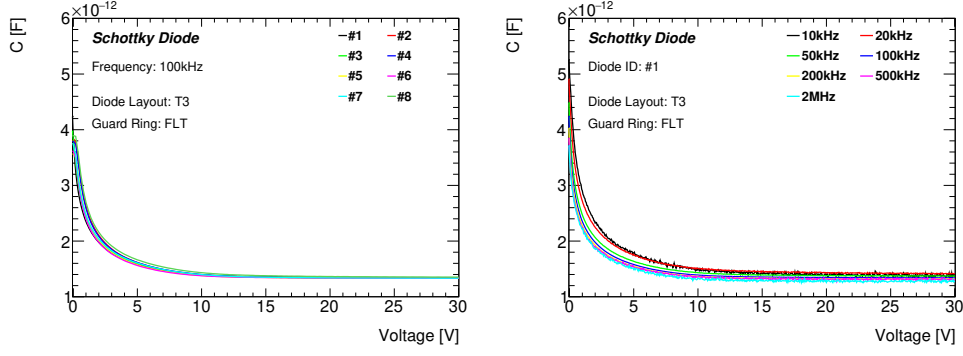


Figure 14. Left: the reverse CV of Schottky diodes of Layout 3 measured at the signal frequency of 100 kHz. Right: the reverse CV versus frequency of a Schottky diodes of Layout 3.

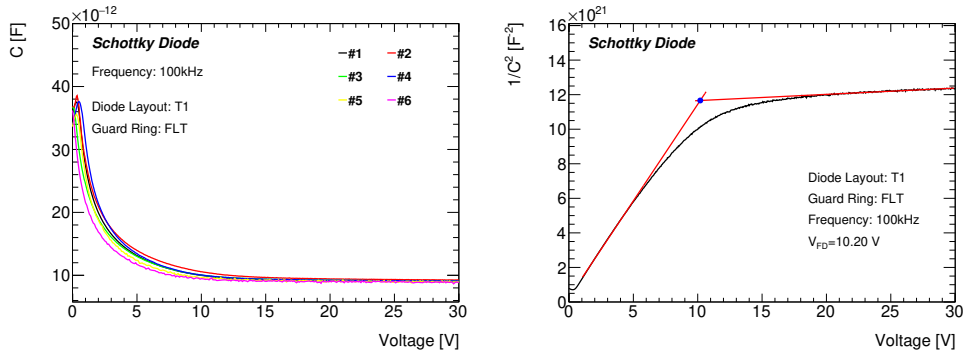


Figure 15. Left: the reverse CV of Schottky diodes of Layout 1 measured at the signal frequency of 100 kHz. Right: an example of $1/C^2$ versus voltage of Schottky diode of Layout 1, with the extracted full depletion voltage.

Table 2. Parameters of Schottky diodes of Layout 1 and 3.

Sample	Parameter	Average	σ
Schottky diode T3	Barrier height Φ_{Bp0} [V]	0.744	0.014
	Ideality factor $n(0)$	3.72	0.97
	Breakdown Voltage [V]	> 650/700	–
	Leakage current density at 50 V [$A \cdot cm^{-2}$]	1.35×10^{-5}	6.28×10^{-7}
Schottky diode T1	Barrier height Φ_{Bp0} [V]	0.88	0.072
	Ideality factor $n(0)$	3.32	0.6
	Full depletion voltage V_{FD} [V]	9.84	0.71
	Leakage current density at 50 V [$A \cdot cm^{-2}$]	1.01×10^{-5}	2.9×10^{-7}

example of $1/C^2$ versus voltage. The fully depleted voltage is extracted using the procedure described in appendix D, and it is ~ 10 V for Schottky diode of Layout 1.

Table 2 shows the Schottky diode parameter values obtained from IV and CV measurements.

pn junction. The plot of figure 16 shows the CV characteristics of one pn junction with the regular guard ring of the Layout 1 at the signal frequency of 100 kHz. The extrapolated full depletion voltage

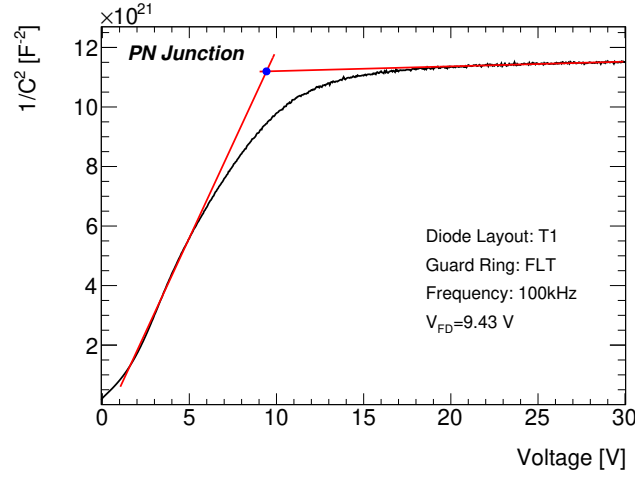


Figure 16. An example of $1/C^2$ versus voltage of pn junction of Layout 1 and the extrapolated full depletion voltage.

is 9.43 V and it is consistent with the value obtained from the Schottky diode and the expected theoretical value of the abrupt pn junction.

4.4 Charge collection efficiency test results

The CCE of the Schottky diode of Layout 3 and pn junction of Layout 2 were measured using the laser setup described in section 4.1 and scanning across the central region of the device in steps of 5 μm . The CCE values shown in this paper are the integral charges of the signal pulse.

Schottky diode. Figure 17 and figure 18 show the CCE of the Schottky diode along the scanning path crossing the device center at temperatures of 20, 10, 0, -10 , -20 $^{\circ}\text{C}$ and bias voltages of 50, 100, 200, 300, 400 V. The peaks in all figures represent the CCEs on the left and right edge of the cathode with the distance between the two peaks of ~ 600 μm , corresponding to the cathode size plus the overlapping metal. The effect of the decrease of the IR absorption coefficient due to the temperature [18] is evident in all figures, with a significant decrease of CCE from the temperature of 20 $^{\circ}\text{C}$ to -20 $^{\circ}\text{C}$, as shown in figure 17. The lateral extension of the depletion region changes marginally with the increase of bias voltage as shown in figure 18.

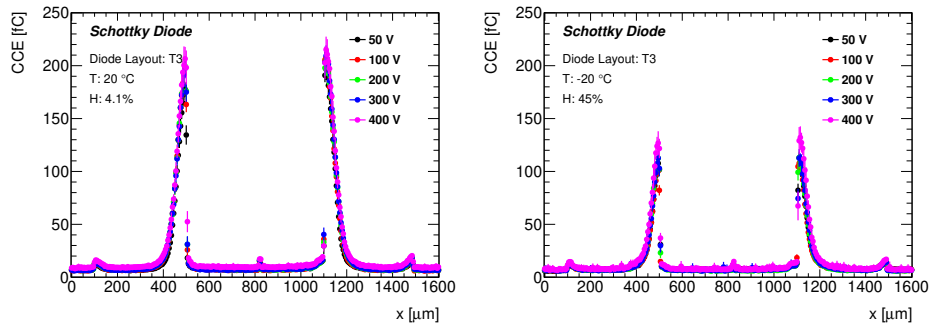


Figure 17. The CCE of the Schottky diode of Layout 3 versus bias voltages at two different temperatures. Left: $T = 20$ $^{\circ}\text{C}$. Right: $T = -20$ $^{\circ}\text{C}$.

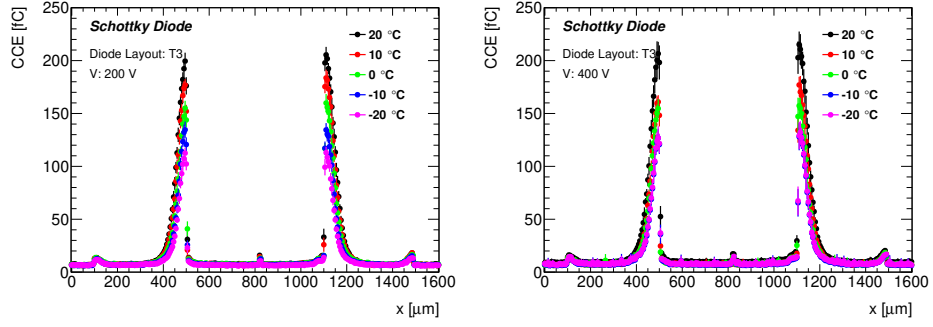


Figure 18. The CCE of the Schottky diode of Layout 3 versus temperatures at two different bias voltages. Left: 200 V. Right: 400 V.

pn junction. Figure 19 and figure 20 show the CCEs of the *pn* junction of the Layout 2 along the scanning path crossing the device center at temperatures of 20, 10, 0, -10 , -20 °C and bias voltages of 50, 100, 200 V. The central plateau corresponds to the central aperture of the Layout 2 with the size of ~ 200 μm , but otherwise the CCE plot shows the same characteristics as the Schottky diode.

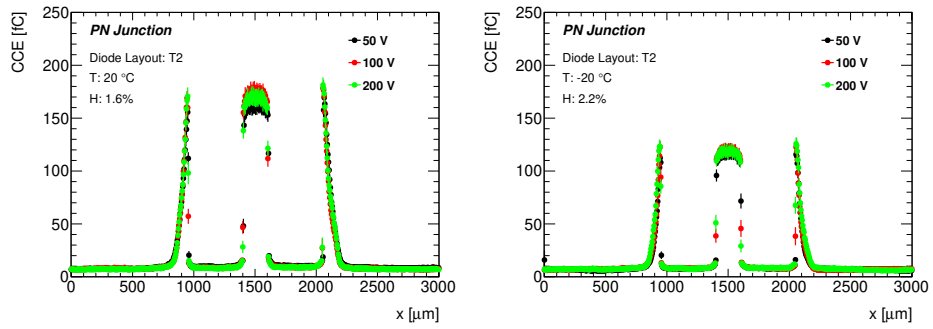


Figure 19. The CCE of the *pn* junction of the Layout 2 versus bias voltages at two different temperatures. Left: $T = 20$ °C. Right: $T = -20$ °C.

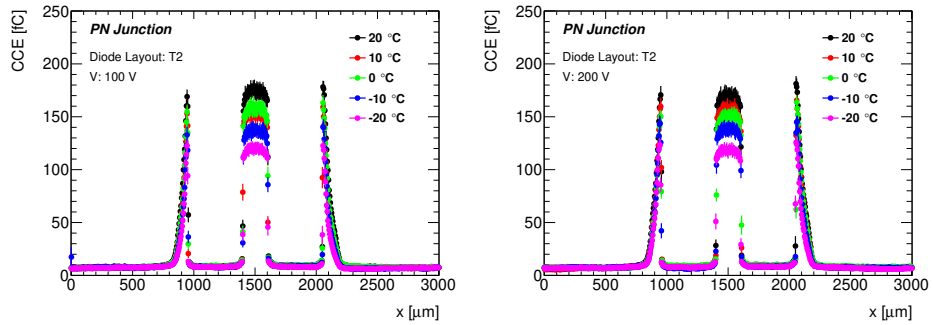


Figure 20. The CCE of the *pn* junction of Layout 2 versus temperatures at two different bias voltages. Left: 100 V. Right: 200 V.

4.5 DLTS results

The defect parameters of the unirradiated Schottky diodes and *pn* junctions of various flavors and production iterations have been characterised using the DLTS setup described in section 4.1. These parameters will then be implemented in TCAD models to compare simulations with test results. The same procedure will be repeated in the future with irradiated samples. For the DLTS measurements, multiple complete scans were performed for all diode samples at different bias voltages and filling pulse settings.

***pn* junction.** The left plot of figure 21 shows the obtained DLTS spectra of a *pn* junction with *p*-stop guard ring. Its extrema are extracted by the double or triple-Gaussian fit algorithms. The right plot of figure 21 shows the comparison between DLTS spectra derived from different selected rate windows and obtained for two distinct filling pulses. For the device with *p*-stop guard ring, using a filling pulse with forward bias allows measuring minority carriers (electrons), while majority carriers (holes) are measured using reverse bias filling pulses. The DLTS spectra did not qualitatively change with the applied bias voltage and only the observed trap saturation was affected. DLTS spectra are used to yield the Arrhenius plots for each of the scans performed, two of which are shown in figure 22 as examples. From both the DLTS spectra and the Arrhenius plots a good agreement is observed for the parameter causing the peak centered around 170 K.

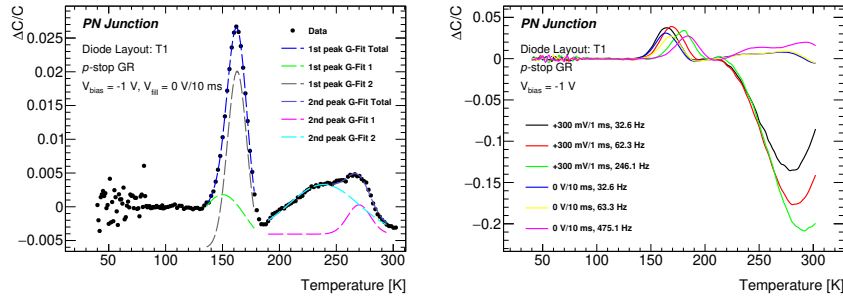


Figure 21. DLTS spectra of a *pn* junction with *p*-stop guard ring for selected rate windows. The double-Gaussian fits to derive the peak parameters are shown on the left as an example for the general analysis procedure.

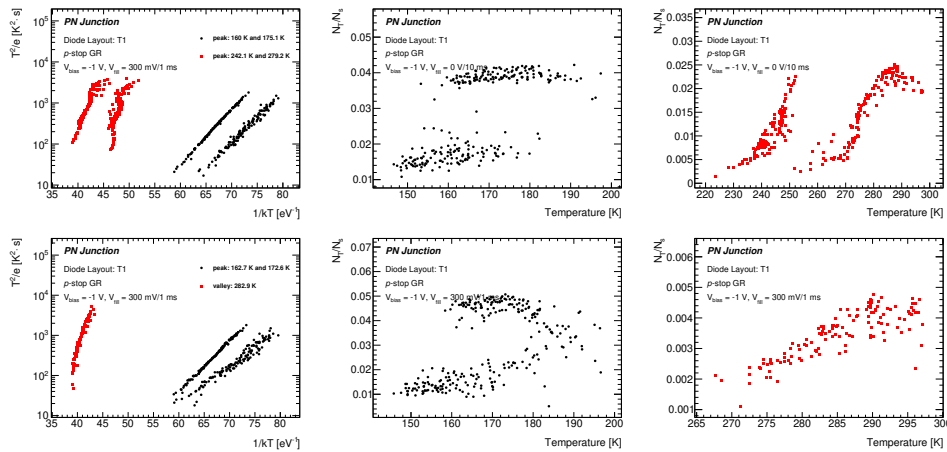


Figure 22. Left: Arrhenius plots of a *pn* junction with *p*-stop guard ring as examples for results obtained with both hole and high injection, using reverse and forward bias pulses, respectively. Middle and Right: relative trap saturation corresponding to the data points on the Arrhenius plots.

The *pn* junction samples with the regular guard ring were measured and analyzed in the same way, the DLTS spectra and the Arrhenius plots are shown in figure 23. Unlike the samples with the *p*-stop guard ring, the spectra did not vary much by changing the filling pulse voltage and there was no electron trap to be observed. However, the results for different bias voltages differed by a large margin and a specific peak at low temperatures showed a large dependence on the applied bias. This is an indication that this peak stems from surface or interface traps. Aside from that, the same common peak around 170 K could be observed and parameters showed good agreement between all scans. An additional onset of a peak at higher-than-room-temperature can be seen in the spectrum, but an analysis was not possible due to the limited temperature range of the scan.

Table 3 shows the trap parameters obtained from the DLTS measurements.

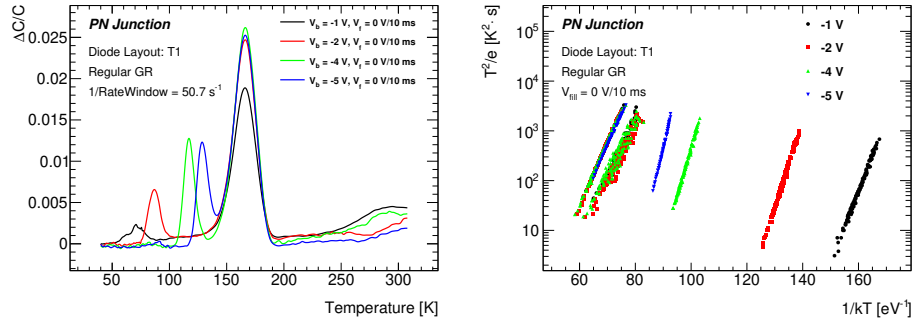


Figure 23. DLTS spectra of a *pn* junction without *p*-stop guard ring for the same filling pulse but different applied bias voltages (left) and resulting Arrhenius plots (right).

Table 3. Trap parameters obtained from DLTS measurements for *pn* junction diode samples. Common peaks between different scans are represented by a range of observed parameters.

Sample	Scan	T_{median} [K]	E_{trap} [eV]	σ [cm ²]
<i>pn</i> junction <i>p</i> -stop GR	$V_{\text{fill}} = 0 \text{ V}/10 \text{ ms}$	242.7	N/A	N/A
	$V_{\text{fill}} = 0 \text{ V}/10 \text{ ms}$	276.2	0.59 ± 0.04	$2.4 \times 10^{-14} \pm 5.4 \times 10^{-14}$
	$V_{\text{fill}} = 0 \text{ V}/10 \text{ ms}$	276.2	0.59 ± 0.04	$2.4 \times 10^{-14} \pm 5.4 \times 10^{-14}$
	$V_{\text{fill}} = 300 \text{ mV}/1 \text{ ms}$	282.9	-0.832 ± 0.037	$1.8 \times 10^{-10} \pm 4.5 \times 10^{-10}$
	common peaks	160–163 172–175	0.217–0.268 0.287–0.309	7.8×10^{-18} – 3.0×10^{-16} 2.2×10^{-16} – 1.0×10^{-15}
<i>pn</i> junction regular GR	$V_{\text{bias}} = -1 \text{ V}$	72.6	0.330 ± 0.007	$4.1 \times 10^{-1} \pm 3.1 \times 10^{-1}$
	$V_{\text{bias}} = -2 \text{ V}$	87.4	0.407 ± 0.005	$9.4 \times 10^{-1} \pm 2.0 \times 10^{-1}$
	$V_{\text{bias}} = -4 \text{ V}$	118.6	0.442 ± 0.005	$9.9 \times 10^{-6} \pm 1.6 \times 10^{-6}$
	$V_{\text{bias}} = -5 \text{ V}$	129.2	0.545 ± 0.007	$1.0 \times 10^{-3} \pm 1.9 \times 10^{-3}$
	common peaks	157–159 169–172	0.241–0.260 0.296–0.303	4.7×10^{-17} – 1.9×10^{-16} 4.9×10^{-16} – 8.3×10^{-15}

In addition to standard DLTS measurements, TAS scans were performed on the samples. This method not only complements the results obtained from DLTS, but also serves as a good method to test irradiated devices due to the limitations of DLTS for samples with high leakage current.

The Arrhenius plots of pn junctions with regular and p -stop guard ring are shown in figure 24, the obtained trap parameters are listed in table 4.

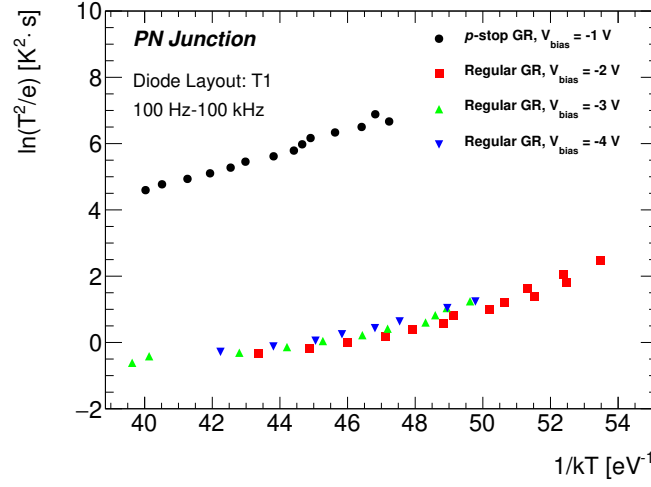


Figure 24. Arrhenius plots obtained from TAS measurements of pn junction diode samples.

Table 4. Trap parameters obtained from TAS measurements for pn junction diode samples.

Sample	V_m [V]	E_{trap} [eV]	σ [cm ²]
p -stop GR	-1	0.311 ± 0.026	$8.4 \times 10^{-19} \pm 3.1 \times 10^{-19}$
regular GR	-2	0.277 ± 0.043	$1.0 \times 10^{-16} \pm 8.3 \times 10^{-16}$
	-3	0.168 ± 0.040	$4.9 \times 10^{-19} \pm 6.2 \times 10^{-19}$
	-4	0.209 ± 0.037	$3.3 \times 10^{-18} \pm 5.5 \times 10^{-18}$

Schottky diode. Similar to the pn junction samples, the Schottky diodes have a common peak centered around 170 K. However, as can be seen in figure 25, unlike the pn junction diodes no other defects were observed in DLTS measurements. An additional minimum in the DLTS spectrum vanished when using shorter filling pulses, which indicates a small capture cross-section, and reduced voltages, thus avoiding surface and interface states from influencing the measurement. The resulting trap parameters are summarized in table 5.

Table 5. Trap parameters obtained from DLTS measurements for Schottky diode samples. N_T : the total density of deep level traps, N_s : the total free charge carrier density.

T_{median} [K]	E_{trap} [eV]	σ [cm ²]	N_T/N_s^*
170	0.312	5.5×10^{-15}	7.8×10^{-3}
180	0.294	3.3×10^{-16}	2.2×10^{-2}

TAS results for Schottky diodes show two trap states, while only one for pn junction diodes, as seen in figure 26. Arrhenius analyses of both (table 6) yield trap energy levels closer to the middle of

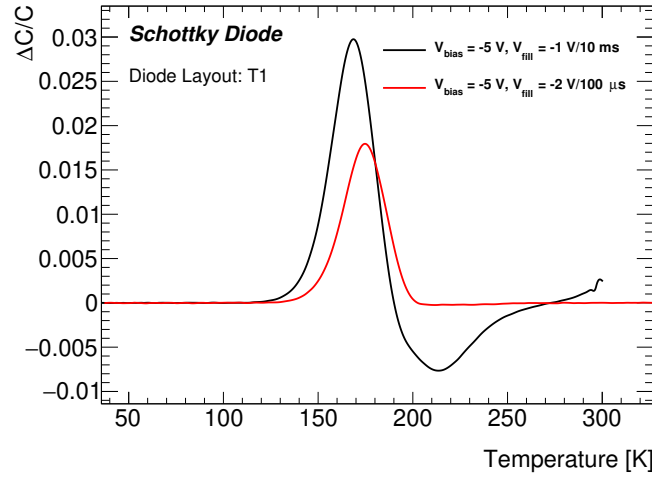


Figure 25. DLTS spectra of a Schottky Diode for different measurement parameters.

the band gap than those obtained from standard DLTS. In particular, the second trap near the midgap is expected to be a generation center and thus controlling the leakage current in the device.

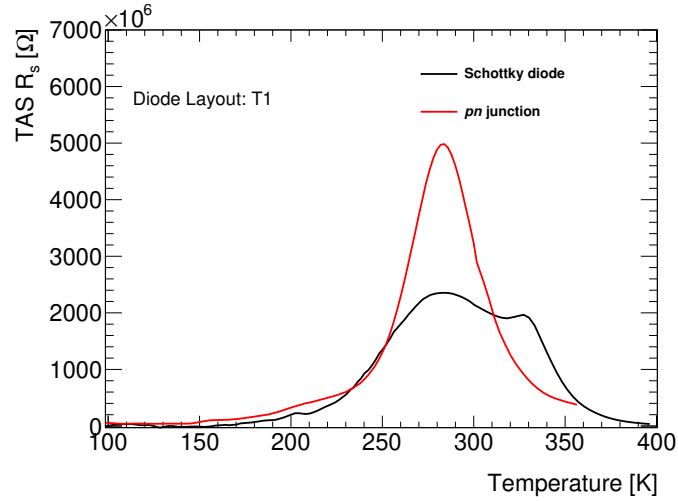


Figure 26. TAS R_s signal of a Schottky Diode (black) in comparison to a pn junction diode (red) as a function of time for a fixed AC signal frequency.

Table 6. Trap parameters obtained from TAS measurements for Schottky diode samples.

Sample	V_m [V]	E_{trap} [eV]	σ [cm ²]
Schottky diode	-1	0.498	1.6×10^{-14}
		0.664	3.5×10^{-13}
	2	0.467	3.0×10^{-15}
		0.614	3.7×10^{-14}

5 Conclusion and future plan

A research aimed at fabricating test structures, Schottky and *pn* junctions on *p*-type Silicon wafers, for the investigation of radiation bulk damage, has been described. The wafers used in this project are 6'' in size and feature a 50 μm thick epitaxial layer of five different levels of resistivity. The design consists of four different types of device layouts, differing in size to allow investigation of IV, CV and charge collection characteristics. Currently, Schottky diodes on three wafers of the highest resistivities, corresponding to the doping concentration of 10^{13} cm^{-3} have been successfully manufactured. Another two wafers have been successfully used for the fabrication of *pn* junctions, on wafers of doping concentration of 10^{13} cm^{-3} . Characterization of both Schottky and *pn* junctions is underway. First test results of the performances of the non-irradiated devices have been shown, demonstrating good electrical characteristics of the fabricated devices and the reliability of the in-house fabrication process. Extrapolation of variables of interest, from reverse and forward mode of operation, from CV analysis and charge collection using a custom-made laser injection setup have been reported. Results of the defect investigations using the DLTS technique have also been shown. The next step of this research is to complete the characterization by including results of neutron irradiated devices, from which we plan to extrapolate models to include in device simulators, and fabricate and test devices on wafers of medium (doping concentration: 10^{14} cm^{-3}) and low (doping concentration: 10^{15} cm^{-3}) resistivities.

Acknowledgments

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A Device fabrication process

Schottky diode. The full synopsis of the manufacturing process is shown in figure 27. Firstly, a 500 nm oxide layer was deposited on the wafers via Low-Pressure Chemical Vapour Deposition (LPCVD). The oxide thickness was measured at several places across the wafer. Then a 1.5 μm thick layer of JSR-IX575 photoresist was spin-coated onto the wafer surface. The wafers were then given a soft bake and exposed using broadband UV light followed by a post exposure bake. Thereafter, the wafers were developed using the TMA238WA developer. After resist development the wafers were given a descum to remove any resist residues. Next, the oxide was etched in an Ar/CHF₃ plasma using reactive ion etching. A white light reflectometer was used to check all the oxide had been etched. The resist was then stripped using acetone followed by an oxygen plasma in a barrel asher. To define the

metal contacts for the cathode and guard ring, a 3.3 μm thick layer of SPR220-7 photoresist was spun on the wafers followed by soft bake, a broadband UV exposure, subsequent hold time, post-exposure bake and development in MF26-A developer. This step was followed by a deposition of a 500 nm thick layer of Al using magnetron sputtering. The subsequent step of lift-off was performed in an ultrasonic bath of acetone. To aid resist removal the acetone was heated to 40 °C via DI water and the wafers were subjected to regular ultrasonic bursts of 30 minutes. The LPCVD oxide was then etched from the backside of the wafer and a 1 μm thick layer of Al was deposited to create an Ohmic contact. As the second process of photoresist deposition took place not immediately after the step of RIE oxide etching, with the wafers left exposed in free air inside the clean room, it is expected that a thin layer of native oxide grew over the top surface of the wafers. The presence of thin native oxide has been taken into account in the device analysis shown in appendix B.

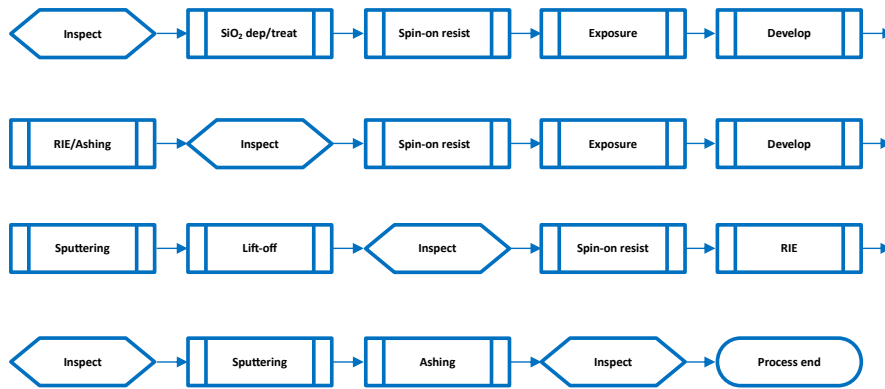


Figure 27. Process flow of Schottky device fabrication.

pn junction. *pn* junction diode fabrication began with the growth of 150 nm of thermal oxide in a dry oxygen ambient at 1025 °C. This oxide provides surface passivation and serves to mask the phosphorus diffusion used to form the junction. Oxidation was followed by an in-situ nitrogen ambient anneal for 20 minutes to reduce oxide fixed charge. Contact photolithography with wet etching was then used to open windows through the oxide for phosphorus diffusion to form large circular n^+ cathodes. Oxide was left on the wafer backsides as a diffusion mask. Diffusion was carried out from a POCl_3 vapour source diluted in nitrogen at 900 °C for 5 minutes. Processing then split into three different paths for guard ring (GR) formation. For *p*-stop GR samples photolithography with plasma etching was used to thin the oxide to 20 nm in annular rings surrounding the cathodes. $^{11}\text{B}^+$ ions were implanted through the thinned oxide at $3 \times 10^{13} \text{ cm}^{-2}$ dose and 20 keV energy to form a region of enhanced *p*-type doping preventing surface inversion. Photoresist was left in place to mask the implant. The implant was annealed at 900 °C for 10 minutes in nitrogen. For non-isolated GR samples oxide was completely removed in the annular ring, but these samples were not implanted. For isolated GR samples no additional processing was done at this stage. After etching 1% hydrofluoric acid to hydrophobia to clear oxide from contact windows. A 750 nm aluminum layer was then deposited on the front of all samples by e-beam evaporation. Photolithography with wet etching in hot phosphoric acid was used to pattern the aluminum. Swabbing with hydrofluoric acid was then used to remove oxide from

the wafer backs, after which 500 nm of aluminum was deposited by e-beam to create a back contact. Contacts were sintered in pure hydrogen at 400 °C for 10 minutes.

B Schottky barrier in the presence of interface states

Figure 28 shows the band diagram of a Schottky junction on *p*-type silicon with a thin insulating layer between the metal cathode and substrate:

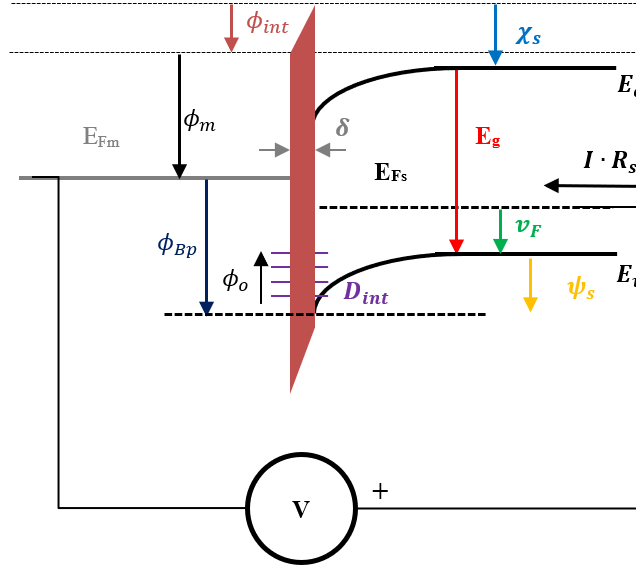


Figure 28. Band diagram of Schottky junction on *p*-type silicon, including a thin interface layer and interface states.

The voltage ϕ_{int} across the layer of thickness δ is given by:

$$\phi_{\text{int}} = -V + IR_s - v_F - \psi_s + \frac{1}{e}(E_g + \chi_s - \phi_m) \quad (\text{B.1})$$

where $v_F = \frac{kT}{e} \ln\left(\frac{N_v}{N_a}\right)$ [V] is the Fermi potential, ψ_s [V] is the surface potential, E_g [eV] is the bandgap, χ_s [eV] the electron affinity of semiconductor, ϕ_m [eV] the metal work function, e [C] the elementary charge magnitude, V the external voltage applied, R_s the bulk resistance and I the current flowing across the device. From Gauss's law:

$$\frac{\phi_{\text{int}}}{\delta} = \frac{Q_m}{\epsilon_i} \quad (\text{B.2})$$

where Q_m is the charge accumulated on the metal side and ϵ_i is the permittivity of the interface layer. The neutrality condition implies:

$$Q_m = -Q_{\text{sc}} - Q_{\text{ic}} \quad (\text{B.3})$$

where Q_{sc} is the space charge in the semiconductor and Q_{ic} is the interface charge. Under the full depletion approximation, furthermore:

$$Q_{\text{sc}} = -\sqrt{2e\epsilon_s N_a \psi_s} \quad (\text{B.4})$$

$$Q_{\text{ic}} = -eD_{\text{is}}(\psi_s + v_F - \phi_o) \quad (\text{B.5})$$

where D_{is} [$\text{cm}^{-2} \text{eV}^{-1}$] is the density of interface states, ϕ_o [V] their neutral potential level from the top of valence band and N_a [cm^{-3}] the dopant concentration.

From (B.1)-(B.5) one gets:

$$-V + IR_s - v_F - \psi_s + \frac{1}{e}(E_g + \chi_s - \phi_m) = \frac{\delta}{\varepsilon_i}(\sqrt{2e\varepsilon_s N_a \psi_s} + eD_{is}(\psi_s + v_F - \phi_o)) \quad (\text{B.6})$$

After collecting the terms, (B.6) gives:

$$\psi_s + \gamma\zeta\sqrt{\psi_s} = \gamma\frac{1}{e}(E_g + \chi_s - \phi_m) + \gamma(-V + IR_s) - v_F + (1 - \gamma)\phi_o \quad (\text{B.7})$$

where $\gamma = \frac{\varepsilon_i}{\varepsilon_i + e\delta D_{is}}$, $\zeta = \frac{\delta}{\varepsilon_i}(\sqrt{2e\varepsilon_s N_a})$.

Equation (B.7) expresses the non-linear relationship between ψ_s and the applied voltage V . For no interface layer, i.e. $\gamma = 1$ and $\zeta = 0$, (B.6) reduces to the Schottky-Mott limit [17, 19, 20], with the barrier height a function of the metal work function ϕ_m only. The presence of a thin layer reduces the Schottky-Mott and increases a Bardeen behavior of the junction [21], introducing a non-linearity in the relationship through the second term in the left hand side of (B.7). Furthermore, as the interface state density D_{is} might depend on the energy and, thus, present different values depending on the voltage bias applied, the ψ_s relationship with V might take a rather complicated form. It is possible to simplify (B.7) in the case of an interface layer of small thickness, e.g. when only 1–2 nm of native oxide is present on the silicon surface [22, 23]. Indeed, the product $\gamma\zeta$, essentially a measure of the dominance of surface states charge over space charge, is usually < 1 up to relatively high values of doping N_a and realistic values of D_{is} [24], which allows neglecting the second term in left hand side of (B.7), as shown in figure 29:

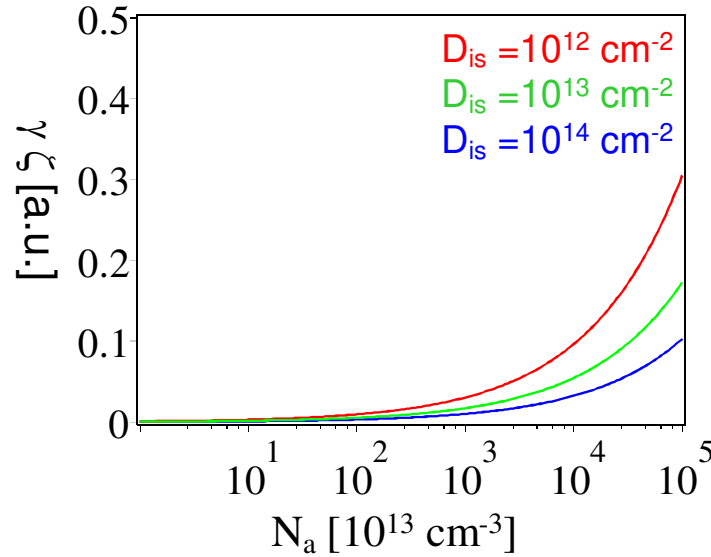


Figure 29. The $\gamma\zeta$ product of equation (B.7) versus doping $N_a/10^{13}$ for different values of D_{is} and $\delta = 2$ nm.

For doping N_a up to 10^{17} cm^{-3} , (B.6) can be approximated as:

$$\psi_s = \gamma\frac{1}{e}(E_g + \chi_s - \phi_m) + \gamma(-V + IR_s) - v_F + (1 - \gamma)\phi_o \quad (\text{B.8})$$

The expression (B.8) for $V = 0$ gives the barrier height at zero bias ϕ_{Bp0} :

$$\psi_{s0} + v_F = \phi_{Bp0} = \gamma \frac{1}{e} (E_g + \chi_s - \phi_m) + (1 - \gamma) \phi_o \quad (\text{B.9})$$

C Schottky barrier IV characteristics in the presence of interface states

To have good rectifying properties, a Schottky diode should be fabricated using metals of suitable work function, to guarantee high barrier height to the semiconductor substrate. According to the Schottky-Mott model the barrier height ϕ_{bp} of an ideal contact between a metal and a p -type semiconductor in the absence of surface states depends on the difference between the metal work function ϕ_m and the electron affinity χ_s of the semiconductor:

$$\phi_{bp} = \frac{1}{e} (E_g + \chi_s - \phi_m) \quad (\text{C.1})$$

where $e[C]$ is the elementary electron charge and $E_g[\text{eV}]$ is the band gap energy. Choosing the correct metal is therefore essential to obtain a high barrier height [25]. As aluminium has a relatively low work function [26], it is a suitable candidate for fabricating Schottky devices on p -type silicon. However, various reports [27–29] show that the barrier height ϕ_{bp} indeed changes with ϕ_m but does not scale linearly as predicted by the Schottky-Mott model (C.1). The model proposed by Bardeen includes the presence of interface states, due to silicon dangling bonds at the surface. These states might cause a pinning of the Fermi level which influences the barrier height. The resulting relationship between metal work function and barrier height in the presence of a thin insulating layer and related interface states is given by (B.7). With the doping concentrations satisfied in this project, the model of Cowley and Sze [30, 31], which essentially connects the Schottky-Mott and Bardeen models, is however valid and is expressed by (B.8).

The parameters of the interface can be determined from the forward biased diode characteristics [32], which, under the assumption of thermionic emission and neglecting image force lowering [25, 33] express the current as:

$$I = SA^*T^2 e^{\left(-\frac{e\phi_{Bp0}}{kT}\right)} e^{\left(\frac{eV}{nkT}\right)} = I_0 e^{\left(\frac{e}{nkT}(V - RI)\right)} \quad (\text{C.2})$$

where $S [\text{cm}^2]$ is area of the device, $A^* [\text{A} \cdot \text{cm}^{-2} \cdot \text{K}^{-2}]$ the Richardson's constant, around 32 for p -type silicon, $T [\text{K}]$ the temperature, n the ideality factor, $\phi_{Bp0} [\text{eV}]$ the barrier height between semiconductor and metal at zero bias and R is the resistivity of the bulk, which causes an ohmic drop in the applied voltage. From (C.2), by extrapolation at $V = 0$, one obtains:

$$\phi_{Bp0} = \frac{kT}{e} \ln \left(\frac{SA^*T^2}{I_{V=0}} \right) \quad (\text{C.3})$$

and, after some algebraic manipulation:

$$\frac{dV}{d \ln(I)} = \frac{nKT}{e} + RI \quad (\text{C.4})$$

which, plotted as function of I , provides R as the slope in the linear region of the plot and values of $n(I)$, from which the ideality factor $n(V)$ can be obtained. Assuming the interface states equilibrate with the semiconductor only [34], the ideality factor n can be expressed as:

$$n(V) = 1 + \frac{\delta}{\epsilon_i} \left(\frac{\epsilon_{si}}{W} + eD_{is} \right) \quad (\text{C.5})$$

where ϵ_i is the permittivity of the insulating layer between silicon and the metal, ϵ_{si} the permittivity of silicon, W is the width of the space charge region and D_{is} is the density of interface states. From (C.5) one gets:

$$D_{is}(V) = \frac{1}{e} \left(\frac{\epsilon_i}{\delta} (n(V) - 1) - \frac{\epsilon_{si}}{W} \right) \quad (C.6)$$

In the case of a p -type silicon, the interface state energy E_s measured from the top of the valence band E_v is given by:

$$E_s - E_v = e \left(\phi_{Bp0} - \frac{V}{n(V)} \right) \quad (C.7)$$

Using (C.5), (C.6), the plot of interface states D_{is} versus energy $E_s - E_v$ can be obtained. From (B.9) and the value of D_s at $V = 0$ the value of neutrality level ϕ_0 can also be obtained.

D Schottky capacitance in the presence of interface states

Using (B.4) and (B.5), the capacitance per unit area is given by:

$$C = \frac{d}{dV} (Q_{sc} + Q_{ic}) = \frac{d}{d\psi_s} (Q_{sc} + Q_{ic}) \frac{d\psi_s}{dV} \quad (D.1)$$

The full expression of (D.1) would require using (B.7) and current expression (C.2) to calculate the derivative of ψ_s versus V . However, using the approximate expression (B.8), one gets:¹

$$C(V) = \left(\sqrt{\frac{e\epsilon_s N_a}{2\psi_s}} + eD_{is} \right) \frac{\gamma}{1 + IR_s \frac{e}{n kT}} \cong \left(\sqrt{\frac{e\epsilon_s N_a}{2\psi_s}} + eD_{is} \right) \frac{\gamma}{1 + \gamma IR_s \frac{e}{kT}} \quad (D.2)$$

The approximation of $\frac{1}{n} = \gamma$ in the right hand side of (D.2) stems from (C.5), assuming negligible² the contribution of $\frac{\epsilon_{si}}{W(V)}$ to D_{is} . Expression (D.2) shows that the capacitance depends non-trivially on the interface states. However, in the reverse biased region and for small leakage current I , the contribution in the denominator of second term in right hand side of (D.2) is negligible,³ from which:

$$C(V) \cong \left(\sqrt{\frac{e\epsilon_s N_a}{2\psi_s}} + eD_s \right) \gamma \quad (D.3)$$

The effect of interface states on capacitance is expected to decrease as the frequency of the AC signal applied is increased, owing to the inability of the states to follow rapidly changing signals. Thus, at high frequency, and neglecting the second term in parenthesis in the right hand side of (D.3), one gets:

$$C^{-2}(V) \cong \frac{2\psi_s}{e\epsilon_s N_a} \gamma^{-2} \quad (D.4)$$

¹The derivative $\frac{d\gamma}{dV}$ is assumed to give negligible contribution.

²The extension of depletion width $W(V)$ renders the second term in right hand side of (C.5) negligible w.r.t. the first. This is certainly verified for low doping conditions and up to moderate forward biasing.

³In case of irradiated devices the condition of low leakage might not be fulfilled, a case not treated here. This would require a different approach to the calculation of capacitance, due to the introduced defects in the bandgap.

Substituting in (D.4) expression (B.8) for ψ_s and equating to 0 gives for the diffusion potential ψ_{s0} :

$$V_0 - I_0 R_s = \frac{\frac{\gamma}{e} (E_g + \chi_s - \phi_m) - v_F + (1 - \gamma)\phi_o}{\gamma} = \frac{\psi_{s0}}{\gamma} \quad (\text{D.5})$$

i.e. the point of intercept of C^{-2} with the V axis provides the γ -scaled diffusion potential ψ_{s0} .

From (D.4), the slope of $C^{-2}(V)$ with respect to V is given by:

$$\frac{dC^{-2}(V)}{dV} \cong \frac{2}{e\epsilon_s N_a} \gamma^{-1} \quad (\text{D.6})$$

i.e. the slope depends not only on the actual doping N_a but also on the density of interface states via γ^{-1} .

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