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An ultrafast digitizer for continuous measurements from microwave fusion diagnostics

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ABSTRACT

Fast digitizers are employed in a variety of experimental contexts, including for microwave measurements from fusion plasma diagnostics. However, most existing commercial digitizers used for this purpose are severely limited by their onboard memory. Here we present a system developed from mostly commercially available hardware components capable of acquiring essentially indefinitely (here ~10 s) while meeting the target performance of 5 GHz analog bandwidth with a rate of 10 billion samples per second and 8 bits per sample. At its core is a field-programmable gate array (FPGA) receiving data from a high-performance analog-to-digital converter (ADC). The data are continuously streamed with a maximum throughput of 120 Gb/s from the FPGA to a computer over optical fiber in the form of raw Ethernet packets, allowing the use of entirely standard networking hardware in the PC. Whilst this technology is transferable to a range of applications, we are motivated by the demands of microwave scattering measurements, for which the new digitizer increased the acquisition duty cycle from 6% to 100%. In this paper we describe our digitization system, demonstrate its capability, and then use it to acquire data from microwave diagnostics at the ASDEX Upgrade and Wendelstein 7-X fusion experiments.

1. Introduction

Global efforts towards achieving fusion energy as a viable power source undergo an increase in the size of experiments and the duration of their discharges, particularly for magnetically confined plasmas. This means that any measurement made on such devices must be taken over a longer time than previously. Furthermore, to better understand the physics of the plasmas in these machines, the performance of diagnostic systems must be improved. Specifically, microwave diagnostics are of general importance for monitoring laboratory plasmas. They are likely to retain a key role in future devices as they can robustly operate under reactor-relevant conditions. An example is collective Thomson scattering (CTS), planned for fusion-born alpha-particle monitoring in ITER [1–3] and potentially DEMO [4].

Most fusion plasma diagnostics in the microwave range rely on spectrograms with high frequency and time resolution across several GHz of bandwidth. While traditional filter-based radiometers can offer a very broad bandwidth, they are in practice limited in their frequency resolution. Instead, the increase in digitizer sample rate has enabled direct sampling of GHz waves. This has significant advantages when resolving MHz waves in the microwave spectrum [5,6]. However, for 5 GHz of bandwidth with 8-bit samples, this represents at least 80 Gb/s of data to transfer to storage, usually exceeding the typical storage capacity and/or transfer rate (e.g. PXIe max rate of 56 Gb/s per slot [7]) of commercial products, for long acquisitions. At these data rates, the performance of commercially available digitizers is usually limited by either total acquisition duration or cost.

To increase the acquisition performance, one could use digitizers with a bigger on-board memory. The latter is usually limited by hardware compatibility, therefore preventing further upgrades, and puts an upper cap to the acquisition time per plasma discharge. The other option is to increase the transfer rate beyond the acquisition rate, and stream the data with First-In-First-Out (FIFO) protocols. The only limitation is then the final storage space, which is a lot less restricted.

In this paper we present a novel fast digitizer which allows improved sampling capabilities at a much lower cost than comparable commercially available digitizers. This new setup is inspired by the

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digitizers of the Mega Amp Spherical Tokamak (MAST) synthetic aperture microwave imaging system [8]. We employed a similarly generic approach, pursuing the technical requirements relevant for CTS at ASDEX Upgrade (AUG) and future fusion devices. The new digitizer is centered around a high-speed analog-to-digital converter (ADC), operated through a field-programmable gate-array (FPGA) carrier. The ADC+FPGA combination is a challenging tool to develop in many aspects (Verilog language, custom PCB design...). It also offers unparalleled flexibility and state-of-the-art performance for multi-GHz sampling rates and bit-depth. These architectures allow real-time processing (*i.e* computing in a timely manner with respect to deadlines imposed by external processes [9]) and have thus become a preferred solution for this performance range, driven by commercial applications in radar systems [10], cellular networks [11] and software-defined radios [12]. By leveraging cutting-edge technology, they also find applicability in radio astronomy [13] and particle accelerators [14] as well as fusion engineering [15]. The setup presented here allows acquisition with 8-bit precision at 10 GSa/s (Gigasamples per second) and bandwidth of 5 GHz. In addition to this performance, the main improvement in our system lies in the capability of continuous data streaming to the storage computer, providing access to uninterrupted measurements. This uses commercially off-the-shelf network interface components and streams the data over arbitrary long distances through optical fibers. This optimizes scientific returns as data acquisition covers full discharges, which also greatly facilitates experimental planning and diagnostic operation. The ADC is furthermore potentially capable of a 12-bit precision, with additional development.

This paper describes the new digitizer setup, referred to as SiCCAF (Single-Channel Continuous ADC+FPGA), and the context it has been used in by detailing the hardware and software development, a summary of its characterization tested in our lab, and some examples of the recorded data in current fusion devices (AUG and W7X). With its low cost, easy reproducibility, and superior sampling capabilities, such a setup could be of general relevance for any microwave diagnostics, including in existing and future fusion devices.

2. Experimental context

The digitizer described in the following, while relevant for a broad range of applications, has been developed both to fulfill the requirements of present collective Thomson scattering diagnostics installed on AUG and W7X and to prepare for future fusion devices. CTS diagnostics observe the interactions of high-power microwave beams with plasmas, providing essential information on confined-ion properties [16]. While the primary goal is the characterization of thermal and fast ions, the heterodyne receiver lines have seen increasing use for the observation of parametric decay instabilities (PDI) [17] at various frequencies. While the physics behind these phenomena differ, their observation can be done with very similar setups: powerful microwave beams must be injected into the plasma, and, provided the appropriate conditions are met, *e.g.* the Salpeter criterion for CTS [18] or the local power threshold for PDI [19], this generates microwave signals, which can be detected by a receiver.

Both AUG and W7X make use of 140 GHz gyrotrons for heating the plasma in standard operation, with frequency regions of interest around 70, 140, and 210 GHz for PDI observation [20]. For CTS, the measurements are typically performed using probe frequencies of 105 GHz (AUG) and 140/174 GHz (W7X). These microwave signals are intercepted by horns and brought to measurable frequencies with one- and two-step heterodyne downconversion chains, the details of which are beyond the scope of this article. However, the last stage of the system, allowing digitization, constitutes the baseline for the acquisition performance of any new digitization system. The existing setups consist of filter banks [21] measuring around a center frequency of 10 GHz, and one fast digitizer [6] measuring from DC to its bandwidth.

The filter banks have historically been the primary source for CTS data, particularly fast ion measurements [22–24]. These filter banks split the signal into separate channels. Each channel has a filter of bandwidth ranging from 80 MHz to 1.0 GHz across a wide frequency span (9.75 GHz and 6.75 GHz in AUG, 10 GHz in W7X). The remaining signal is then sent through Schottky diodes and the produced voltage is digitized with PCI-4472 ADCs by National Instruments. This effectively yields the mean power going through each channel with 24 bit precision at 102,400 samples per second. This system achieves continuous acquisition, with a 10 μs time resolution over the whole spectrum investigated, at the cost of having a relatively low frequency resolution. This, however, makes it less relevant for PDI studies or thermal-ion CTS measurements [6].

Complementing this is a PXIe-5186 fast digitizer by National Instruments, already characterized in previous literature [6]. It has the capacity to sample an 8-bit dynamic range at 12.5 Gigasamples per second, with an analog bandwidth of 5 GHz. However, the current setup makes use of the two channels of the device for an improved background subtraction via a secondary "passive" view [25], effectively cutting the sampling rate to 6.25 GSa/s per channel at a bandwidth of 3.125 GHz. This has allowed to accurately resolve bulk ion properties [16,26] and to conduct 70/140 GHz PDI observations [19,27]. The instrument is equipped with one GB of memory buffer, meaning it can hold 80 ms of data at any given time, if running at full sampling rate. This buffer memory is being transferred continuously to permanent storage at a rate of 550 MB/s which is lower than the acquisition rate by a factor of ≈ 20. To avoid overflowing the buffer memory, the acquisition is done in pulses of duration in the order of a millisecond, potentially distributed across the full duration of a discharge. In its current state, this device is limited to less than half a second of acquisition over an eight-seconds discharge. This duty cycle below 6% (or 11% in single-channel/half-rate operation) puts heavy constraints on how dedicated CTS/PDI shots are planned, and adds extensive preparation work. Additionally, the reduced bandwidth currently used precludes measurements at frequency shifts $\gtrsim 1.5$ GHz from the probe gyrotron, such as those of the fast-ion tails in CTS spectra.

An ideal addition to these devices would be a fast digitizer (improving on the frequency resolution of the filter-banks) which would be capable of continuous acquisition (improving on the duty cycle of the current digitizer) for at least the duration of experiments on AUG (≈ 10 s). Such a device should have a bandwidth of at least 5 GHz, to allow useful coverage of CTS/PDI spectra. Considering the exploratory nature of some of the conducted CTS/PDI measurements, no fixed time-averaging can be considered appropriate in all cases, thus the new device should at least initially store all acquired data. However, with W7X aiming at 30 min shots in future campaigns and much longer discharges envisaged for future fusion power plants, the storage of full-discharge data acquired with present fast digitizers would become impractical, with 30 min of raw data potentially taking up ≈ 20 TB. Therefore, having a platform to start developing and testing on-board processing of digitizer data (e.g. FFT, averaging, machine learning methods...) is essential for any future digitizer-based real-time applications.

3. FPGA based fast digitizer

3.1. Overview

As described in Section 2, our microwave diagnostics at AUG and W7-X would ideally require acquisition speeds of several billion samples per second over plasma discharge lengths of up to 10 s. To achieve this, we developed a system with three primary blocks: an analog-to-digital converter (ADC), a field-programmable gate array (FPGA), and a storage computer (PC). An overview of the generic workflow is sketched in Fig. 1.

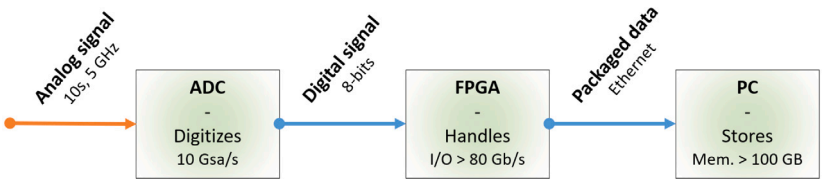

Fig. 1. Schematic overview of the acquisition system and requirements established in Section 2: an analog signal (left) of specific duration and bandwidth arrives at the device. It is digitized by the ADC at the required Nyquist rate. The FPGA then handles the digital data faster than it is received and sends it to storage on the PC's memory. These requirements avoid memory overflow on any shown component.

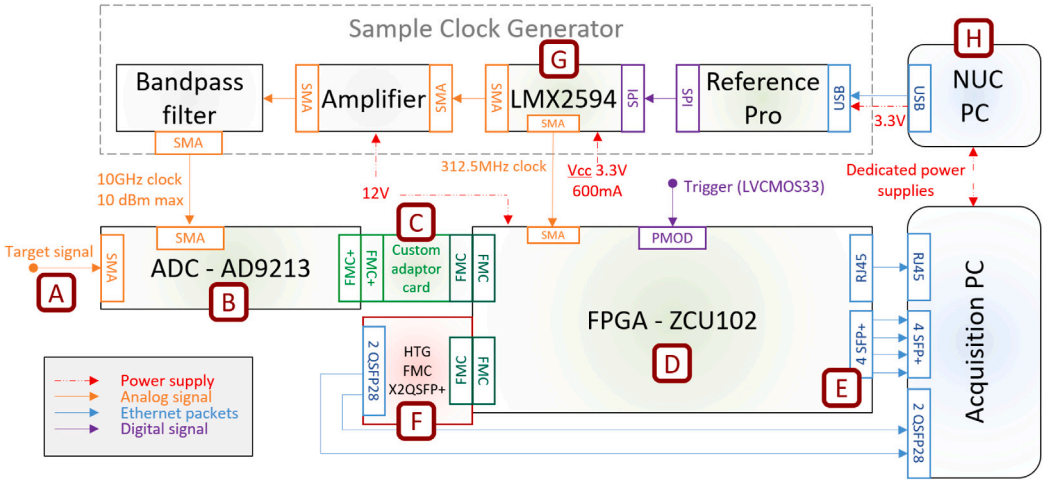

Fig. 2. Schematic of the fast digitizer setup, including the sample clock generation. The analog signal arrives at A, and data flows following alphabetical order until F. See text for details. External connections are represented by arrows, color coded by the type of signal sent.

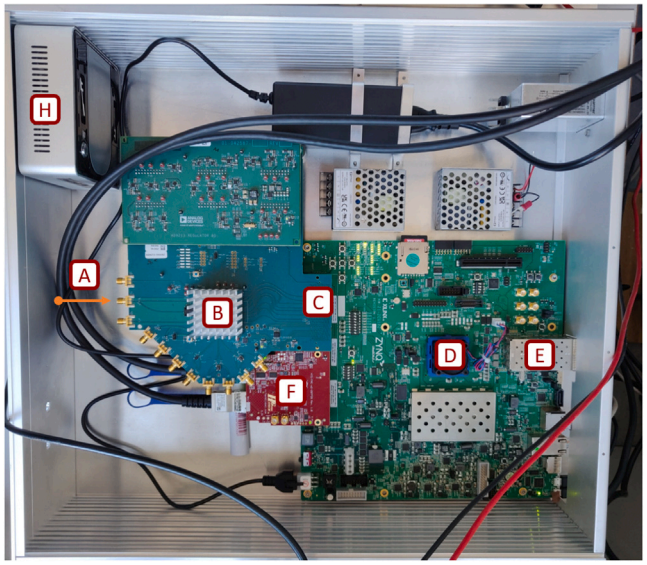

Fig. 3. Physical setup displaying the essential components of the fast digitizer system, with most power supplies and clock-related components removed for legibility. The labels are the same as in Fig. 2 (except **(G)** as the sample clock generator is not visible).

More specifically, the FPGA receives the data and packages it into raw Ethernet frames which are then transmitted over optical fibers to the PC on the fly. The acquisition length is therefore only limited by the total memory in the PC (which can be very large). The computer has entirely standard components, making the system and future iterations robust to changes in PC technology and standards.

3.2. Hardware

The core components currently used in SiCCAF were chosen based on compatibility, availability, development practicality and performances. These components and the associated flow of information will be described in the following with labels going from A to F, as pictured in Figs. 2 and 3. The labels G and H are for the clock control. Fig. 2 is a schematic view and Fig. 3 is a picture of the physical setup, labeled identically.

The analog signal of interest **(A)** is connected to an SMA port onto the ADC. The ADC is Analog Devices' AD9213 mounted on the AD9213-10GEBZ evaluation board **(B)**. This ADC offers up to 12-bit precision over a 1.4 V peak-to-peak dynamic range with a 6.5 GHz analog bandwidth, and a sampling rate up to 10.25 GSa/s. The ADC's data is transmitted on up to 16 JESD204B [28] lanes, each capable of up to 16 Gb/s, all exposed on the furnished FMC+ connector. JESD204 is a high-speed serial interface designed to connect Analog-to-Digital Converter (ADCs) and Digital-to-Analog Converter (DACs) to logic devices, such as an FPGA. As discussed below, we acquire data at 10 GSa/s and 8 bits per sample.

The FPGA is Xilinx's Zynq Ultrascale+ multiprocessor system on chip (MPSoC) XCZU9EG-2FFVB1156 mounted on the ZCU102 evaluation board **(D)**. This MPSoC combines a hard-wired ARM processor and a genuine FPGA on the same silicon die. This means that we can use a readily available Linux operating system to control and debug the programmable logic. This chip is also chosen because it has a sufficient number of multi-gigabit transceivers (MGTs) for both the input data from the ADC (8 MGTs) and the output data to be sent over the network (12 MGTs). The maximum data rate of each MGT is 16.3 Gb/s, although the limit for data entering Xilinx's JESD204 IP core is 12.5 Gb/s (see Firmware in Section 3.3.1). It is equipped with two FMC connectors.

Connecting the ADC to the FPGA poses two challenges:

Mechanical - The ADC board's FMC+ connector is mechanically incompatible with the ZCU102's FMC connectors. Consequently we designed and implemented a custom FMC+/FMC adaptor **(C)** to connect

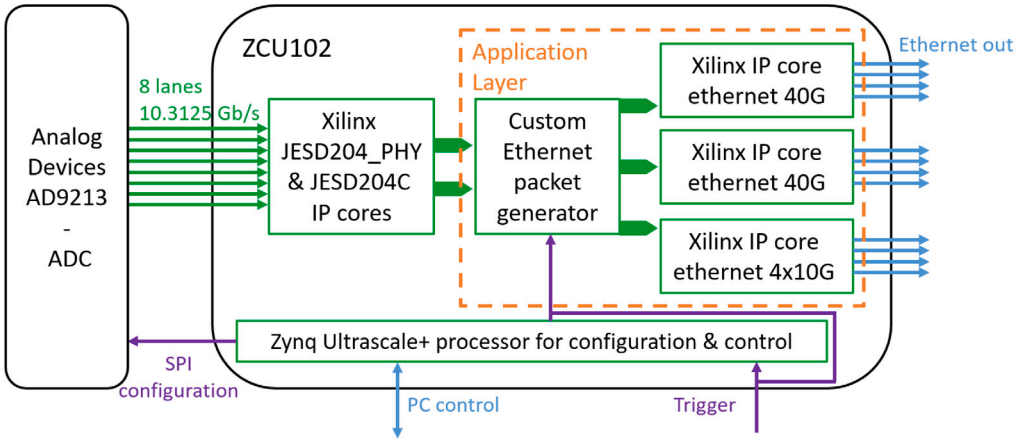

Fig. 4. Simplified block diagram of the control and data flow through the FPGA. The AD9213 is an external hardware component, transmitting data through 8 physical JESD204 lanes. The rest corresponds to the FPGA programming referred to as hardware description language (HDL) blocks, following the JESD204B framework, see text for details.

the two cards. This adaptor also provided a direct JTAG pass-through which was not implemented on our version of the ADC board.

Data transfer - The ZCU102 FMC port is connected to (only) 8 multigigabit transceivers. Consequently we were constrained to using maximally 8 JESD204B lanes. If using the maximum 12-bit precision, the AD9213's hardware is constrained to use either three, six or twelve lanes (where the last option is not feasible because of the ZCU102's 8-lane maximum). The maximum sampling rate at 12-bit precision is therefore 5 GSa/s if also using the ZCU102. However, if the precision is reduced to 8-bit, then all eight lanes can be used. We then implement an acquisition rate of 10 GSa/s corresponding to a line rate of 10.3125 Gb/s due to the JESD204B's 66/64-bit encoding.

The FPGA is receiving 8-bit precision binary data at 10 GHz corresponding to a data rate of 80 Gb/s = 10 GB/s. These data could be stored on the 4 GB of RAM on the ZCU102, corresponding to a maximum acquisition period of 0.4 s. The ZCU102 can also be equipped with an SSD for larger long-term storage, with a PCIe Gen2 x4 slot with maximum data rates at 16 Gb/s. These options are insufficient for our requirements, since a typical AUG discharge duration is ~10 s. Consequently, we need to stream the data to the memory in our acquisition PC simultaneously. We achieve this using six physical interfaces: the ZCU102 has a built-in 4xSFP+ connector **(E)**, and two additional QSFP connections using Hitech Global's HTG-FMC-X2QSFP+ FMC-to-2×QSFP adaptor card **(F)**. Each SFP+ interface can support 10 Gb/s (sometimes referred to as 10G or 10GbE in standard Ethernet nomenclature), while the QSFPs can each support 40 Gb/s transmission speeds. This amounts to a theoretical maximum transfer rate of 120 Gb/s, sufficient to stream the required 80 Gb/s of data, in addition to the overhead of data packaging with a sufficient margin. The choice of SFP/QSFP fiber optic connectors allows data transfer over long distances and between electrically isolated areas.

The acquisition PC uses only standard hardware. It is equipped with three network cards: one Intel Ethernet Network Adapter X710-DA4 with 4 × 10 Gb/s ports (PCIe 3.0 x8) and two Mellanox MCX515A-CCAT 40 Gb/s cards (each PCIe 3.0 x16). The remaining key PC components are the 192 GB of RAM (6 × 32 GB modules) operating at 2933 MHz, and an Intel Xeon Gold 5218 CPU in order to process and receive the data at a sufficient rate. All these components are supported by a Supermicro X12SPA-TF motherboard.

A Texas Instruments (TI) LMX2594EVM board **(G)** generates both the 312.5 MHz clock for the JESD204 blocks on the FPGA and the synchronized 10 GHz (= 32 × 312.5 MHz) ADC clock, to avoid clock drift. This clocking source has rms jitter < 46.9 fs at 10 GHz and is configured via serial peripheral interface (SPI). Direct SPI control is possible but, for ease of use, the SPI instructions are sent via a dedicated TI companion board, the Reference Pro, which is USB controlled. The Reference Pro itself currently has drivers only for Microsoft Windows. A miniature NUC PC **(H)** running that operating system is currently employed for the setup of the clock, which can be replaced by a microcontroller at a later stage. In order to better match the requirements for an external clock supply on the AD9213, additional amplification (Narda Microwave-West's amplifier DBS-0112N210) and band-pass filtering of the 10 GHz signal is needed. These elements are represented in the schematic of the setup in Fig. 2, in the "Sample Clock Generator" block.

3.3. Firmware and software

Here we describe the FPGA firmware running on the ZCU102 labeled as **(D)** in Figs. 2 and 3. This firmware has been developed using Xilinx's Vivado development software and flowchart of its main is shown in Fig. 4. Key elements of the software on the multiprocessor system-on-a-chip (MPSoC) and on the storage PC are also discussed in this section.

3.3.1. Firmware

The data flow through the FPGA starts with the eight physical lanes connected to the ADC. The interface between the two systems follows the JESD204C RX chain standard, illustrated within the first HDL (hardware description language) block of Fig. 4: the JESD204 PHY IP and JESD204C IP cores act as a unit that receives data from the ADC and presents it to the Application Layer. The JESD204 PHY IP core receives 8 streams, each at 10.3125 Gb/s, accounting for the 64b/66b bits data packing.[3] The JESD204C IP core, operating in JESD204B mode, then presents it to the next stage as a bus of data, 256 bits wide (32 times 8-bit samples), clocked at 312.5 MHz.

We have implemented a "JESD204 frame cleaner" that handles any error in each of the 32 samples. This flags errors on a per-sample basis as follows:

- Error-free samples with data value 0 are mapped to data value 1.
- Errors are mapped to data value 0.

This method effectively reduces the valid 8-bit value range to $[1, 255]$, but prevents the propagation of detected errors.

The data are then sent through our custom Ethernet packet generator, which dispatches packets to each of the network interfaces in turn (sending four times more packets to the 40 Gb/s interfaces **(F)** than the

[3] JESD204 [28] permits one of several standard encodings; we chose 64b/66b [29] since it has the lowest overhead: only 3.125% compared to 20% for the earlier 8b/10b encoding, for example.

10 Gb/s interfaces **(E)**). We use jumbo frames in order to exceed the usual Ethernet frame limit size of 1536 bytes per packet [29]. We use raw Ethernet frames rather than a higher level protocol such as UDP since this reduces bandwidth overhead and coding complexity; each network link is (single) point-to-point and so no routing of packets is required. Each packet includes a 256-bit header containing

- The MAC address of the destination as well as the MAC address of the source. This is necessary for correct packet routing on the (virtual) interfaces of the acquisition PC.
- A custom EtherType equal to an arbitrary large offset (e.g. 0x2200) plus a number labeling the interface, which enables us to verify which interfaces on the FPGA side are connected to which interfaces on the PC side.
- The packet number.

The header is followed by 8192 bytes of data (corresponding to 8192 samples or 819.2 ns of data). As data arrive from the ADC, tests have demonstrated that each of the Ethernet interfaces cannot individually stream at the same rate. We have therefore implemented First-in-first-out (FIFO) buffers. While data transfer between the ADC and the FPGA takes place continuously, an acquisition effectively starts when receiving a trigger (physical or software). The trigger is fed as an effective "enable" input to the packet generator: it starts generating packets only once the trigger has been received and does so until a pre-specified number of packets have been generated.

With the ADC and FPGA running on the same clock source (see Section 3.2 label **(G)**), they remain synchronized as long as the JESD204 protocol is running. For synchronization with other diagnostic systems, we rely on their underlying clocks being sufficiently similar, which we estimate provides a synchronicity error of approximately 10 microseconds per second acquisition time. This level of accuracy is sufficient for the vast majority of our intended applications.

On-board real-time processing of the data, before Ethernet streaming and storage, is being considered for further development of this system, and would also be implemented in the Application Layer.

We use Xilinx's tools to generate a `BOOT.BIN` firmware and bootloader file which includes the bitstream, an ARM trusted firmware binary executable, a first stage bootloader, and a U-Boot [30] universal bootloader. This file is stored, in addition to the device tree blob and Linux kernel, onto the bootable partition of an SD card. In the second partition of the SD card, we load the Debian 11 operating system pre-compiled for 64-bit ARM processors.

3.3.2. Software

The software on the MPSoC board consists of code to initialize the ADC via SPI and resetting the various programmable logic blocks.

On the acquisition PC, we configure each of the two 40 Gb/s interfaces as four logical interfaces (with MAC addresses that match the MAC addresses in the custom packet generator described above). Including the 4 × 10 Gb/s interfaces, this results in a total of 12 logical interfaces. To maximize performance, we limit each interface to use a single queue and then map the interrupt associated with each interface to a distinct processor. We collect the data using an instance of `tcpdump` for each interface, locked to the same processor as the interrupt for that interface. We direct the output of `tcpdump` to a ramdisk. Post-acquisition, we then copy the collected data from the ramdisk to NVMe drives. A direct output to NVMe drives, in hardware RAID, is possible but was not pursued due to various incompatibilities, mainly between OS version and motherboard.

3.4. Performance assessment

With the system described in the previous sections, it is possible to achieve acquisitions of around ten seconds, with an 8-bit precision at 10 GSa/s. Such an acquisition fills up 12 million ethernet packets, each containing 8192 samples of data and 32 bytes of metadata (header).

Table 1
Comparison of key metrics for the Data acquisition systems currently installed on AUG, and SiCCAF. The quoted time/frequency resolutions of the fast digitizers assume an FFT window of 8192 samples and the sampling frequency.

		FilterBank	PXIe-5186	SiCCAF
Resolution	Type	Fixed	Tunable FFT (8192 samples)	
	Time	10 μs	0.66 μs	0.82 μs
	Frequency	80–1000 MHz	1.5 MHz	1.2 MHz
Sampling rate		102.4 kSa/s	12.5 GSa/s	10 GSa/s
Bandwidth		10 GHz	5 GHz	5 GHz
Bit-depth		24	8	8 (pot. up to 12)
Max Duty Cycle		100%	6%	100%

The packets are streamed as they are produced with a maximum throughput of 120 Gb/s and fetched on the PC side with `tcpdump` processes, spread over individual CPU cores. Storing these packets in `.pcap` files introduces another 16 bytes of metadata per packet, resulting in under 0.6% data overhead. In total, this procedure amounts to approximately 100 GB of binary data per 10 s acquisition.

Our main goal for such a digitizer is to observe the variation in frequency response of plasmas. The commonly used approach is to piece together spectra over time, thus producing spectrograms. Due to the sheer quantity of data, it is too inefficient to join the packets and to use a moving window. Instead, the packet length ($8192 = 2^{13}$ samples) is chosen for FFT performance. This produces 1 spectrum every 0.82 μs, with 1.2 MHz frequency resolution. These spectra can be pieced together individually for a spectrogram, or displayed with a moving average to increase the Signal-to-Noise Ratio.

During testing of the device, the 12 virtual interfaces each carry one million samples, of which 99.95% are received on average. This number was estimated in nominal conditions (only task running on PC or MPSoC being the acquisition) with a minimum value of 98.7% over 50 acquisition cycles. These rates drop sharply to 50%–70% if other CPU/RAM heavy tasks are running simultaneously on the PC. Out of the received data, consistently around 0.4% of the packets are flagged for containing at least one erroneous 32-byte word by the "JESD204 frame cleaner" mentioned in Section 3.3.1. This negligible portion is unused in the following, due to the difficulty of accounting for 32 contiguous missing samples. In addition, around 40% of the packets contain between one and ten corrupted individual samples, also flagged by the frame cleaner. With all losses considered, in the current nominal case, well over 98% of the data is usable for further analysis.

In comparison to the existing fast digitizer presented in Section 2, used in ideal conditions and in single-channel mode, the new system acquires approximately 15 times more data for a 10 s acquisition. In practice, this can be improved further as experimental conditions rarely allow to use the maximum duty cycle of the existing PXIe-5186. This is due to the fact that it must be operated in short acquisition pulses covering the discharge sparsely, which must be programmed individually to follow the additional constraints of dedicated discharges. Lifting these restrictions with the new digitizer adds up to many times more data acquired, in single-channel mode, without requiring any dedicated planning or programming of the data acquisition scheme. For example, SiCCAF recorded 50 times more data on AUG shot 41537, detailed further in Fig. 7, where the PXIe-5186 acquired 634 pulses of 0.5 ms per channel at 6.25 GSa/s (manually planned, maxing out the memory usage). A summary of the performance of the existing digitizers presented in Section 2 and of SiCCAF is shown in Table 1. For most metrics, the PXIe-5186 and SiCCAF are comparable, with the improvement in duty cycle being the core reason to develop a new continuous digitizer.

Looking further, the modular design of the ADC+FPGA setup can be carried over to upgraded setups with limited additional development time. Currently, an improved system with a different FPGA is being developed to achieve 12-bit precision (16 times better resolution, 50% more data) at the same rate.

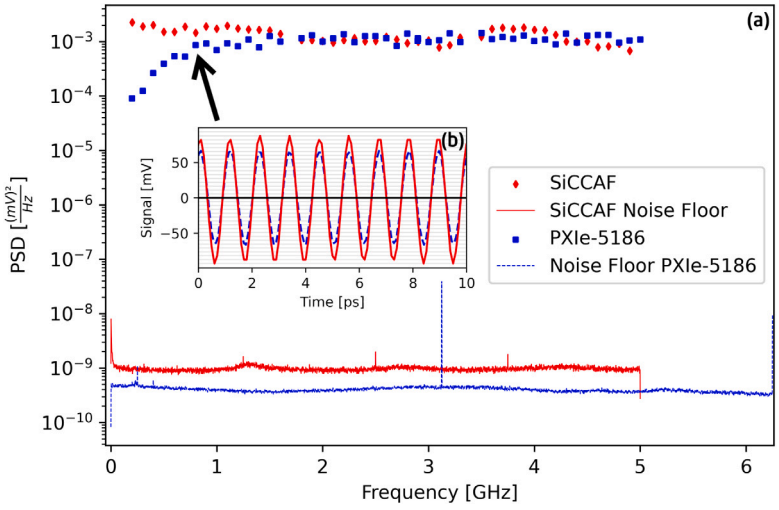

Fig. 5. (a) Frequency response in log scale to an imperfect single-frequency source for both digitizers. The sets of (*highest-peak-power, frequency*) points are scattered for both systems, giving a power distribution per frequency step. Missing data below 100 MHz and gaps at 1.7 GHz and 3.4 GHz are due to the signal generator being unable to produce a stable signal during the sweep. No error bars are shown, as they would be smaller than the markers shown. (b) Example of the raw sampling of an 800 MHz sinusoidal signal for both systems, using the same colors. SiCCAF's signal is converted from unsigned 8-bit integers (uint8) to volts with a 1.4 V dynamic range, while the PXIe-5186 uses signed int8 over 0.8 V.

4. Calibration procedure

The full calibration procedure consists of two steps: a preliminary assessment, presented below, and an absolute calibration. The absolute calibration will be carried out routinely during operation, using a well-established hot-cold source technique to relate measured black-body spectra to radiation temperature [6,31]. The preliminary assessment performed here was a cross-calibration to the previous digitizer – the NI PXIe-5186 – using a signal generator. This allowed to assess general performance and identify any discrepancies between the devices.

The cross-calibration consisted in generating a single-frequency signal swept across the whole 5 GHz bandwidth and splitting the output into each fast digitizer. Here, the single-frequency source was a Rohde and Schwarz SMR20 (R&S) microwave signal generator. To cross-calibrate the frequency response of both digitizers, a frequency sweep was conducted in 100 ms steps at a given frequency, from 10 MHz to 5 GHz in 100 MHz increments. A full sweep was recorded continuously by the FPGA over ten seconds. For the PXIe-5186 digitizer, this configuration allowed up to two 0.5 ms acquisition pulses per 100 ms step, after the signal generator stabilized. For a perfect signal generator, the frequency spectrum should contain a single peak at a constant level, which, in reality, varied in power and was accompanied by various low level harmonics and noise. Therefore, for each spectrum, the value of the highest peak and its frequency were recorded. The resulting power spectrum density (PSD) peak value against frequency is shown in Fig. 5, with an example of the signal read by both digitizers at low frequencies, where the sampling rate allows to visualize and compare the sinusoid clearly.

At low frequencies, the older system was known to be less sensitive and the response of SiCCAF was much flatter. Minor discrepancies arrived at higher frequencies, as the ADC got closer to its Nyquist frequency (5 GHz) than the PXIe-5186 did (6.25 GHz). This is of little concern as such response differences will be routinely calibrated out during the second phase of the calibration process. Both devices clearly observe and record the same signal, with a different frequency response.

In addition, a simple linearity test of the new digitizer was performed by feeding it a strong signal and progressively adding attenuation. The results are shown in Fig. 6. The peak response of the new digitizer remained perfectly linear across all frequencies for well resolved signals, *i.e.* of amplitude above the two-bit resolution $2\delta_{res}$

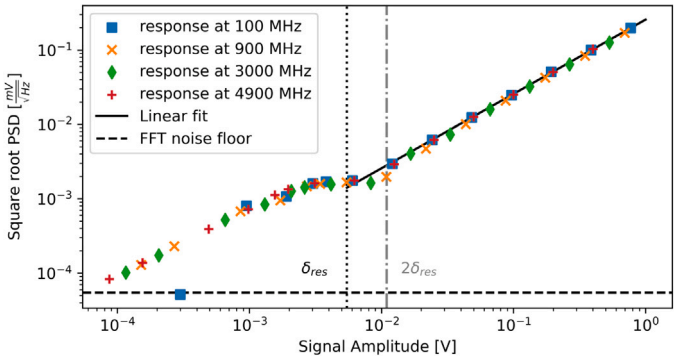

Fig. 6. Square root of the highest peak in the PSD at given frequencies, as a function of the source signal amplitude. To account for frequency dependence due to the R&S source signal, cable response and digitizer response (shown in Fig. 5), the highest voltage measured at each frequency was used as reference (6 dB difference between 100 MHz and 4.9 GHz). All other values on the abscissa are calculated based on the added attenuation, previously verified to be flat across this frequency range. $\delta_{res} = 5.4$ mV is the voltage resolution of SiCCAF. For visual guidance, in the region of interest (above δ_{res}), a linear function passing by 0 and the point of highest signal amplitude is plotted in black.

(with a bit-depth of 8, the smallest voltage step resolved is $\delta_{res} = 1.4\text{V}/2^8 = 5.4$ mV). Furthermore, above 100 MHz, these monochromatic signals could be attenuated further by a factor 40 dB below the bit-resolution (*i.e.* down to 50 μV amplitude) and were still clearly visible in the FFT of each packet. However, other peaks in the noise floor start becoming comparable in size at these levels, as shown in Fig. 5, corresponding to a conservative value of $3{\cdot}10^{-9}\ \frac{(\text{mV})^2}{\text{Hz}}$ for the noise floor. It must be noted that, with weak signal levels and in the presence of a comparably low noise (both $\lesssim \delta_{res}$), we observe a behavior similar in appearance to gain-compression but without any saturation: the noise floor in FFTs appears lower than its value without any signal, as is expected from Parseval's theorem [32]. Values above 0.8 V amplitude could not be obtained at these frequencies due to the signal generator becoming unstable. Although voltages up to saturation were not tested, the digitizer is responding linearly up to at least 1.2 V (not shown here).

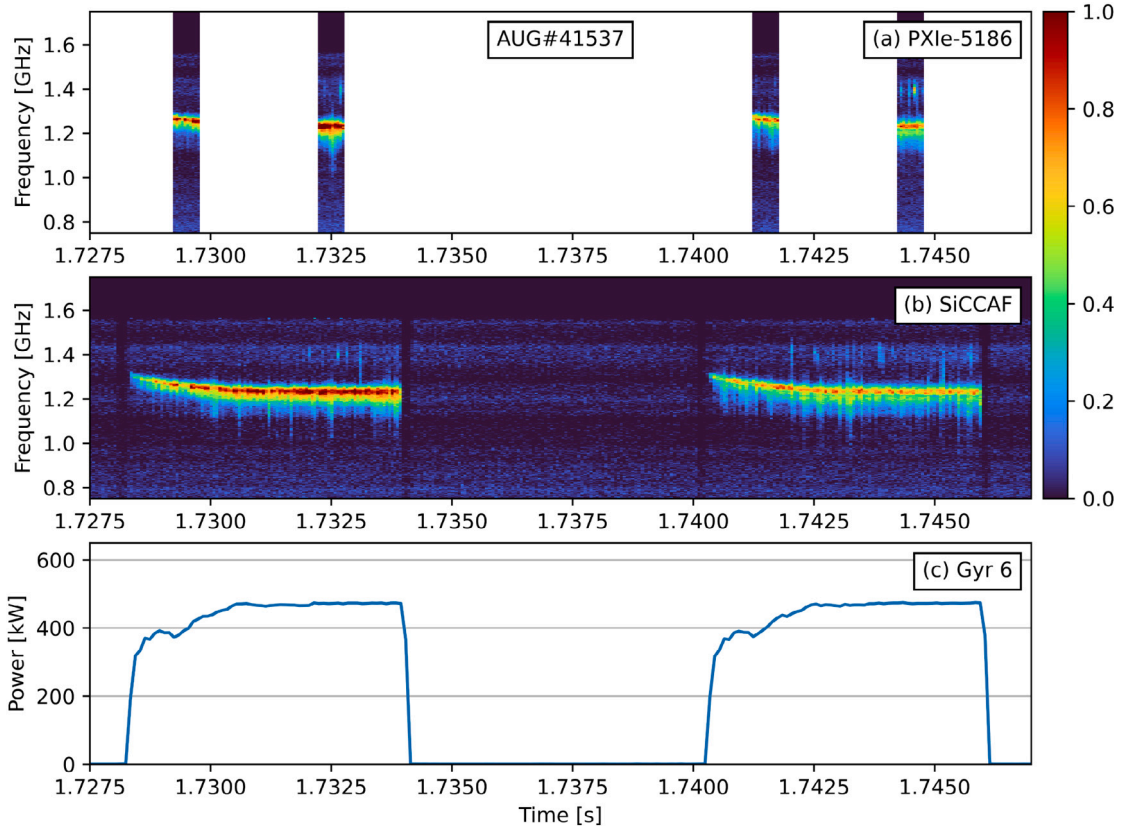

Fig. 7. (a) and (b): Uncalibrated spectrograms of the direct input to both digitizers after down-conversion, sampling the same signal in AUG discharge 41537, synchronized to the global AUG clock for $t = 0$. Four 0.5 ms pulses of the PXIe-5186 (a) are acquired, compared to SiCCAF (b) on the same logarithmic scale in spectral power density [a.u.] between 0.75 GHz and 1.75 GHz. In both cases, each spectrum (vertical slice) is averaged over 40 μs for readability. This data was acquired in an early development stage, thus explaining the minor discrepancies between the two digitizers. White color represents an absence of data. The signal appears correlated with the digital power modulation of gyrotron 6 (c), at 140 GHz, the only gyrotron firing at the time.

5. Experimental results

Measurements from a plasma discharge at ASDEX Upgrade are presented in Fig. 7. These highlight the significant improvement of the new FPGA-based system over the previous digitizer, from a continuous acquisition point of view. We show the plasma response down-converted in two stages, with a second-harmonic mixer at $2\times97.4 = 194.8$ GHz and regular mixer at 14.8 GHz, during digital modulation (on/off pulses) of heating gyrotron 6 injecting power at 140 GHz. Full analysis of these data will be presented in a forthcoming publication. A signal mimicking the characteristic downwards chirping of the gyrotron during the "on" phase of its modulation is clearly visible on the continuous spectrogram. Without prior knowledge, the sparse time windows acquired by the old system would make such a chirp much harder to infer.

Another measurement at Wendelstein 7-X, shown in Fig. 8, highlights further the benefits of a continuous acquisition, with an unknown and previously unobserved signal above 174 GHz. All heating gyrotrons are using 140 GHz, and gyrotron B1 was used as a CTS probe at 174 GHz, firing in 10 ms blips. The effects of the active frequency stabilization of gyrotron B1 [33] can be seen in Fig. 8(c), compensating the thermal expansion of the resonator after a few milliseconds of firing. As no gyrotron was firing at that frequency throughout most of the 2 s shown here, no signal was expected when B1 was off. Thus, the short available record time of the PXIe-5186 was better used around the gyrotron blips, 2 ms on/2 ms off for background subtraction. However, a clear signal can be observed at a higher frequency (see Fig. 8(b), which does not appear to be clearly correlated with any gyrotron. This signal, currently under investigation, is also visible in the PXIe-5186 spectra, although very hard to distinguish from noise, and would not have been identified if not for the capabilities of SiCCAF.

6. Conclusion and outlook

The continuous acquisition of data is essential to maximize the scientific returns for each discharge observed by any microwave diagnostic. Furthermore, the observation via fast digitizers of a wider bandwidth will allow detailed observation of currently unexplored physics, with clear prospects for the CTS diagnostic in the domains of fast-ion dynamics and PDI analysis. To achieve this, we have developed a novel FPGA-based fast digitizer (SiCCAF) at a very competitive cost per bandwidth, and equipped it on the CTS system on AUG and on W7-X. Here, we have presented the hardware specifications and critical aspects of the software programming necessary for the digitizer to operate, with some examples of the first results obtained. In its current state, our system can achieve continuous digitization for up to 10 s at 10 GSa/s, with an 8-bit precision and over an analog bandwidth of 5 GHz. The ADC/FPGA combination allows continuous streaming of all data with a throughput up to 120 Gb/s. This constitutes a vast improvement over the pre-existing setup, for which the current base usage allowed a nominal duty cycle $\leq 6\%$ of the total discharge time. The additional data obtained by the new setup facilitates a significant part of the discharge acquisition planning, avoids missing critical data due to the sparsity of the acquisition, and can furthermore be used to increase the signal-to-noise ratio or the frequency resolution.

In addition, the inherently flexible nature of our system allows on-the-fly performance upgrades, such as improving the total acquisition time by increasing the PCs RAM, for example. Hardware upgrades, which can be implemented with limited additional development time, are already being considered for exploiting the full capacity of the AD9213 digitizer and increasing the acquisition precision to 12 bits. In the future, the additional computing power offered by the FPGA can

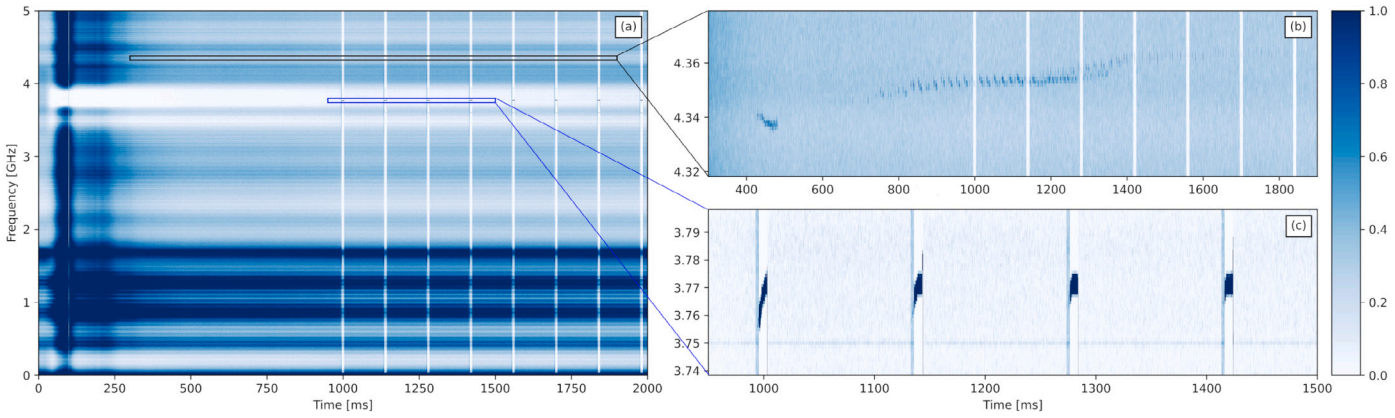

Fig. 8. (a) Uncalibrated spectrogram of the direct input to SiCCAF after downconversion from 170 GHz in Wendelstein 7-X shot 20230330.23. Each spectrum (vertical slice) is averaged over 250 μs. Thin vertical white lines correspond to the PIN-switch attenuation reducing the signal when gyrotrons start or stop. Wider vertical bands starting from 1.0 s are an example of the "Parseval background compression" when gyrotron B1 is firing at 174 GHz, due to insufficient amplification during this shot. (b) Zoom on the unexpected signal observed. (c) First four gyrotron B1 blips, with the frequency stabilizing after the first 2.

also be used to perform a wide array of tasks, among which real-time FFT processing and averaging, paving the way for CTS-based real-time analysis and control of fusion plasmas.

CRediT authorship contribution statement

T. Verdier: Writing – review & editing, Writing – original draft, Visualization, Validation, Supervision, Software, Resources, Project administration, Methodology, Investigation, Funding acquisition, Formal analysis, Data curation. **R.G.L. Vann:** Writing – review & editing, Visualization, Validation, Software, Resources, Methodology, Investigation, Funding acquisition, Conceptualization. **A.S. Jacobsen:** Software, Investigation, Conceptualization. **T. Jensen:** Resources, Investigation. **J. Rasmussen:** Writing – review & editing, Validation, Supervision. **R. Ragona:** Resources, Investigation. **S.K. Nielsen:** Writing – review & editing, Supervision, Resources, Project administration, Methodology, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Theo Verdier reports financial support and travel were provided by European Consortium for the Development of Fusion Energy. Theo Verdier reports equipment, drugs, or supplies was provided by Xilinx Inc. Stefan Kragh Nielsen reports financial support was provided by Villum Foundation. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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