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PCB busbar optimization for distributed DC link capacitors and parallel discrete SiC MOSFETs

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***Abstract*—Commutation loop inductance is critical in the design of high-power density power electronic converters that employ fast switching Silicon Carbide (SiC) MOSFETs as it impacts the losses and voltage/ current stresses on the devices and thereby the overall reliability of the converter. This inductance is influenced by the DC link capacitance layout and the relative placement of the DC link capacitors and power devices. In this paper, a distributed DC link capacitor layout strategy that minimizes the commutation loop inductance is investigated. The principle of flux cancellation is utilized in designing the PCB busbar board. The layout scheme is analyzed using ANSYS Q3D and the resulting inductance contributed by the DC link to the commutation loop is estimated. The above analysis is validated both through simulations and double pulse test results. Additionally, the arrangement of paralleled power devices in a half bridge is analyzed using ANSYS Q3D with the objective of improving the current sharing.**

I. Introduction

Layout optimization is a critical contributing factor in design of high-power density power electronic converters employing wide band gap devices. [1], [2] present optimization of commutation loop for SiC power modules. While [1] investigates the design of PCB busbar considering the role of decoupling capacitors when 1.2kV devices are used, [2] details out the commutation loop minimization strategy for 1.7kV SiC power modules-based converters. In [3], the PCB busbar for discrete devices is optimized by providing slots that improve current sharing in parallel SiC MOSFETs, while [4]-[7] optimizes parasitic inductances in GaN based converters. In [8],[9], a capacitor interconnect strategy with flux cancelling between the capacitor and PCB layer is presented. In this paper, a concept of distributed DC link capacitance along with paralleled MOSFETs is considered for the design of 40kW SiC inverter operating at 120^0C ambient for an actuator system. Various layout constraints, considering the unique envelope, that can affect both the commutation loop inductance and current sharing in parallel devices are analysed through ANSYS simulations and design decision were outlined.

II. Inverter Design Plan: Envelope & Components

Considering an 800V, 40kW design, 1.2 kV SiC MOSFET options having a junction temperature of around 175^0 C were explored and C3M0016120K from Wolfspeed was chosen considering its low $R_{DS\text{-}ON}$ and 4 – pin package with Kelvin source that decouples gate drive to source inductance and thereby reducing the switching time and switching losses. To further reduce the semiconductor losses, paralleling of MOSFETs was considered with three devices in parallel. Ceramic capacitors were chosen for DC link due to its better thermal capacity. Fig. 1(a) shows the PCB envelope that is to be shared by two inverter PCBs. The available annular envelope is then divided into high voltage (DC link capacitors, power semiconductors, current sensors) and low voltage areas (gate drivers and control circuitry) with gate drivers providing the isolation as shown in Fig. 1(b).

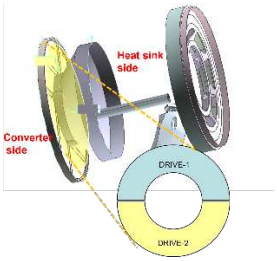

Fig. 1(a): Envelope of inverter

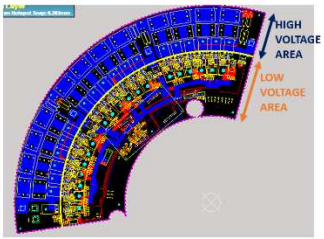

Fig. 1(b): Separation of high & low voltage areas on PCB

III. PCB Busbar Layout Optimization

A. Distributed DC link capacitors and power semiconductors

Several key factors need to be considered such as minimal commutation loop inductance, that reduces the voltage spike induced across the drain – source of the MOSFET and thereby the loss, minimal gate loop inductance that reduces the unwanted ringing in the gate voltage and avoids device failure, equal sharing of currents by devices in parallel that influences the relative placement of the DC link capacitors, and MOSFETS along with the gate drivers. Considering these factors, the capacitors and power devices are symmetrically distributed. It is ensured that the three phases are identical to each other, with the DC capacitors localized to power devices of each phase maintaining symmetry as well as minimized commutation loop.

B. DC link layout planning

Fig. 2(a) shows the positioning of the DC link capacitors in one phase. Since each ceramic capacitor is rated for 500V, two in series are needed for 800V and four such combinations are paralleled. The outer (top and bottom) layers are assigned for

DC+ while the internal layers are assigned for DC- and DC/2 potentials. This ensures that the adjacent layers carry currents in opposite direction causing flux cancellation and reduced commutation loop inductance. The side view of individual layers along with the flux cancellation is shown in Fig. 2(b).

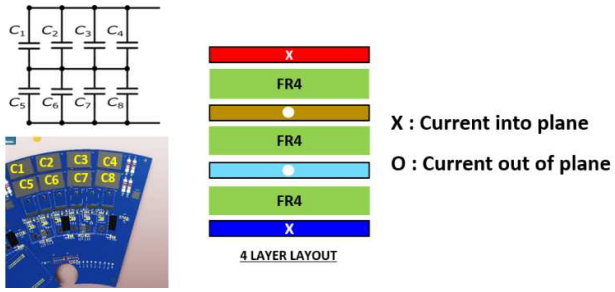

Fig. 2(a): Capacitor placement on PCB and current directions in 4 layers of distributed DC link layout

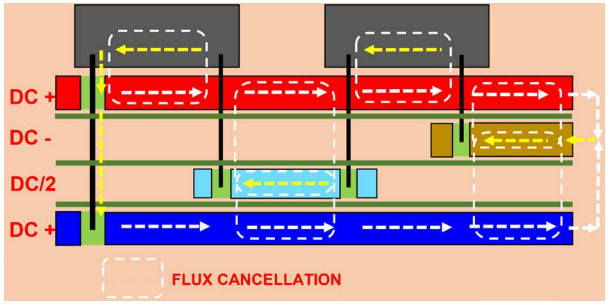

Fig. 2(b): Lateral view of capacitor currents in all 4 layers of PCB busbar

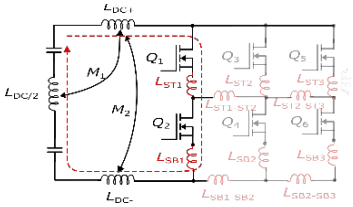

Fig. 2(c): Equivalent circuit of commutation loop considering one parallel branch

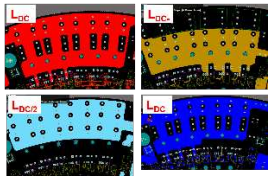

Fig. 2(d): Distribution of DC link layout across 4 layers

Fig. 2(c) shows commutation loop inductance of one of the parallel branches (highlighted). From Fig. 2(c), the equivalent loop inductance seen by the branch formed by MOSFETs Q1 and Q2 is given as $L_{comm} = L_{DC+} + L_{DC-} + L_{DC/2} + L_{ST-1} + L_{SB-1} - M_1 - M_2$, where M_1, M_2 are mutual inductance between DC+ layer and DC/2 ,DC- layers respectively. Fig. 2(d) shows the optimized outer and inner layers of PCB busbar of distributed DC link. Using ANSYS Q3D, the commutation loop inductance formed by the devices Q1, Q2 and the distributed capacitance was estimated to be 67nH. From the double pulse test results at 390V/22A, the turn off voltage overshoot across Q1 was around 450V (390V + 60V) at a current slope of 1A/ns as shown in Fig. 3. The estimated overshoot $L_{comm.}\frac{di_d}{dt}$ is 67V, which validates the ANSYS simulation.

C. *Parallel device arrangement: Layout considerations*

The paralleled power devices of high side switch position in a phase leg are placed together followed by the devices constituting the low side. This ensures minimal asymmetry in source inductance between paralleled devices which improves current sharing while reducing the gate – kelvin loop lengths. The comparison of both arrangements is shown in Fig. 4. Using ANSYS Q3D, the maximum difference between paralleled MOSFETs (Q1 – Q3) as per placement – 1 scheme is 20nH, while as per placement – 2 scheme is 40nH. This is due to the doubling of parasitic inductance components $L_{ST_1-ST_2}$ and $L_{ST_2-ST_3}$ in Fig. 2(c).

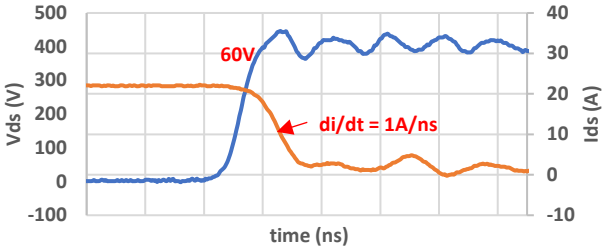

Fig. 3 Turn OFF voltage and current waveforms at 390V/22A

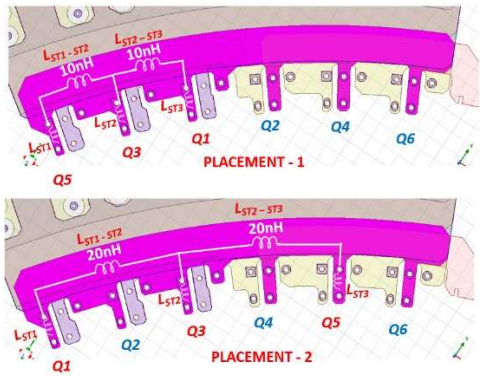

Fig. 4: Comparison of placement styles of parallel MOSFETs (high side MOSFETs compared)

IV. Conclusions

In this paper, the distributed DC link PCB busbar optimization using ceramic capacitors for an 800V, 40kW inverter is investigated. Multilayer strategy that causes flux cancellation and thereby minimized commutation loop inductance is proposed and analyzed through ANSYS Q3D simulations. To experimentally verify the simulation result, a double pulse test is performed on the experimental layout and the voltage overshoot is verified. Additionally, the possible options of placing the SiC MOSFETs in parallel were investigated. The analysis shows that placing the high side and low side devices together instead of the alternate arrangement results in lesser source inductance difference between paralleled MOSFETs which enhances the current sharing.

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