

# A simplified consensus-based distributed secondary control for battery energy storage systems in DC microgrids

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## ABSTRACT

DC microgrids have become a promising solution for efficient and reliable integration of renewable energy sources (RESs), battery energy storage systems (BESSs) and loads. To simultaneously achieve average voltage regulation, accurate current-sharing and state-of-charge (SoC) balance, at least two state variables need to be transmitted between neighboring BESS nodes in conventional distributed secondary control. In this paper, a simplified consensus-based distributed secondary control for BESSs in DC microgrids is proposed with only one virtually defined state variable being transmitted, where a cascaded control framework consisting of an SoC controller and a voltage controller is used to regulate DC bus voltages. This virtual state variable combines BESS SoC and its converter output current, there is no need to change the control law when BESSs switch between charging/discharging modes. Once SoCs are balanced, SoC controller works as a current controller. With the proposed control strategy, the number of transmitted state variables and the complexity of controller design are significantly reduced. Stability and steady-state analysis are also conducted to confirm the effectiveness of the proposed control strategy. Finally, Simulink simulation and hardware-in-loop tests are presented to validate the proposed control strategy.

## 1. Introduction

Due to the increasing demand for electricity, compounded by the pressing need for addressing the environmental pollution and carbon emission challenges due to substantive consumption of fossil fuels in all sectors, distributed energy resources (DERs) using renewable energy sources (RESs), and battery energy storage systems (BESSs) have been intensively researched [1]. The microgrid has been widely recognized as an effective means to integrate the RESs, BESSs and loads [2]. Microgrids can generally be grouped to AC microgrids and DC microgrids, the latter is drawing much attention as they can more effectively and efficiently interface with various DC sources and loads, such as photovoltaics (PVs), electric vehicles (EVs), BESSs [3]. Furthermore, compared with AC microgrids, DC microgrids have no need for frequency control and harmonics cancellation, and no requirement for synchronization, etc [4], which makes them a more attractive solution in many application scenarios. Even without suffering from the aforementioned issues of AC microgrids, DC microgrids still need be controlled properly. The control objectives of DC microgrids often include average voltage regulation, current-sharing between different DERs, state-of-charge (SoC) balance and avoidance of overcharging

and over-discharging of BESSs if multiple BESSs are connected to the DC microgrids [5]. To achieve these control objectives, various control strategies have been proposed, which can be categorized as centralized, decentralized and distributed control [6]. In centralized control, a microgrid central controller (MGCC) monitors entire system and dispatches loads and DERs. However, MGCC often suffers from heavy computational burden and single-point-failure issues [7]. While the droop control is a typical and widely used decentralized control strategy, it makes decision only using local information, hence the aforementioned shortcomings are addressed. In the droop control, output voltage linearly decreases as output current increases, DC microgrids achieve automatic voltage regulation and current-sharing based on this principle [8]. Furthermore, SoC information sometimes is also integrated into the droop control to achieve SoC balance, e.g., Lu et al. set the droop coefficient proportional to the  $n$ th order of SoC in the charging process, while set it inversely proportional to the  $n$ th order of SoC in the discharging process [9,10]. Li et al. dynamically changes the reference voltage of droop control according to SoC [11]. However, the droop control has an inherent challenge for the trade-off between the voltage regulation and current-sharing [12,13].

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To restore the voltage droop introduced by the droop control and achieve accurate current-sharing between DERs, the distributed secondary control is widely used. In the single DC bus system, the measured common DC bus voltage is sent to DERs as feedback for voltage restoration [14]. In the multiple DC buses system, the controller design is more complex where the average voltage of individual DC buses needs to be calculated for global voltage restoration. Ref. [15] proposed a dynamic consensus protocol (DCP) based distributed secondary control, where the average voltage is obtained with an average voltage observer, and both the average voltage observer and current controller are designed based on the consensus algorithm. In the DCP-based distributed secondary control, DERs only communicate with their neighboring DERs and only a sparse communication network is needed for average voltage/SoC estimation, and current controller design. Thus, new distributed secondary control strategies have been proposed. These control strategies can be divided into two groups, the first is voltage-shifting-based control, and the second is voltage-shifting-and-slope-adjusting-based control.

In the voltage-shifting-based control, the reference voltages for DERs are shifted according to the voltage regulation and power flow requirement while the droop coefficients are kept fixed. Zhou et al. proposed a resilient controller to enhance the controller resilience against time delays and disturbances, the SoC balance of BESSs is not considered [16]. A novel secondary optimal control for multiple BESSs in DC microgrids is proposed, where a distributed optimal voltage controller is used and its convergence is independent of time delay [17]. Zhang et al. proposed a distributed secondary controller with three voltage shifting terms, the dynamic SoC equilibrium and accurate current distribution are realized by the consensus iteration of the designed coupling factor, and the bus voltage recovery is achieved by compensating for the average output voltage [18]. Zeng et al. proposed a distributed unified controller for parallel BESSs in DC shipboard microgrids [19], where a dynamic diffusion algorithm is used for average information estimation. In their follow-on two publications, two voltage-shifting terms are produced based on three state variables for power flow regulation and average voltage regulation [20,21]. Shafiee et al. presented a distributed hierarchical control framework to ensure the reliable operation of DC microgrids, the SoC mismatch between neighbors is passed through a PI controller to adjust the power flow [22]. Chen et al. proposed a distributed cooperative secondary control for batteries in DC microgrids, a state variable related to the battery SoC is defined and it varies when BESSs switch between charging and discharging modes to achieve SoC balance [23,24]. Zhang et al. proposed a novel distributed multi-agent finite-time control strategy with time delays for the SoC balance and average voltage restoration in DC microgrids with distributed BESSs, where a feedback linearization technique is used to obtain a second-order consensus strategy for SoC [25]. Mi et al. proposed a multiagent dynamic-tracking-consensus-protocol-based on the random packet loss model to estimate the global information for the dynamic network with lossy communication [26]. Then the adaptive current sharing algorithm is designed to balance the SoC for BESSs with different capacities.

In the voltage-shifting-and-slope-adjusting-based control, both the reference voltage and droop coefficients for DERs are dynamically adjusted. Xu et al. proposed a double-quadrant SoC consistent adaptive droop control, and the average voltage is observed by the DCP-based average voltage observer [27]. Similarly, Zhang et al. proposed a distributed secondary control framework, where the droop coefficients of BESSs are adjusted according to average SoC value and a new state variable is defined to eliminate the influence of insistent line resistance and DC bus voltage recovery [28]. Sahoo et al. proposed a distributed optimal voltage controller for voltage recovery against transmission delay, SoC balance and smooth mode transition to constant power charging are obtained by adjusting droop coefficients with SoC [29]. In [30], the voltage droop on the droop coefficient and its integration are used as two state variables for voltage recovery under time delay,

and the droop coefficients are adjusted according to battery SoC. Hu et al. proposed a secondary control strategy with four controllers, including a current-sharing controller, an SoC balance controller, a virtual impedance correction controller, and a local reference voltage controller, they collectively achieve voltage regulation and SoC balance [31].

It is well-acknowledged that the transmission delay will introduce steady-state error and even make the whole system unstable. The control strategies considering the transmission delay have been intensively researched. Besides the control strategies in [16,25,26], a distributed optimal voltage controller is used in [17,29,30] for effective average voltage regulation against time delay, where the voltage is regulated by solving the optimization problem in a distributed way. Yu et al. proposed a consensus-based proportional-integral predictive control strategy, which can actively compensate for communication delays and consecutive packet dropouts encountered by DC microgrids through the established physical model, rather than passively tolerating communication delays [32]. To cope with the communication induced time delay and attackers, a new time-varying sampling period and an improved communication mechanism are first introduced within the sampling control framework, and a resilient secondary controller is designed Based on them in [33]. Further, some event-triggered-based control strategies are proposed to achieve consensus under time delay [34].

The name and number of transmitted state variables in the aforementioned control strategies are summarized in Table 1, where  $X_{avg}$  represents the observed average value with the average observer in [15], e.g.,  $v_{avg}$  is the observed average voltage,  $i_{o,avg}$  is the observed average converter output current.  $R_{dr}$  is the droop coefficient. These control strategies have the following disadvantages: Firstly, at least two or three state variables are transmitted for generating the voltage regulation term and power flow adjusting term to achieve average voltage regulation, accurate current-sharing and SoC balance, which increases the communication burden and complexity of controller design. Secondly, there may be a conflict between the voltage regulation term and the power flow adjusting term, and the coordination between the two terms is not elaborated by the authors, especially in the situation where one of the control objectives is forced to be abandoned when individual DC bus voltages reach to limit. Thirdly, some state variables are designed to be very complex and are changed when BESSs switch between charging/discharging modes, like the control strategies in [21, 23,24]. To overcome these disadvantages, a simplified consensus-based distributed secondary control for BESSs in multiple DC bus microgrids is proposed in this paper. The main contributions of this paper are summarized as follows:

- (1) A cascaded control framework consisting of an SoC controller and a voltage controller is proposed with the information of only one virtually defined state variable being transmitted, which is kept unchanged when BESSs switch between charging/discharging modes. Thanks to the virtual state variable and simplified controller design, the response of state variables can be easily inferred from the transfer function.
- (2) Not only the average voltage is regulated, but the voltage deviations between individual DC buses and nominal value are also constrained by setting a voltage deviation limiter in the proposed SoC controller. The average voltage regulation will be canceled automatically and only power flow regulation will be enabled when the individual DC bus voltages reach to their upper/lower limit.
- (3) The stability analysis and steady-state analysis of the system considering time delays are conducted with the proposed control strategy.

The remainder of this paper is organized as follows. Section 2 presents the problem formulation and control objectives. Section 3 details the proposed distributed secondary control. The system stability and steady-state analysis are presented in Section 4. The simulation and hardware-in-loop (HIL) test results with the proposed control strategies are detailed in Section 5. Finally, Section 6 concludes the paper.

**Table 1**  
Comparison between existing methods.

Existing methods	Name and number of exchange state variables	Definition of some exchange state variables
Zhou et al [17]	$v_u / \int v_u dt / i_o$ 3	$v_u$ is average voltage regulation term
Zhang et al [18]	$v_{avg} / \text{SoC}_{avg} / \kappa_{avg}$ 3	$\kappa$ refer to [18]
Zeng et al [19]	$\chi / \text{SoC}$ 2	$\chi = \left(1 - \frac{\Delta u}{\Delta u_{max}}\right) v_{bus}, \Delta u = R_{dr} i_o$
Zeng et al [20]	$v_{avg} / \text{SoC}_{avg} / k_{avg}$ 3	$k = i_o / C_b \exp\left(\frac{\text{sgn}(i_o)(\text{SoC}_{avg} - \text{SoC})}{ \text{SoC}_{avg} - \text{SoC}  + \epsilon}\right)$
Zeng et al [21]	$\Delta u_{avg} / i_{o,avg} / \text{SoC}_{avg}$ 3	$\Delta u = i_o R_{dr}$ $R_{dr} = \begin{cases} \frac{R_{dro}}{C_b} [1 + \text{SoC}_{avg} - \text{SoC}]^\epsilon & i_o \geq 0 \\ \frac{R_{dro}}{C_b} [1 + \text{SoC} - \text{SoC}_{avg}]^\epsilon & i_o < 0 \end{cases}$
Shafiee et al [22]	$v_{avg} / \text{SoC}$ 2	\
Chen et al [23,24]	$v_{avg} / x$ 2	$x = i_{load} v_{bus} / F_{\text{SoC}}$ $F_{\text{SoC}} = \begin{cases} \text{SoC} - \text{SoC}_{low} & i_o \geq 0 \\ \text{SoC}_{high} - \text{SoC} & i_o < 0 \end{cases}$
Zhang et al [25]	$v_{avg} / \text{SoC} / \text{SoC}$ 3	$\text{SoC} = \frac{d\text{SoC}}{dt}$
Mi et al [26]	$v_{avg} / \text{SoC}_{avg} / i_{o,avg}$ 3	\
Xu et al [27]	$v_{avg} / \text{SoC}$ 2	\
Zhang et al [28]	$\xi_{avg} / \text{SoC}_{avg}$ 2	$\xi = \left(1 - \frac{\Delta u}{\Delta u_{max}}\right) v_{bus}, \Delta u = R_{dr} i_o$
Shahoo et al [29]	$v_u / \int v_u dt / \text{SoC}$ 3	$v_u$ is average voltage regulation term
Huang et al [30]	$R_{dr} i_o / \int R_{dr} i_o dt / \text{SoC}_{avg}$ 3	\
Hu et al [31]	$\text{SoC} / i_o / R_{dr,avg}$ 3	\
The proposed control strategy	$\rho$ 1	$\rho = i_o / C_b - \theta \text{SoC}$

## 2. Problem formulation and control objectives

### 2.1. Configuration of DC microgrids

The configuration of DC microgrids used in this paper is illustrated in Fig. 1, which consists of  $N$  DC buses, where each DC bus is connected with a BESS, a RES and a resistive load. Each BESS is connected to the DC bus through a DC–DC converter, and converters are operated at voltage control mode to support DC bus voltage, the DC buses are linked through tie-lines. Besides, the resistive loads absorb power from the microgrids while the RESs generate power for the microgrids.

### 2.2. Electric network model

In Fig. 1,  $v_{busi}$  represents  $i$ th DC bus voltage,  $i_{oi}$  is the  $i$ th converter output current, which is positive when BESS is discharging, while negative when the BESS is charging. Based on the Kirchhoff's law, the voltage and current relationship of whole system can be expressed as follows

$$i_o + i_{\text{RES}} = Y v_{\text{bus}} \quad (1)$$

where  $v_{\text{bus}} = [v_{bus1}, v_{bus2}, \dots, v_{busN}]^T$  is the DC bus voltage vector,  $i_o = [i_{o1}, i_{o2}, \dots, i_{oN}]^T$  is the converter output current vector.  $i_{\text{RES}} = [i_{\text{RES}1}, i_{\text{RES}2}, \dots, i_{\text{RES}N}]^T$ , where  $i_{\text{RES}i}$  is the RES current fed into  $i$ th DC bus.  $Y$  represents the nodal admittance matrix of DC microgrids, and it

can be calculated according to

$$Y_{ij} = \begin{cases} y_i + \sum_{j \in N_i^c} y_{ij} & \text{if } i = j \\ -y_{ij} & \text{if } i \neq j \end{cases} \quad (2)$$

where  $N_i^c$  denotes the set of DC buses which are electrically connected to the  $i$ th bus,  $y_i$  is the admittance of resistive load connected to the  $i$ th bus,  $y_{ij}$  is line admittance between the  $i$ th bus and the  $j$ th bus, these elements are none zero only when the corresponding buses are physical connections.

### 2.3. Primary droop control and control objectives

In DC microgrids, the droop control is widely used due to its simplicity and effectiveness. In the droop control, the converters are controlled at voltage mode to support DC bus voltage, and the reference of DC bus voltage decreases with converter output current

$$v_{refi} = v^* - R_{dri} i_{oi} \quad (3)$$

where  $v^*$  is the nominal DC voltage,  $v_{refi}$  is the reference of DC bus voltage and  $R_{dri}$  is the droop gain for the  $i$ th converter.

The primary droop control can achieve automatic current-sharing and voltage regulation only with local information. However, the  $R_{dri}$  will cause a voltage deviation from its set-point  $v^*$ , and precise current-sharing is also unachievable due to the existence of the line resistance. Furthermore, for the health of BESSs, the SoCs of BESSs should be balanced, i.e., maintaining the SoCs of all BESSs at almost the same level during BESSs charging and discharging. Thus, SoC estimation

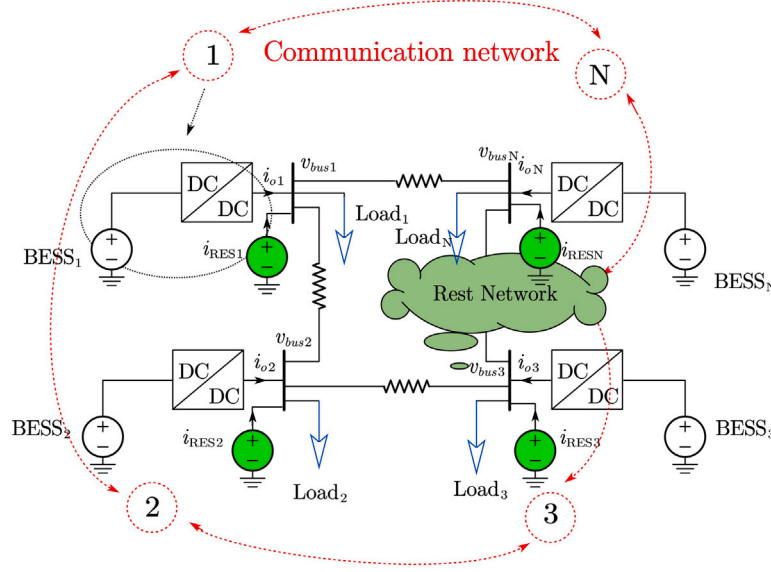


Fig. 1. Configuration of DC Microgrids.

is essential, and it is usually updated with the Coulomb Counting method [35]

$$\text{SoC}_i = \text{SoC}_{\text{init}_i} - \frac{1}{C_{bi}} \int i_{oi} dt \quad (4)$$

where  $\text{SoC}_i$  and  $C_{bi}$  are the SoC and capacity of  $\text{BESS}_i$ , respectively.  $\text{SoC}_{\text{init}_i}$  is the initial SoC value of  $\text{BESS}_i$ . In summary, the following three objectives, i.e., accurate current-sharing, SoC balance, average voltage regulation, should be achieved in the DC microgrids operation, and the proposed distributed secondary control is introduced in Section 3 to achieve following objectives

$$\lim_{t \rightarrow \infty} (i_{oi}/C_{bi} - i_{oj}/C_{bj}) = 0 \quad \forall i, j \quad (5a)$$

$$\lim_{t \rightarrow \infty} (\text{SoC}_i - \text{SoC}_j) = 0 \quad \forall i, j \quad (5b)$$

$$\lim_{t \rightarrow \infty} 1/N \sum_{i=1}^N v_{busi} - v^* = 0 \quad (5c)$$

## 2.4. Graph theory

To achieve the aforementioned objectives in the DC microgrids operation, a communication network is needed in the proposed distributed secondary control. As illustrated in Fig. 1, the communication network topology can be modeled as an undirected graph, where each BESS and converter are represented as a node and these nodes are connected by a communication digraph represented by edges. Their connections can be represented by an adjacency matrix  $\mathbf{A} = [a_{ij}] \in \mathbb{R}^{N \times N}$ , where the communication weights are given by:

$$a_{ij} = \begin{cases} 1 & \text{if } j \in N_i^c \\ 0 & \text{otherwise} \end{cases} \quad (6)$$

$N_i^c$  denotes the set of nodes that have a communication links with  $i$ th node. Further, the incoming cyber information matrix can be denoted by  $\mathbf{Z}_{in} = \text{diag}\{d_i\}$ ,  $d_i = \sum_{j \in N_i^c} a_{ij}$ . In this paper, all communication links are bidirectional and the Laplacian matrix  $\mathbf{L}$ ,  $\mathbf{L} = \mathbf{Z}_{in} - \mathbf{A}$ , is balanced [36].

## 3. Proposed control strategy for DC microgrids

### 3.1. Secondary control term generation

To achieve objectives in Eq. (5), the distributed secondary control is usually used to generate a secondary term  $u_i$ , which is added to the

droop expression Eq. (3), it yields

$$v_{refi} = v^* - R_{dri} i_{oi} + u_i \quad (7)$$

In the proposed control strategy, the detail control algorithm for  $u_i$  is presented in Fig. 2, where a cascaded framework consisting of an SoC controller and a voltage controller is proposed and a virtual state variable  $\rho_i$  combing current and SoC information is defined

$$\rho_i = i_{oi}/C_{bi} - \theta \text{SoC}_i \quad (8)$$

$\theta$  is an SoC balance index, a greater  $\theta$  causes faster SoC balance speed, the influence of  $\theta$  to SoC balance speed will be discussed in the Section 5. In the SoC controller,  $\text{BESS}_i$  compares its local  $\rho_i$  with neighbors'  $\rho_j$  then the difference is sent to PI controller to generate a voltage correction term  $\delta_i$

$$\delta_i = k_p \sum_{j \in N_i^c} a_{ij} (\rho_j - \rho_i) + k_s \int \sum_{j \in N_i^c} a_{ij} (\rho_j - \rho_i) dt \quad (9)$$

where  $k_p$  and  $k_s$  are proportional gain and integral gain, respectively. In the voltage controller,  $\delta_i$  is added to nominal voltage  $v^*$  to modify DC bus voltage. As elaborated in Eq. (10), the  $u_i$  is expressed as

$$u_i = \gamma \int v^* + \delta_i - v_{busi} dt \quad (10)$$

where  $\gamma$  is the voltage regulation index. With the proposed control strategy, the voltage deviation between  $v^*$  and  $v_{busi}$  is  $\delta_i$ . In some situation that the RESs and loads are uneven distributed in different DC buses, to achieve accurate current-sharing and average voltage regulation, some DC buses have to largely deviate to the nominal voltage, which will deteriorate the bus voltage quality. Hence, a voltage deviation limiter is introduced to constrain the voltage deviation between  $v^*$  and  $v_{busi}$ .

### 3.2. Control objectives achievement discussion

The SoC controller is designed based on consensus protocol, hence, this protocol drives all states to the same consensus value [36], i.e.,

$$\rho_i = \rho_j \rightarrow i_{oi}/C_{bi} - i_{oj}/C_{bj} = \theta \Delta \text{SoC}_{ij} \quad \forall i, j \quad (11)$$

where  $\Delta \text{SoC}_{ij} = \text{SoC}_i - \text{SoC}_j$ .

This virtually defined state variable helps SoC balance no matter in BESSs charging or discharging mode, and the process of SoC balancing is elaborated below. Combining Eq. (4) and Eq. (11), it yields

$$\frac{d\text{SoC}_j}{dt} - \frac{d\text{SoC}_i}{dt} = \theta \Delta \text{SoC}_{ij} \quad (12)$$

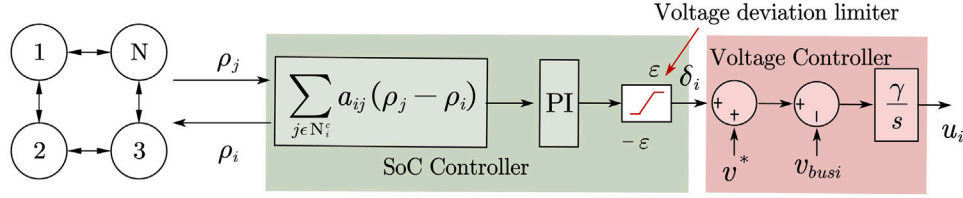


Fig. 2. The proposed distributed secondary control framework.

For the simplicity, the following scenarios are used to demonstrate the SoC balancing process based on the assumption that  $\text{SoC}_i > \text{SoC}_j$ , i.e.,  $\Delta \text{SoC}_{ij} > 0$ . It is worth noting that the dynamics of the output current is much faster than the SoC, hence,  $\Delta \text{SoC}_{ij}$  can be considered as unchanged.

**Scenario 1:** Both  $\text{BESS}_i$  and  $\text{BESS}_j$  are discharging

Eq. (4) indicates that  $\frac{d\text{SoC}}{dt} < 0$  in BESSs discharging process. As  $\Delta \text{SoC}_{ij} > 0$ , it is easy to infer that  $|\frac{d\text{SoC}_i}{dt}| > |\frac{d\text{SoC}_j}{dt}|$ , which indicates that SoC decrease speed of  $\text{BESS}_i$  is quicker than  $\text{BESS}_j$ , thus  $\text{BESS}_i$  and  $\text{BESS}_j$  will be gradually balanced.

**Scenario 2:** Both  $\text{BESS}_i$  and  $\text{BESS}_j$  are charging

Eq. (4) indicates that  $\frac{d\text{SoC}}{dt} > 0$  in BESSs charging process. As  $\Delta \text{SoC}_{ij} > 0$ , it is easy to infer that  $|\frac{d\text{SoC}_j}{dt}| > |\frac{d\text{SoC}_i}{dt}|$ , which indicates SoC increase speed of  $\text{BESS}_j$  is quicker than  $\text{BESS}_i$ , so that  $\text{BESS}_i$  and  $\text{BESS}_j$  will be gradually balanced.

**Scenario 3:**  $\text{BESS}_i$  is discharging and  $\text{BESS}_j$  is charging

In this scenario,  $\text{BESS}_i$  and  $\text{BESS}_j$  will be gradually balanced.

The steady-state analysis presented in Section 4 will further demonstrate that the SoC balance is achieved with the proposed control strategy.

Based on above analysis, the control objectives of accurate current-sharing and SoC balance are achieved with the proposed secondary control. As demonstrated in Table 1, to restore the average voltage to its nominal value, the average voltage observer proposed in [15] is widely used in previous study, and it is expressed as

$$v_{avg_i} = v_{bus_i} - \int \sum_{j \in N_c^i} a_{ij} (v_{avg_i} - v_{avg_j}) dt \quad (13)$$

where  $v_{avg_i}$  and  $v_{avg_j}$  are observed average voltages at  $\text{BESS}_i$  and  $\text{BESS}_j$ . In these average voltage observer based (AVOB) methods, information of voltage state variable  $v_{avg}$  needs to be transmitted to their neighbors for average voltage observation, which introduces an extra state variable. In the proposed control strategy, the average voltage observer is removed. Due to  $L$  is balanced, the average voltage regulation is achieved automatically when output current is regulated, it will be demonstrated in the stability and steady-state analysis in Section 4.

In summary, only the state variable  $\rho$  need to be exchanged between neighboring BESSs and the average voltage observer is removed, the average voltage regulation, accurate current-sharing and SoC balance are achieved with the proposed control strategy. The reduction of exchanged state variable and the simplicity of  $\rho$  design (no need to change when BESSs switch between charging/discharging) makes the proposed control strategy more straightforward and simplified compared with existing methods.

### 3.3. Design of control parameter $\theta$

As aforementioned, a larger  $\theta$  leads to a faster SoC balance speed, but its value has a limit. The design of  $\theta$  can be referred to Eq. (11). For simplicity, the power mismatch between the loads and RESs is represented by equivalent load  $I_e$

$$I_e = \sum_{i=1}^N (i_{load_i} - i_{RES_i}) \quad (14)$$

where  $i_{load_i}$  is the current drawn by the  $i$ th load. Assuming two BESSs are connected in the system, it yields

$$i_{o1}/C_{b1} - i_{o2}/C_{b2} = \theta \Delta \text{SoC}_{12} \quad (15a)$$

$$i_{o1} + i_{o2} = I_e \quad (15b)$$

It is worth noting that  $i_{o1}/C_{b1}$ ,  $i_{o2}/C_{b2}$  are the charging/discharging C-rate for two BESSs. In the microgrid application, BESSs charging/discharging current is usually smaller than 1C, i.e.,  $i_{o1} < C_{b1}$  and  $i_{o2} < C_{b2}$ . Combining Eq. (15), it yields

$$-1 < i_{o1}/C_{b1} = \frac{I_e + \theta C_{b2} \Delta \text{SoC}_{12}}{C_{b1} + C_{b2}} < 1 \quad (16a)$$

$$-1 < i_{o2}/C_{b2} = \frac{I_e - \theta C_{b1} \Delta \text{SoC}_{12}}{C_{b1} + C_{b2}} < 1 \quad (16b)$$

Based on Eq. (16), the feasible range for  $\theta$  can be expressed as

$$0 < \theta < \frac{C_{b1} + C_{b2} - I_e}{C_{b2} \Delta \text{SoC}_{12}} \text{ if } I_e > 0 \quad (17a)$$

$$0 < \theta < \frac{C_{b1} + C_{b2} + I_e}{C_{b1} \Delta \text{SoC}_{12}} \text{ if } I_e < 0 \quad (17b)$$

If the circulating current between BESSs is not allowed, i.e., the BESSs are always working at same mode (charging/or discharging), another constraints should be applied

$$\theta < \frac{I_e}{C_{b1} \Delta \text{SoC}_{12}} \text{ if } I_e > 0 \quad (18a)$$

$$\theta < \frac{-I_e}{C_{b2} \Delta \text{SoC}_{12}} \text{ if } I_e < 0 \quad (18b)$$

The above analysis can also be extended to a system with  $N$  BESSs, then the feasible range for  $\theta$  can be calculated accordingly.

### 3.4. Complete control block for BESSs

With the primary droop control and the proposed distributed secondary control, the detailed control algorithm and power electronics circuit for  $\text{BESS}_i$  are illustrated in Fig. 3, where  $\pm i_{limit}$  is the charging and discharging current limit for all converters, and  $L$  and  $C_{bus}$  are induction for all converters and capacitance for all DC buses, respectively. The  $\text{BESS}_i$  is connected to the DC bus through a bidirectional buck-boost converter, and it is operated in voltage control mode. The  $v_{ref_i}$  is generated according to Eq. (7), the voltage loop tracks  $v_{ref_i}$  and generates the  $i$ th converter output current reference  $i_{ref_i}$ . Similarly, the current loop tracks  $i_{ref_i}$  and generate two complementary Pulse Width Modulations (PWMs).

## 4. Stability and steady-state analysis

This section presents the stability and steady-state analysis to demonstrate the effectiveness of the proposed control strategy and investigate the influence of system parameters on the system stability

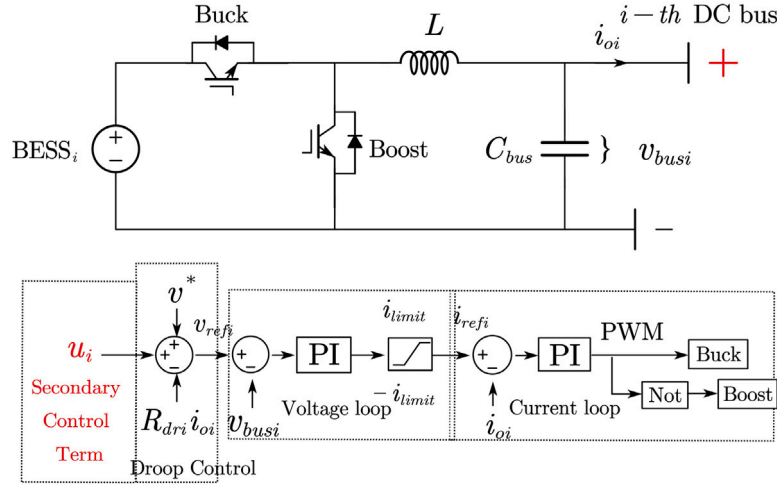


Fig. 3. Complete control block and power electronics circuit for BESS<sub>i</sub>.

and steady-state performance. To research the impact of communication delay on the system stability and steady-state performance, the adjacency matrix  $A$  is modified in to  $A' = [a'_{ij}] \in R^{N \times N}$

$$a'_{ij} = \begin{cases} 1/(1 + \tau s) & \text{if } j \in N_i^c \\ 0 & \text{otherwise} \end{cases} \quad (19)$$

where  $\tau$  is the communication delay between neighboring nodes. The self communication delay is introduced and set to  $\tau$  in the proposed control strategy, then the incoming cyber information matrix can be denoted by  $Z'_{in} = \text{diag}\{d_i\}$ ,  $d_i = \sum_{j \in N_i^c} a'_{ij}$ , and the modified Laplacian matrix becomes  $L' = Z'_{in} - A'$ .

Combining Eq. (7), Eq. (9) and Eq. (10), the system voltage reference can be expressed as

$$v_{ref} = v^* - R_{dr} i_o + \gamma \int (v^* - k_p L' \rho - k_s L' \int \rho dt - v_{bus}) dt \quad (20)$$

where  $v_{ref} = [v_{ref1}, v_{ref2}, \dots, v_{refN}]^T$  is the reference voltage sector,  $v^* = v^* \mathbf{1}_N$  is the nominal voltage sector and  $\mathbf{1}_N$  is N-th order vector with all elements equal to 1.  $R_{dr} = \text{diag}\{R_{dri}\}$  is droop coefficient matrix. And

$$\rho = C_b^{-1} i_o - \theta \text{SoC} \quad (21)$$

$\text{SoC} = [\text{SoC}_1, \text{SoC}_2, \dots, \text{SoC}_N]^T$  is SoC vector,  $C_b = \text{diag}\{C_{bi}\}$  is battery capacity matrix. Combining Eq. (20) and (21) and applying Laplace transform

$$V_{ref} = V^* - R_{dr} I_o + \frac{\gamma}{s} \left[ V^* - \left( k_p + \frac{k_s}{s} \right) L' (C_b^{-1} I_o - \theta \text{SOC}) - V_{bus} \right] \quad (22)$$

where  $V^* = \frac{v^*}{s} \mathbf{1}_N$  is the Laplace transform of  $v^*$ , similarly,  $V_{bus}$ ,  $V_{ref}$ ,  $I_o$  and  $\text{SOC}$  are the Laplace transform of  $v_{bus}$ ,  $v_{ref}$ ,  $i_o$  and  $\text{SoC}$ , respectively.

Applying Laplace transform to Eq. (1) and Eq. (4)

$$I_o + I_{RES} = Y V_{bus} \quad (23)$$

$$\text{SOC} = -C_b^{-1} I_o / s \quad (24)$$

where  $I_{RES} = [i_{RES1}/s, i_{RES2}/s, \dots, i_{RESN}/s]^T$  is the Laplace transform of  $i_{RES}$ .

As illustrated in Fig. 3, the speed of the inner loops (voltage loop and current loop) are usually much faster than the reference voltage update, thus, the inner loops can be viewed as '1' [37], i.e.,  $V_{ref} = V_{bus}$  is assumed in the following analysis. Combining Eq. (22) to Eq. (24), the closed loop transfer function of DC bus voltages with input  $V^*$  and  $I_{RES}$

Table 2

System and control parameters used in stability and steady-state analysis.

Parameters	Value	Parameters	Value
$y_1$	0.1 $\Omega^{-1}$	$y_r, (i = 2, 3, 4)$	Not Connected
$y_{12}, y_{14}$	10 $\Omega^{-1}$	$y_{23}$	5 $\Omega^{-1}$
$y_{34}$	2 $\Omega^{-1}$	$C_{bus}$	0.1 F
$i_{RES3}$	50 A	$i_{RESi}, (i = 1, 2, 4)$	Not Connected
$C_{bi}, (i = 1, 2, 3, 4)$	50 A h	$\gamma$	1
$k_i$	50	$k_p$	50
$\theta$	2	$v^*$	380 V

can be expressed as by Eq. (25), where  $\mathbf{I}_N$  is N-th order identity matrix. Given Eq. (25), the dynamics of DC bus voltages can be calculated directly.

$$V_{bus} = \frac{A_n s^3 + B_n s^2 + C_n s + D_n}{A_d s^3 + B_d s^2 + C_d s + D_d} \quad (25)$$

where

$$\begin{aligned} A_d &= \mathbf{I}_N + R_{dr} Y & B_d &= \gamma \mathbf{I}_N + \gamma k_p L' C_b^{-1} Y \\ C_d &= (\gamma k_s + \gamma \theta k_p) L' C_b^{-1} Y & D_d &= \gamma \theta k_s L' C_b^{-1} Y \\ A_n &= I_{RES} R_{dr} + V^* & B_n &= \gamma k_p L' C_b^{-1} I_{RES} + \gamma V^* \\ C_n &= (\gamma k_s + \gamma \theta k_p) L' C_b^{-1} I_{RES} & D_n &= \gamma \theta k_s L' C_b^{-1} I_{RES} \end{aligned}$$

#### 4.1. Stability analysis

Based on closed loop transfer function of DC bus voltages in Eq. (25), the stability analysis of DC microgrids with the proposed control strategy is shown in Figs. 4 and 5. For simplicity, a four-bus system is used, and the system and controller parameters used in the stability and steady-state analysis are given in Table 2.

Fig. 4 illustrates the movement of poles as  $\gamma$  and  $\theta$  increase, the blue stars represent the location where the poles move from while the red stars show the location where the poles end. The poles in the red cycle are related to the battery SoCs. In Fig. 4(a),  $\gamma$  increases from 0.1 to 10, while the other parameters used in the analysis are kept same as shown in Table 2. It is shown that all the poles are located in the left half of s-plane, which shows that DC microgrids with the proposed control strategy are stable. The poles related to the battery SoCs are kept unchanged as  $\gamma$  increases, which confirms that the SoC balance speed is not affected by  $\gamma$ . And the other poles move towards left as  $\gamma$  increases, demonstrating that a greater  $\gamma$  leads a faster voltage regulation speed.

As illustrated in Fig. 4(b),  $\theta$  increases from 0.1 to 10, similarly, it can be observed that all the poles are located in the left half of s-plane.

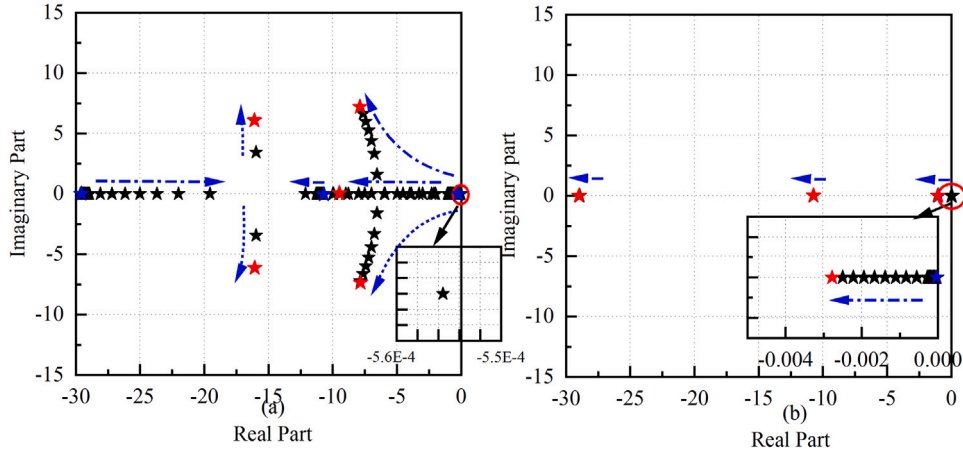


Fig. 4. Root locus with the proposed control strategy (a) as  $\gamma$  increases (b) as  $\theta$  increases.

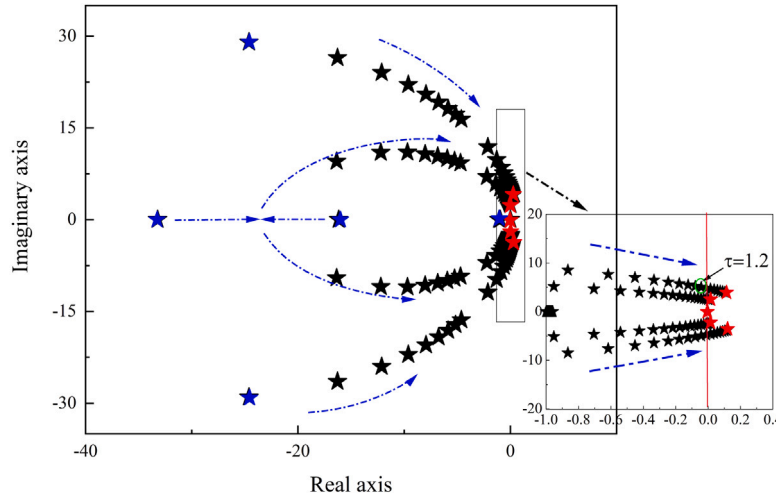


Fig. 5. Root locus as  $\tau$  increases from 0.02 s to 2 s in the proposed control strategy.

The poles related to the battery SoCs moves towards left while the other poles are almost kept unchanged as  $\theta$  increases, which demonstrates that a greater  $\theta$  leads a faster SoC balance speed.

In the communication-based control strategy, a large communication delay will inevitably make the system unstable. Fig. 5 illustrates the locus of poles as the communication delay  $\tau$  increases, and it is evident that the system response slows down with the increase of  $\tau$ , and it is shown in the enlarged figure that the poles move to the right half of s-plane when  $\tau$  is greater than 1.2 s, which implies that the system will become unstable.

#### 4.2. Steady-state analysis

Based on Eq. (22), the system DC bus voltage can be rewritten as

$$\begin{aligned} V_{bus} &= V^* - R_{dr} I_o + \frac{\gamma}{s} (V^* - V_{bus}) \\ &\quad - L' \left( \frac{\gamma k_p}{s} + \frac{\gamma k_s}{s^2} \right) (C_b^{-1} I_o - \theta SOC) \end{aligned} \quad (26)$$

As the Laplacian matrix  $L'$  is balanced,  $\mathbf{1}_N^T L' = 0$  [36]. By multiplying  $\mathbf{1}_N^T$  at both sides of Eq. (26), it yields

$$\mathbf{1}_N^T V_{bus} = \mathbf{1}_N^T \left[ V^* - R_{dr} I_o + \frac{\gamma}{s} (V^* - V_{bus}) \right] \quad (27)$$

Based on Eq. (27), it is evident that

$$\lim_{s \rightarrow 0} (\mathbf{1}_N^T \gamma + s \mathbf{1}_N^T) s V_{bus} + s^2 \mathbf{1}_N^T R_{dr} I_o = \lim_{s \rightarrow 0} s^2 \mathbf{1}_N^T V^* + s \mathbf{1}_N^T \gamma V^* \quad (28)$$

Applying the final value theorem [38], then

$$v_{bus}^{ss} = \lim_{s \rightarrow 0} s V_{bus} \quad (29a)$$

$$i_o^{ss} = \lim_{s \rightarrow 0} s I_o \quad (29b)$$

$$SoC^{ss} = \lim_{s \rightarrow 0} s SOC \quad (29c)$$

where  $v_{bus}^{ss} = [v_{bus1}^{ss}, v_{bus2}^{ss}, \dots, v_{busN}^{ss}]$ , is the DC bus voltage vector at steady-state,  $i_o^{ss}$  is the converter output current vector at steady-state,  $SoC^{ss}$  is the SoC vector at steady-state. At the left side of the Eq. (28),  $\lim_{s \rightarrow 0} \mathbf{1}_N^T \gamma s V_{bus} = \gamma \sum_{i=1}^N v_{busi}^{ss}$ ,  $\lim_{s \rightarrow 0} s \mathbf{1}_N^T s V_{bus} = 0$ ,  $\lim_{s \rightarrow 0} s \mathbf{1}_N^T R_{dr} s I_o = \lim_{s \rightarrow 0} s \mathbf{1}_N^T R_{dr} i_o^{ss} = 0$ . At the right side of the Eq. (28),  $\lim_{s \rightarrow 0} s \mathbf{1}_N^T s V^* = 0$ ,  $\lim_{s \rightarrow 0} \gamma \mathbf{1}_N^T s V^* = \gamma N v^*$ . Hence, Eq. (30) is established based on (28)

$$\frac{1}{N} \sum_{i=1}^N v_{busi}^{ss} = v^* \quad (30)$$

Hence, the proposed control strategy achieves average voltage regulation.

Combining Eq. (24) and (26), it yields

$$L' C_b^{-1} I_o = \frac{(s^3 + \gamma s^2) (V^* - V_{bus}) - s^3 R_{dr} I_o}{\gamma k_p s^2 + (\gamma k_s + \gamma \theta k_p) s + \gamma \theta k_s} \quad (31)$$

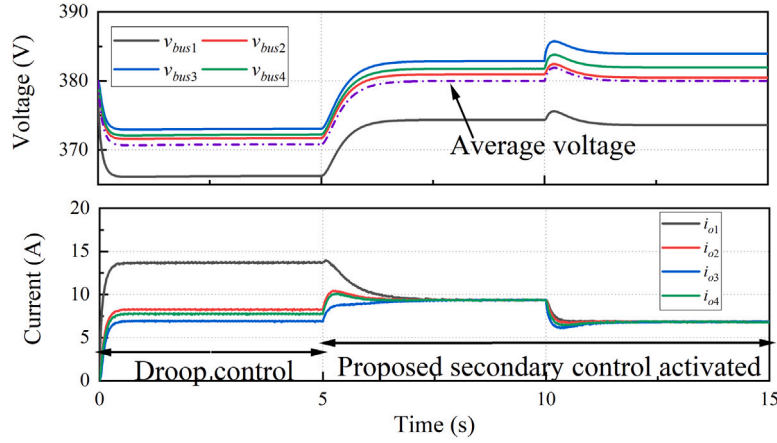


Fig. 6. Test results before and after the secondary control activated.

Combining Eqs. (31) and ((29)ab), it yields

$$L' C_b^{-1} i_o^{ss} = \lim_{s \rightarrow 0} \frac{(s^3 + \gamma s^2) (s V^* - v_{bus}^{ss}) - s^3 R_{dr} i_o^{ss}}{\gamma k_p s^2 + (\gamma k_s + \gamma \theta k_p) s + \gamma \theta k_s} = 0 \quad (32)$$

It is easy to infer that the numerator approaches to 0 when  $s$  approaches to 0 in Eq. (32). Hence,  $L' C_b^{-1} i_o^{ss} = 0$ , which indicates  $C_b^{-1} i_o^{ss}$  is the right eigenvector of  $L'$  associated with zero eigenvalue. According to the property of  $L'$  [36]

$$C_b^{-1} i_o^{ss} = \lambda_1 \mathbf{1}_N \quad (33)$$

where  $\lambda_1$  is a positive value, and  $\lambda_1 C_b$  is a vector that the converter current vector  $i_o$  will finally converge. Hence the accurate current-sharing among BESSs is achieved with proposed control strategy.

Eq. (26) can be rewritten as

$$L' \text{SOC} = \frac{(s^2 + \gamma s) (V_{bus} - V^*) + s^2 R_{dr} I_o}{\gamma \theta k_p s + \gamma \theta k_s} + 1/\theta L' C_b^{-1} I_o \quad (34)$$

Combining Eq. (34) and Eq. (29), it yields

$$\begin{aligned} L' \text{SoC}^{ss} &= \lim_{s \rightarrow 0} \frac{(s^2 + \gamma s) (v_{bus}^{ss} - s V^*) + s^2 R_{dr} i_o^{ss}}{\gamma \theta k_p s + \gamma \theta k_s} + \frac{L' C_b^{-1} i_o^{ss}}{\theta} \\ &= \lim_{s \rightarrow 0} \frac{L' C_b^{-1} i_o^{ss}}{\theta} \end{aligned} \quad (35)$$

$\lim_{s \rightarrow 0} L' C_b^{-1} i_o^{ss} = 0$  based on Eq. (32), thus  $L' \text{SoC}^{ss} = 0$ , which indicates  $\text{SoC}^{ss}$  is the right eigenvector of  $L'$  associated with zero eigenvalue. According to the property of  $L'$

$$\text{SoC}^{ss} = \lambda_2 \mathbf{1}_N \quad (36)$$

where  $\lambda_2$  is a positive value, the SoC vector  $\text{SoC}$  will finally converge to this value. Hence the SoC balance among BESSs is achieved with the proposed control strategy.

## 5. Results and discussions

### 5.1. Simulink test results and discussions

To validate the proposed control strategy, a four-bus system with five case studies is tested in Matlab/Simulink environment. The  $i_{RES3}$  changes with time, and the parameters for the system and controller used in the tests are same with that in Table 2.

#### A. Test Results Before and After Secondary Control

In this case study, the test results with the proposed control strategy before and after the secondary control activated are illustrated in Fig. 6. From 0 s to 5 s, the DC microgrid is controlled only by the droop control, and the average DC bus voltage is stabilized at a value less

than 380 V, the BESSs converters output currents are significantly different from each other due to uneven distribution of load, besides, the mismatch of line resistance also has an impact on the current-sharing.

To achieve accurate current-sharing and average voltage regulation, the proposed secondary control is activated at 5 s, the output currents of all converters converge to about 10 A, achieving even current-sharing among BESSs, and the average DC bus voltage is restored to the nominal value of 380 V. The  $i_{RES3}$  increases to 10 A at 10 s, the accurate current-sharing and average voltage regulation can still be maintained after RES perturbation.

#### B. SoC Balance Speed Study

In this case study, SoC balance speed with different  $\theta$  is investigated. The initial SoCs of the four BESSs are set 0.8, 0.7, 0.6, 0.5, respectively. And to fully investigate the SoC balance dynamics, the  $C_b$  of all BESSs is scaled down from 50 Ah to 0.2 Ah.

The SoC balance trajectory with  $\theta = 2$  is illustrated in Fig. 7. From 0 s to 10 s  $i_{RES3}$  is set to 0 A, four BESSs inject power to the DC microgrid to support the load, the output currents of four BESSs converters are slightly different where the BESSs with higher initial SoC values inject more power to the DC microgrid to achieve SoC balance. From 10 s to 20 s,  $i_{RES3}$  is set to 75 A, four BESSs work in charging mode, BESSs with higher initial SoC values absorb less power to achieve SoC balance. The case study shows that no matter BESSs work in charging or discharging mode, the difference of SoCs will gradually narrow down with time.

The SoC balance with  $\theta = 10$  is illustrated in Fig. 8, it shows a greater difference between the output currents of BESSs compared with the situation where  $\theta = 2$ , and a quicker SoC balance process is achieved. Once SoCs converge, they will keep consensus in the following time.

#### C. Average Voltage Regulation Speed Study

Fig. 9 illustrates the voltage regulation speed with different  $\gamma$ . To achieve accurate current-sharing between four BESSs, the four DC bus voltages are stabilized at different values. It takes about 3 s and 1 s for the average DC bus voltage to be restored to its nominal value 380 V with  $\gamma = 0.5$  and  $\gamma = 2$ , respectively. It is evident that a greater  $\gamma$  leads a faster voltage regulation speed.

#### D. Comparison With AVOB Control Strategy

**Scenario 1:** Under individual DC bus voltage deviation limit

In the situation where the RESs and loads are uneven distributed in different DC buses, some DC buses have to largely deviate to the nominal voltage to achieve accurate current-sharing and average voltage regulation, which will deteriorate the voltage quality. To avoid that, the average voltage regulation function should be abandoned in that situation. To validate the performance of the voltage deviation limiter in the proposed control strategy under uneven load distributed,



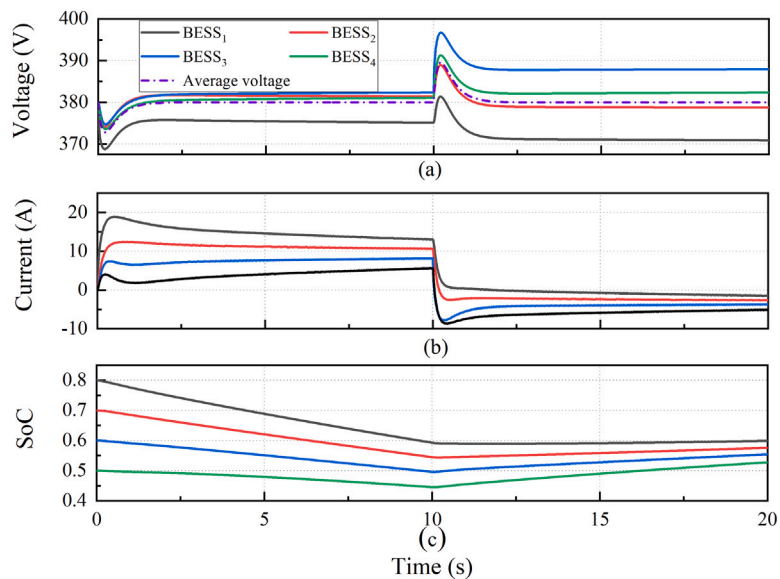


Fig. 7. SoC balance study with  $\theta = 2$  (a)  $v_{bus}$  (b)  $i_o$  (c) SoC values.

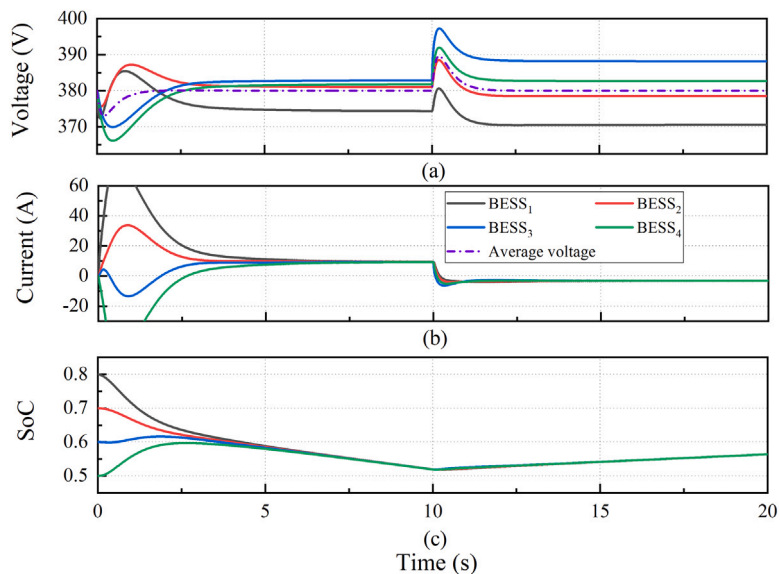


Fig. 8. SoC balance study with  $\theta = 10$  (a)  $v_{bus}$  (b)  $i_o$  (c) SoC values.

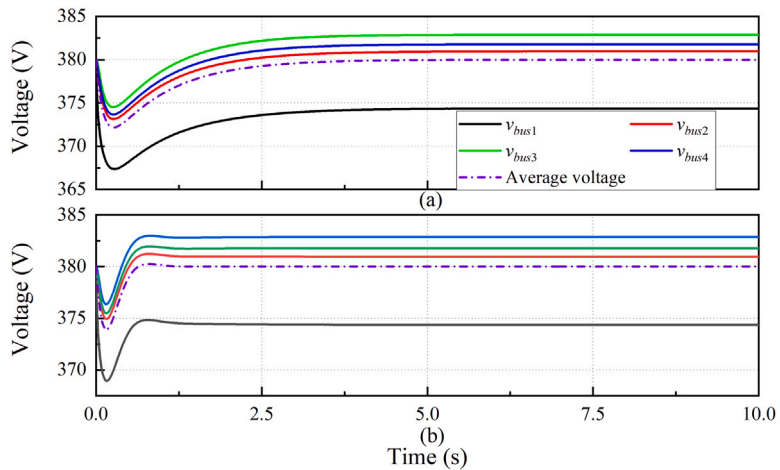


Fig. 9. DC bus voltages with different  $\gamma$  (a)  $\gamma = 0.5$  (b)  $\gamma = 2$ .

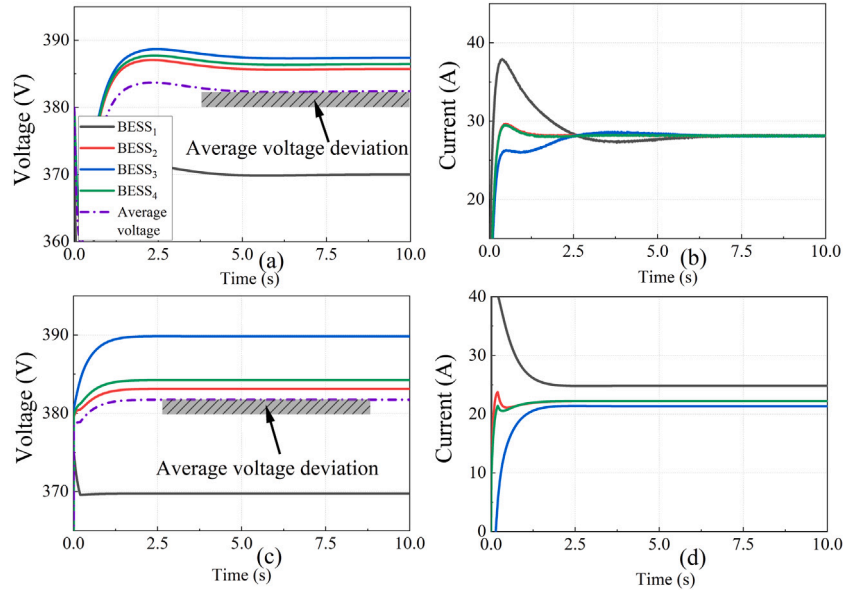


Fig. 10. Performance under DC bus voltage deviation limit (a)/(b)  $v_{bus}/i_o$  with the proposed strategy (c)/(d)  $v_{bus}/i_o$  with AVOB methods.

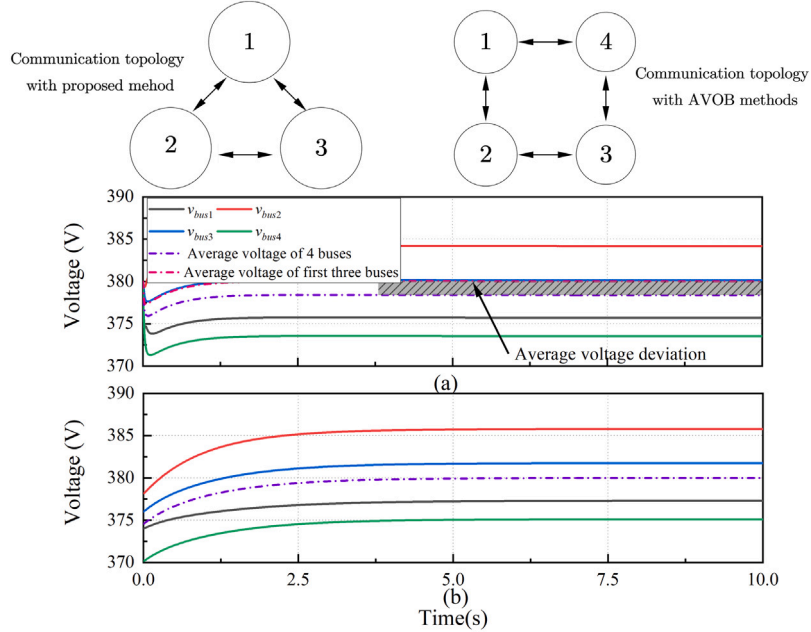


Fig. 11. DC bus voltage regulation when BESS<sub>4</sub> is not connected (a) the proposed control strategy (b) the AVOB control strategies.

$y_1$  is set to  $0.25 \Omega^{-1}$  while other parameters are kept unchanged in Table 2. A strict voltage deviation limiter where  $\epsilon$  is set to 10 V is introduced. Fig. 10 illustrates that voltage regulation and current-sharing with the proposed control strategy and AVOB control strategy. It can be observed that the average voltage is less than 380 V and all individual DC bus voltages are constrained between 370–390 V with the proposed control strategy. In the AVOB control strategy, the coordination between the voltage regulation and power flow term cannot be achieved, both the average regulation and current-sharing are deteriorated.

**Scenario 2: When BESS is not available at 4-th bus**

The aforementioned analysis and simulation are based on that each DC bus is supported by a BESS, where the average voltage regulation, accurate current-sharing, and SoC balance is achieved. In this scenario, BESS<sub>4</sub> is not connected to 4-th DC bus, thus  $\rho_4$  does not

exist consequently, the communication topology with the proposed control strategy is modified according to Fig. 11, while  $v_{avg4}$  is still transmitted and the communication topology is kept unchanged in the AVOB control strategies. It can be easily calculated that the average voltage of first, second and third DC bus equals to 380 V with the proposed control strategy, however, the average voltage of all 4 DC buses is lower than 380 V. In the AVOB control strategies, the average voltage of 4 buses still can be achieved.

In summary, the average voltage regulation can be achieved with the proposed control strategy when each DC bus is supported with a BESS, the AVOB control strategies are preferred to achieve average voltage regulation when BESS is not available.

**E. Comparison With Ref. [22]**

In this subsection, the comparison between the proposed control strategy and the control strategy in Ref. [22] is presented. As listed in

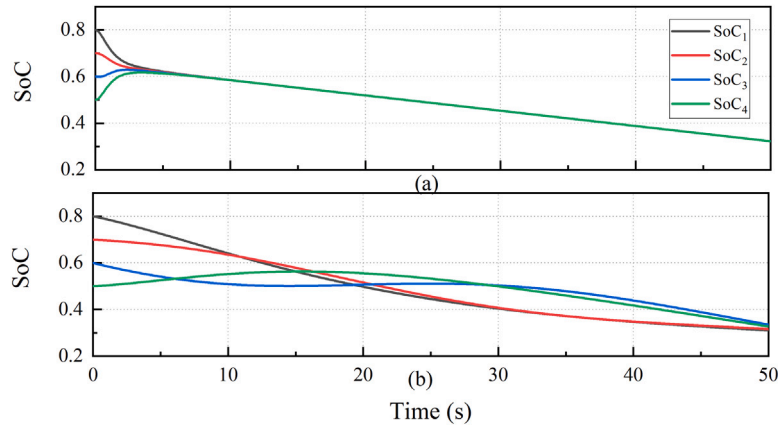


Fig. 12. SoC variations with (a) the proposed control strategy (b) Ref. [22].

the Table 1, the SoC is chosen as a state variable directly in Ref. [22] to adjust the power flow among different BESSs. Fig. 12 illustrates that SoCs of four BESSs with the proposed control strategy are kept consensus after they reach same value at about 5 s. However, the consensus of SoCs are not achieved with the control strategy in Ref. [22], although SoC difference among four BESSs narrows down.

5.2. Hardware-in-loop test results and discussions

To further validate the proposed control strategy, the HIL real-time tests are conducted using the Typhoon HIL-604 platform. This ultra-high fidelity HIL device consists of 8-core processors able for real-time emulation of up to 8 converters, and can test the controller with 20 ns PWM resolution. It can also emulate power stage with up to 2 MHz update rate. This device can interface to external hardware controllers via its 64 analog outputs, 32 analog inputs, 64 digital inputs, and 64 digital outputs. As illustrated in Fig. 13, the whole system (converters, BESSs) is emulated by typhoon HIL-604, while the controller for the real-time emulated system is implemented using a Texas Instruments TI LaunchPad (LAUNCHXL-F28069M), which is interfaced with the typhoon HIL device through a Launchpad interface. The controller communicates the emulated system through 16-ADC channels, then sends PWM signals back to typhoon HIL device.

The HIL test results with the proposed control strategy are illustrated in Fig. 14, and a perturbation is applied to  $i_{RES3}$  at 5s. It can be observed that the average voltage regulation and accurate current-sharing are achieved. Fig. 15 shows the HIL test results with SoC balance, where four BESSs have different initial SoCs. The difference between SoCs is gradually narrowed down with time.

6. Conclusions

In this paper, a simplified consensus-based distributed secondary control for BESSs in DC microgrids has been proposed with the information of only one virtually defined state variable being transmitted, where a cascaded control framework consisting of an SoC controller and a voltage controller is used to regulate DC bus voltages. This virtual state variable combines the BESS SoC and its converter output current, there is no need to change the control law when BESSs switch between charging/discharging modes. Once SoCs are balanced, SoC controller works as a current controller. With the proposed control strategy, the number of transmitted state variables and the complexity of controller design are significantly reduced. Stability and steady-state analysis are also conducted to confirm the effectiveness of the proposed control

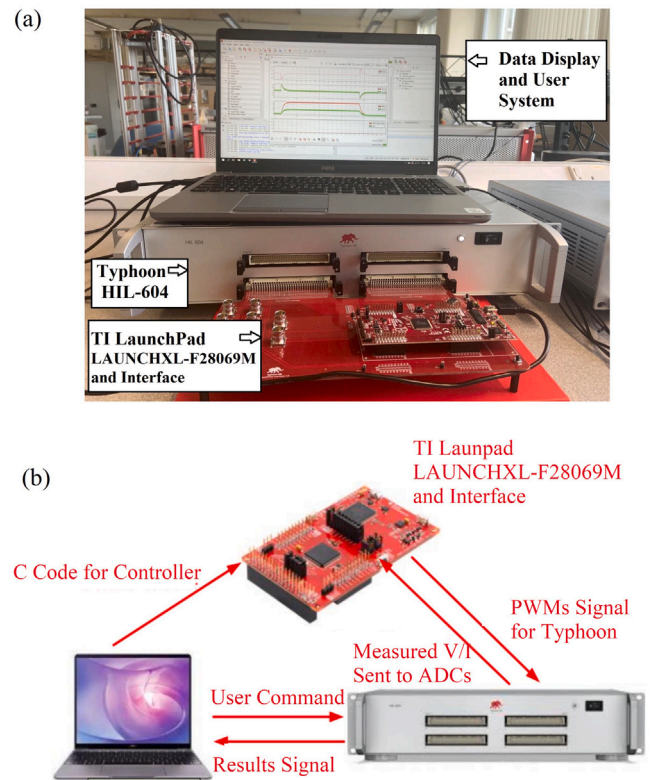


Fig. 13. HIL tests (a) Experimental set-up (b) Device operation details.

strategy. Finally, Simulink simulation and HIL tests are presented to validate the proposed control strategy.

The performance of the proposed control strategy is affected by voltage regulation index  $\gamma$  and SoC balance index  $\theta$ . The test results confirm that a greater  $\gamma/\theta$  lead to a faster average voltage regulation/SoC balance speed. The comparison with other existing methods further validates the effectiveness of the proposed control strategy.

CRediT authorship contribution statement

Jialei Su: Conceptualization, Methodology, Formal analysis, Software, Writing – original draft, Writing – review & editing. Kang Li: Conceptualization, Supervision, Resources, Project administration,

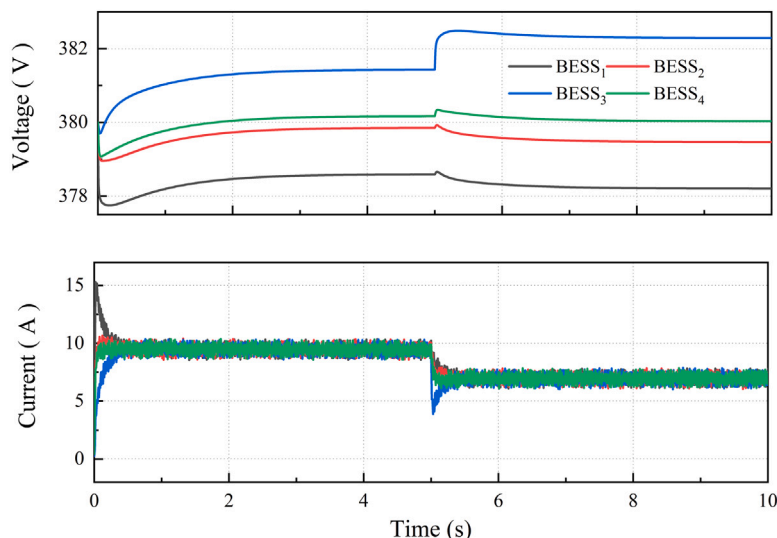


Fig. 14. HIL tests for voltage regulation and current-sharing.

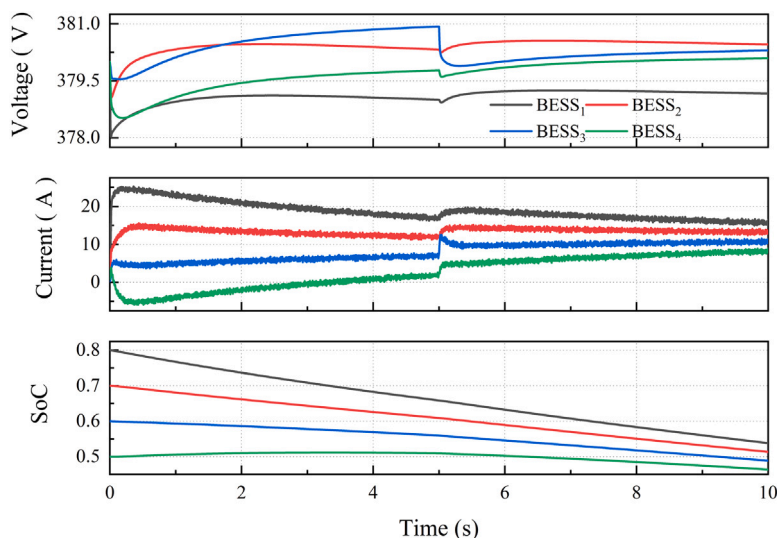


Fig. 15. HIL tests for SoC balance.

Funding acquisition, Writing – review & editing. **Chen Xing:** Validation, Investigation, Formal analysis. **Yihuan Li:** Validation, Investigation, Formal analysis. **James Yu:** Investigation.

**Declaration of competing interest**

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

**Data availability**

No data was used for the research described in the article.

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