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High-order Delayed Signal Cancellation-based PLL under Harmonically Distorted Grid Voltages

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***Abstract*—Quasi type-1 phase-locked loop (QT1-PLL) has become very popular in recent times for grid-connected converters owing to its simple structure and fast dynamic response. By means of the use of a half-cycle moving average filter (MAF), this PLL can completely eliminate all the nominal frequency odd-order harmonics. However, the performance deteriorates when the grid experiences frequency drift. To address this issue, high-order non-adaptive MAF with the same window length has been proposed in the literature. Although it improves the off-nominal frequency performance, the filtering induced phase-lag remains the same. To address this issue, high-order delayed signal cancellation technique is considered in this study. The proposed technique demonstrates similar filtering performance as high-order MAF, however, by using lower window length. This makes the proposed technique fast responsive with lower memory requirement compared to similar other techniques in the literature. Detailed small signal modelling and associated parameter tuning method are established to facilitate the implementation of the proposed method inside current controllers of grid-connected converters. Comparative experimental results are provided with QT1-PLL and third-order QT1-PLL (TQT1-PLL) to illustrate the suitability and performance enhancement by the proposed method. These results show that in addition to the superior filtering capability of the proposed PLL, its settling-time is less than one cycle of nominal frequency under most grid conditions. Consequently, in terms of enhancing the dynamic response of the QT1-PLL, the proposed HDSC-PLL is superior to the TQT1-PLL.**

***Index Terms*—Delayed signal cancellation, grid-connected converter, moving average filter, phase-locked loop.**

I. Introduction

Renewable energy sources (RESs) have started to become very popular over the last few decades as an alternative to conventional fossil fuel for energy supply. RESs are integrated into the existing power grid through power electronic converters. Considering the ever-increasing presence of renewable energy interfaced power converters, electricity network operators in various countries have modified their grid code accordingly. These converters are subject to similar conditions as their fossil fuel counterparts. These converters need to ensure that the injected power is of high quality, and they also need to contribute towards pursuing the stability of the power system. Supporting the grid in faulty condition is often a requirement. These converters need to inject high quality ac power even under heavily distorted grid.

In heavily distorted grid condition (such as imbalances, harmonics, dc-offset, etc.), injecting high quality ac power requires the development of advanced current controllers that can inject fundamental frequency current to the grid while rejecting most of the important harmonic components as specified by various standards e.g. IEEE Std. 519-2014. Most of the existing current controllers are implemented either in the orthogonal (stationary) reference frame (ORF) or in the synchronous reference frame (SRF). In the ORF, the reference current is a sinusoidal signal, which is time-varying. To track this reference, proportional-resonant (PR) current controllers is a popular choice [1]. By using resonant term, which is tuned at the same frequency as the estimated grid frequency, the PR controller can provide zero steady-state tracking error. In this approach, to mitigate the effect of harmonics, multiple resonant blocks are tuned at the frequencies of interest. As the grid frequency alters widely, albeit within a range, the performance of the PR controller depends on the performance of the frequency estimator, which can be performed through a frequency-locked loop [2] or phase-locked loop (PLL) [1]. In the SRF current controller case, time-varying measured current signals are converted to dc quantities through Park transformation, which requires the estimated phase angle of the grid voltage [3]. Since, the reference is a dc quantity here, proportional-integral (PI) controller is sufficient to provide zero steady-state tracking error. In order to provide high quality harmonic current compensation, the estimated phase angle should not contain any ripple/oscillation even when the grid is harmonically distorted by nonlinear loads. The examples highlight the importance of fast, accurate, and robust extraction of frequency and phase for grid-connected power electronic converter control.

In power systems, the widespread use of nonlinear loads such as rectifiers and solid-state controlled equipment causes an increase in harmonic distortion. Nonlinear loads have the tendency to alter the fundamental sinusoidal characteristics of AC currents, thus disturbing the sinusoidal nature of the AC grid voltages. This situation leads to the creation of voltage and current harmonics that propagate throughout the power distribution grid, causing a number of deleterious effects such as reduced power quality, overheating of electrical equipment, and additional losses within the system [3].

In the PLL context, SRF-PLL [4] is undoubtedly one of the most well-known techniques that is widely used in academia and industry. Examples of these areas are sensorless motor

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drives, uninterruptable power supplies, flexible ac transmission systems, distributed power generation systems, shunt active power filters, distributed static compensator, and so on.

The SRF-PLL is very easy to implement and tune and requires one Park transformation block and a PI type low-pass filter (LPF). Tuning of this PLL has a trade-off between dynamic response and disturbance rejection. Therefore, various solutions are suggested in the literature that to break the trade-offs. Broadly speaking, these attempts can be classified into two types. In the first type, various types of pre- and/or in-loop filters are proposed to directly address the harmonics. Some popular pre-loop filters are moving average filter (MAF) [5], delayed signal cancellation (DSC) [6]–[8], complex coefficient filter (CCF) [9], one cycle Fourier (OCF) [10], [11] etc. These filters can completely reject various harmonic components. In the second type, filtering induced phase lag (i.e. slower response) are eliminated either by using additional phase-lead compensator [12]–[14] or through reducing the control type of PLL from the control system viewpoint, e.g., quasi type-1 PLL (QT1-PLL) [15]–[18].

MAF is relatively simple to implement and doesn't require any tuning. Considering this advantage, MAF-PLL and its various variants [19] became very popular in recent times. In most of these implementations, MAF is typically implemented as an in-loop filter inside the SRF-PLL architecture. Using first-order Padé approximation, it can be found that the transfer function of a MAF is the same as a first-order low-pass filter. A lower cut-off frequency (i.e. higher window length for the MAF) will improve the harmonic performance of the MAF-PLL at the cost of slower settling time as settling time can be approximated as four times the time constant of the filter. This issue has been addressed in [20] through an additional in-loop phase-lead compensator, however, it may degrade the transient performance when the grid faces any abrupt change. Since the loop filter of MAF-PLL is of type 2 (i.e., the open-loop system has two poles at the origin), another potential solution to develop the dynamic performance is to use a type 1 loop filter. This has been achieved in [15] through QT1-PLL, where the loop filter has only a proportional parameter to tune. However, this deteriorates disturbance rejection capability when subject to frequency drift. This issue can be handled by making the MAF frequency adaptive [21], [22]. However, it is computationally expensive.

To address the limitation of frequency non-adaptive MAF in QT1-PLL, third-order MAF based QT1-PLL (TQT1-PLL) was proposed in [16]. Here, the half-cycle window length MAF is implemented as a cascaded combination of three MAF with the total window length being the same as the original version. This high-order MAF is significantly less sensitive to frequency drift compared to the conventional counterpart. However, the problem of slow dynamic response remains an issue.

Keeping the TQT1-PLL structure idea in mind, delayed signal cancellation method is considered here for improving the dynamic response. Here two third-order DSC blocks with window length less than half-cycle are considered. Through detailed frequency domain analysis, it has been shown that the proposed implementation is less sensitive to frequency drift while using a reduced window length. This results in lower phase lag, contributing to faster dynamic response. The main contribution of this work is the development of QT1-type PLL with high-order non-adaptive DSC blocks as the in-loop filters (briefly called the HDSC-PLL).

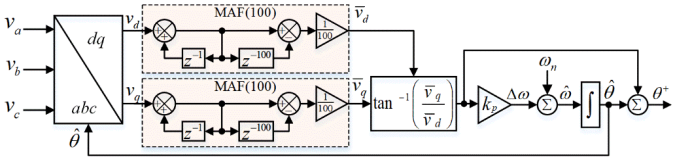

Fig. 1. Block structure of standard QT1-PLL.

The developed HDSC-PLL can eliminate the dominant harmonics, provide fast dynamic response, require lower memory and more robust to frequency drift compared to similar other non-adaptive techniques.

II. Overview of QT1-PLL and TQT1-PLL

Fig. 1 shows the block structure of standard QT1-PLL. As observed, the QT1-PLL includes a MAF in its control loop. Here, the task of the MAF is to reject the harmonic components.

The controller pattern of QT1-PLL is different from conventional SRF-PLL that uses a PI controller. The QT1-PLL employs only a proportional parameter (k_p). So, it may appear as a type-1 system; however, it transforms into type-2 system due to having a feedforward path to the phase angle output as illustrated in Fig. 1. Thus, compared to a type-2 PLL, the QT1-PLL provides increased dynamic performance and, simplifies the controller parameter design. Note that as can be seen in the block diagrams of TQT1-PLL and proposed PLL in the following sections, they also have the same controller structure as QT1-PLL. The feature that sets them apart is the difference in their filtering structure.

Fig. 2 illustrates the block structure of TQT1-PLL. Unlike the conventional QT1-PLL as shown in Fig. 1, the TQT1-PLL operates three cascaded MAFs in its control loop as shown in Fig. 2. Thus, the TQT1-PLL significantly enhances the disturbance rejection ability of conventional QT1-PLL in case of frequency drifts.

As known, in standard QT1-PLL, the window length of MAF is $T/2$ (here, T denotes fundamental grid period). Therefore, the window length of each MAF in TQT1-PLL is $T/6$ so that it has an equivalent phase delay as the standard QT1-PLL. The MAF with window length of $T/6$ (hereafter referred to as $\text{MAF}_{T/6}$) is responsible for eliminating the harmonics of order -5, +7, -11, +13, etc. which are the most dominant disturbances in three phase systems.

Notice that the $\text{MAF}_{T/6}$ cannot block the fundamental frequency negative sequence (FFNS) component which occurs under unbalanced grid conditions such as phase-ground fault, phase-phase fault, etc. Authors in TQT1-PLL have proposed a simplified second-order fast delayed signal cancellation in its prefiltering stage to eliminate the FFNS component [16]. This undesired component can be easily removed by different procedures before the control loop of PLL [8], [17], [18], [23]–[26]. So, in our study, blocking of the FFNS component is not considered.

It is known that a single $\text{MAF}_{T/6}$ can totally eliminate the dominant harmonics at fundamental grid frequency; however, it cannot effectively block these disturbances in case of frequency variations. To deal with this challenge, the $\text{MAF}_{T/6}$ can be made frequency-adaptive. But adaptive $\text{MAF}_{T/6}$ causes nonlinearity and instability problems and has heavy computational burden. Moreover, the parameter design process of PLL becomes difficult because of its structural complexity [8], [19]. For this reason, non-adaptive MAFs are recommended in literature.

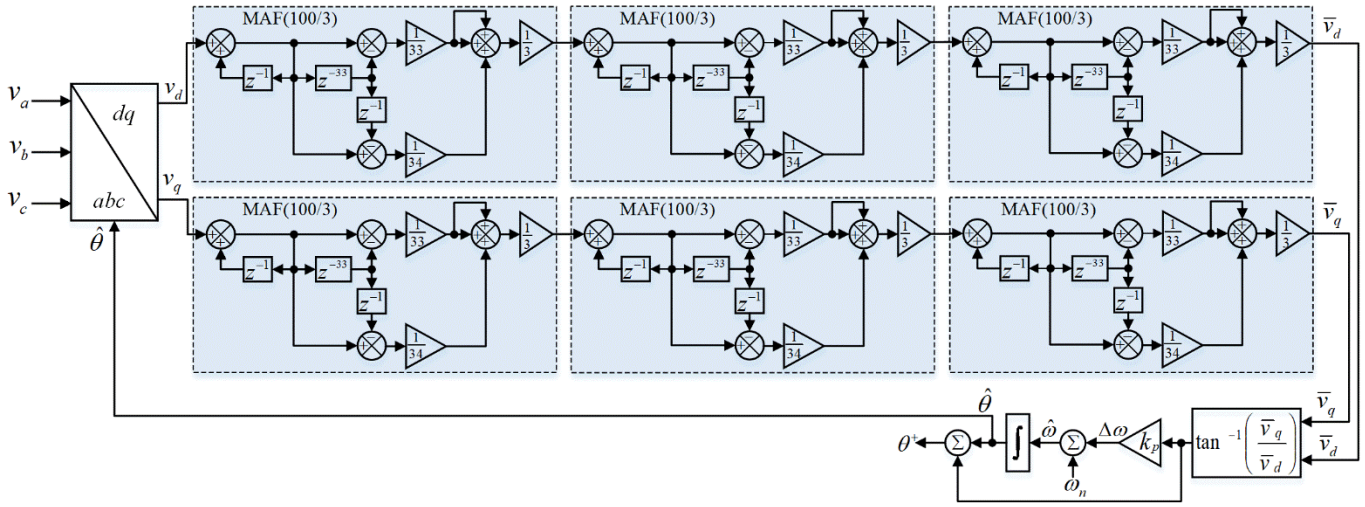

Fig. 2. Block diagram of TQT1-PLL.

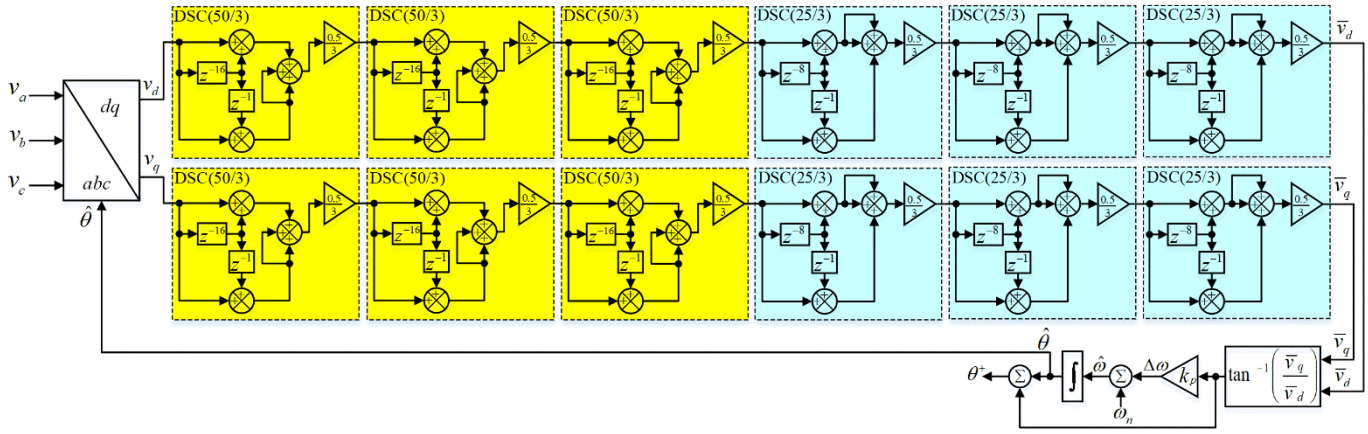

Fig. 3. Schematic of proposed HDSC-PLL.

On the other hand, a single $\mathrm{MAF}_{T/6}$ cannot completely remove the dominant harmonics if frequency varies from its nominal value. As mentioned before, using several cascaded non-adaptive MAFs with same window length improve the filtering ability of system against frequency deviations. Therefore, as shown in Fig. 2, the TQT1-PLL includes three non-adaptive MAFs in its control loop.

For grid frequency $f = 50$ Hz and sampling frequency $f_s = 10$ kHz, order of MAF (N_{MAF}) in standard QT1-PLL equals to 100 ($N_{MAF} = T_\omega f_s$ and here, T_ω denotes the window length of MAF). Note that N_{MAF} must be an integer value to realise the MAF in digital implementation as follows

$$\mathrm{MAF}\left(N_{MAF}\right) = \frac{1}{N_{MAF}} \frac{1 - z^{-N_{MAF}}}{1 - z^{-1}} \tag{1}$$

Nevertheless, in TQT1-PLL, N_{MAF} of each MAF is equal to 100/3, which is a non-integer value. To overcome this issue, MAF(100/3) can be calculated as

$$\mathrm{MAF}\left(\frac{100}{3}\right) = \frac{2\mathrm{MAF}(33) + \mathrm{MAF}(34)}{3} \tag{2}$$

where, two MAFs with $N_{MAF} = 33$ and one MAF with $N_{MAF} = 34$ are considered. Thus, in order to implement the MAF(100/3) as shown in Fig. 2, no fractional delay is used.

If the sampling frequency is chosen as a multiple of three for the fundamental frequency of 50 Hz (i.e., $f_s = 3m$ kHz, $m = 1, 2, 3, \ldots$), N_{MAF} becomes an integer. In this way, MAF structures in TQT1-PLL can be designed more simply.

III. Proposed HDSC-PLL

A. Description

As stated in the previous section, three cascaded $\mathrm{MAF}_{T/6}$ in TQT1-PLL cause a $0.5T$ delay in its dynamic response. To enhance the dynamic performance of the standard QT1-PLL without reducing its harmonic rejection ability, HDSC-PLL is proposed in Fig. 3. As shown, the DSC operators are suggested instead of MAFs in TQT1-PLL.

DSC operator is a kind of finite impulse response filter, and its transfer function is expressed in dq-frame as [27]

$$dq\mathrm{DSC}_n\left(s\right) = 0.5\left(1 + e^{\frac{-T}{n}s}\right) \tag{3}$$

where n and T are the delay factor and fundamental period of input signal, respectively. The schematic of dqDSC operator in discrete time is given in Fig. 4, here N_{DSC} is identified as [28]

$$N_{DSC} = \frac{T}{nT_s} \tag{4}$$

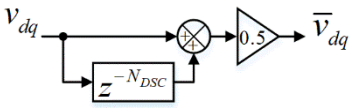

Fig. 4. Discrete time implementation of *dq*DSC operator.

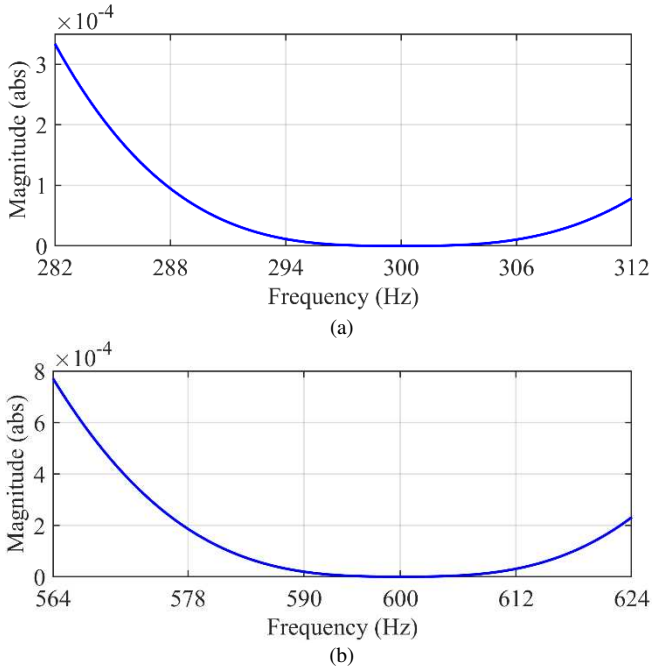

Fig. 5. Gains of third-order $dq\text{DSC}_{12}$ and $dq\text{DSC}_{24}$ operators under frequency drift. (a) Zoom view of third-order $dq\text{DSC}_{12}$. (b) Zoom view of third-order $dq\text{DSC}_{24}$.

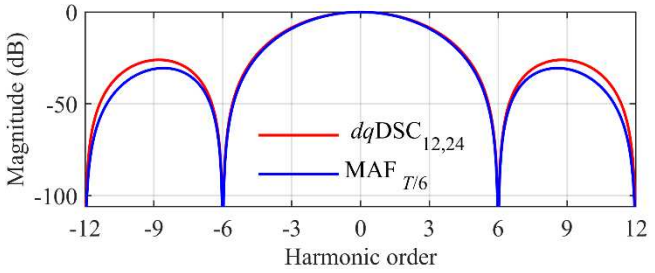

Fig. 6. Frequency response of $\text{MAF}_{T/6}$ and $dq\text{DSC}_{12,24}$ operators.

where T_s denotes the sampling time. As observed from Fig. 4, the *dq*DSC operator has a very simple structure and is easy to carry out in digital applications.

The HDSC-PLL consists of third-order *dq*DSC operators with a delay factor of 12 (briefly referred to as $dq\text{DSC}_{12}$) to remove the harmonics of order -5, +7 as shown in Fig. 5(a). In addition to these operators, it has third-order DSC operators with a delay factor of 24 (briefly referred to as $dq\text{DSC}_{24}$) to block the harmonics of order -11, +13 as shown in Fig. 5(b).

The harmonics of order -5, +7 in *dq*-frame correspond to 300 Hz while the harmonics of order -11, +13 in *dq*-frame correspond to 600 Hz for the fundamental grid frequency of 50 Hz. Notice that Fig. 5 is plotted in the fundamental frequency range of 47–52 Hz, which are the allowable frequency variations according to the European standard EN50160 [29]. Hereby, using cascaded non-adaptive DSC operators enhance the filtering capability of PLL against frequency drifts.

For grid frequency $f = 50$ Hz and sampling frequency $f_s = 10$ kHz, using (4), N_{DSC} values of $dq\text{DSC}_{12}$ and $dq\text{DSC}_{24}$ are calculated as 50/3 and 25/3, respectively. In other words, $\text{MAF}_{T/6}$ in TQT1-PLL and cascaded $dq\text{DSC}_{12}$ and $dq\text{DSC}_{24}$ operators in proposed HDSC-PLL have almost the same filtering capability. Hereafter, cascaded $dq\text{DSC}_{12}$ and $dq\text{DSC}_{24}$ operators are referred to as $dq\text{DSC}_{12,24}$ operators. To better visualise this fact, the frequency response of $\text{MAF}_{T/6}$ and $dq\text{DSC}_{12,24}$ operators is demonstrated in Fig. 6. Note that the harmonics of order -5, +7, -11, and +13 in $\alpha\beta$-frame turn into the harmonics of order -6, +6, -12, and +12 in *dq*-frame, respectively [18]. As observed from Fig. 6, there is no difference between $\text{MAF}_{T/6}$ and $dq\text{DSC}_{12,24}$ operators in terms of filtering out dominant harmonics; however, the proposed HDSC-PLL has two significant advantages over TQT1-PLL.

1) In TQT1-PLL, as the window length of each MAF is $T/6$, third-order MAFs cause a $T/6 + T/6 + T/6 = 0.5T$ delay. On the other hand, each $dq\text{DSC}_{12}$ and $dq\text{DSC}_{24}$ operators have a $T/12$ and $T/24$ delay, respectively, the $dq\text{DSC}_{12,24}$ operators cause a $(3T/12 + 3T/24) = 0.375T$ delay. As a result, the HDSC-PLL is the better option in terms of phase delay.

2) The proposed PLL has a lower memory requirement. Although MAF structures in TQT1-PLL require a total of 210 samples in digital signal processor (DSP) memory in practice, the $dq\text{DSC}_{12,24}$ structures in the proposed HDSC-PLL have a total of 156 samples in DSP memory. The memory requirement of the HDSC-PLL is also less than the standard QT1-PLL. The MAF structures in QT1-PLL require a total of 202 samples.

As mentioned before, N_{DSC} values of $dq\text{DSC}_{12}$ and $dq\text{DSC}_{24}$ are equal to 50/3 and 25/3, respectively, which are not integer values. So, to perform the $dq\text{DSC}_{12,24}$ operators in digital implementation as shown in Fig. 3, $dq\text{DSC}_{12}$ operator [briefly, DSC(50/3)] and $dq\text{DSC}_{24}$ operator [briefly, DSC(25/3)] are calculated as

$$\text{DSC}\left(\frac{50}{3}\right) = \frac{2\text{DSC}(17) + \text{DSC}(16)}{3} \tag{5}$$

$$\text{DSC}\left(\frac{25}{3}\right) = \frac{2\text{DSC}(8) + \text{DSC}(9)}{3} \tag{6}$$

If the sampling frequency is selected as a multiple of six for the fundamental frequency of 50 Hz (i.e., $f_s = 6m$ kHz, $m = 1, 2, 3, \ldots$), N_{DSC} becomes an integer. Thus, DSC operators in HDSC-PLL can be designed more simply as illustrated in Fig. 4.

B. Parameter Design Procedure

To set the control parameter of the proposed HDSC-PLL, its small-signal model is often preferred. Besides, this model is used for evaluating its stability analysis. Fig. 7 illustrates the small-signal model of HDSC-PLL. As observed, only simple gain (k_p) is adjusted.

Based on the small-signal model in Fig. 7, open-loop transfer function of proposed PLL can be determined as

$$\begin{aligned} G_{ol}(s) &= \frac{\Delta\theta^{+}(s)}{\theta_e(s)} \\ &= \left(\frac{\left(dq\text{DSC}_{12}(s)\right)^3\left(dq\text{DSC}_{24}(s)\right)^3}{1-\left(dq\text{DSC}_{12}(s)\right)^3\left(dq\text{DSC}_{24}(s)\right)^3}\right)\left(1+\frac{k_p}{s}\right) \end{aligned} \tag{7}$$

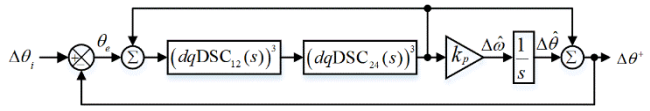

Fig. 7. Small-signal model of proposed HDSC-PLL.

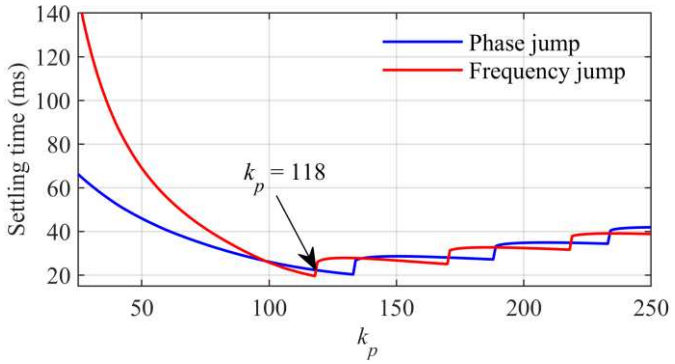

Fig. 8. 2% settling time of (8) as a function of k_p under phase and frequency jumps.

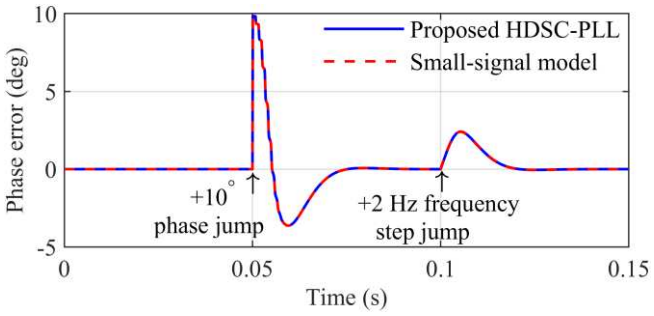

Fig. 9. Accuracy evaluation of the small-signal model.

Using (7), the transfer function of phase-tracking-error is expressed as

$$G_e(s) = \frac{\theta_e(s)}{\Delta\theta_i(s)} = \left(\frac{1}{1+G_{ol}(s)}\right) \tag{8}$$

Based on (8), the phase error under a phase jump ($\Delta\theta$) is obtained as

$$\Theta_e^{\Delta\theta}(s) = \frac{\Delta\theta}{s} G_e(s) \tag{9}$$

Again, using (8), the phase error under a frequency jump ($\Delta\omega$) is calculated as

$$\Theta_e^{\Delta\omega}(s) = \frac{\Delta\theta}{s^2} G_e(s) \tag{10}$$

The change of the 2% settling-time of (9) and (10) as a function of k_p under phase and frequency jumps is plotted as illustrated in Fig. 8. As shown, k_p is chosen as 118, which provides optimum settling-time for phase and frequency jumps. After determining k_p, the model accuracy of HDSC-PLL can be evaluated. Fig. 9 compares the performance of the real model in Fig. 3 and its model in Fig. 7. As observed, its model has a superior accuracy in predicting the HDSC-PLL dynamics.

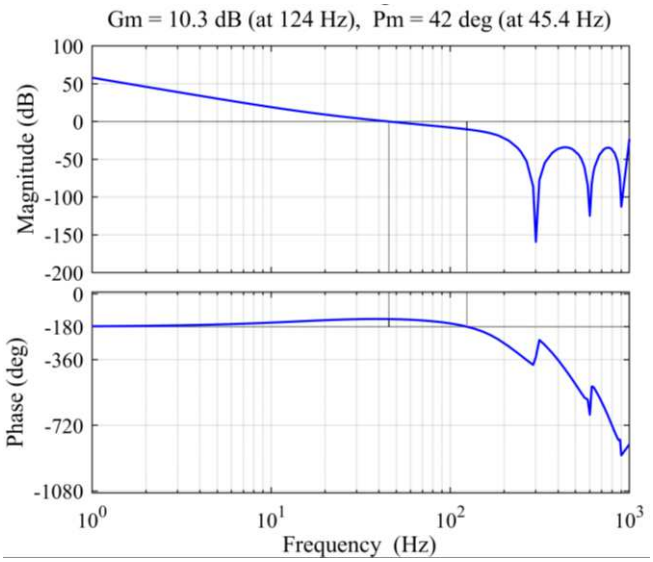

Fig. 10. Bode plot of HDSC-PLL.

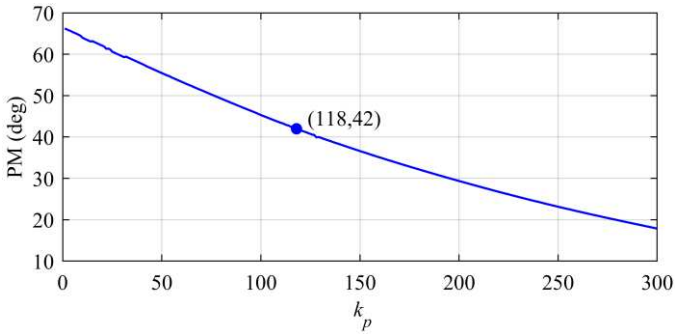

Fig. 11. PM variations as a function of k_p.

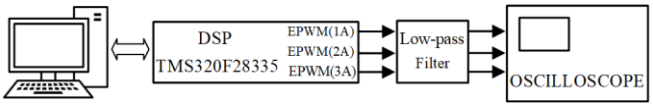

Fig. 12. Experimental setup.

C. *Stability Analysis*

To analyse the stability of proposed HDSC-PLL, its open-loop transfer function in (7) is usually used. Fig. 10 demonstrates the bode diagram of (7). As shown, its gain margin (GM) and phase margin (PM) are obtained as 10.3 dB and 42°, respectively. Besides, using the open-loop transfer function of proposed PLL, its PM variations as a function of k_p can be obtained as illustrated in Fig. 11. As observed that the PM is obtained as 42° corresponding to the selected k_p value. It can be seen that the results in Fig. 10 and Fig. 11 overlap with each other. Mostly, the PM within the range of 30−60° is suggested. As can be understood from Fig. 10 and Fig. 11, the HDSC-PLL ensures the system stability.

IV. Experimental Results

This part evaluates the effectiveness of suggested HDSC-PLL via several experiments. Fig. 12 demonstrates the experimental setup. For the sake of convenience, the virtual grid voltages and PLL methods used in comparison are operated by a TMS320F28335 DSP development board [30].

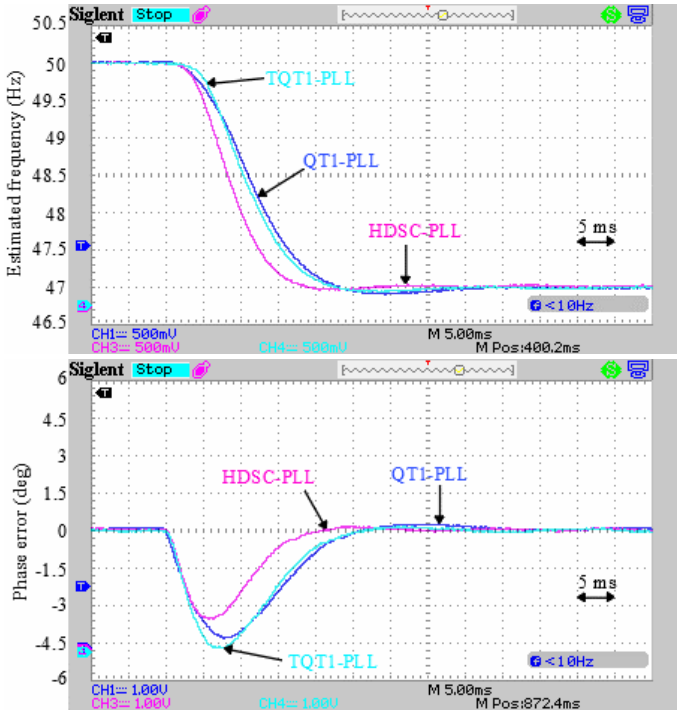

Fig. 13. Test-1: Experimental results under a –3 Hz frequency step change.

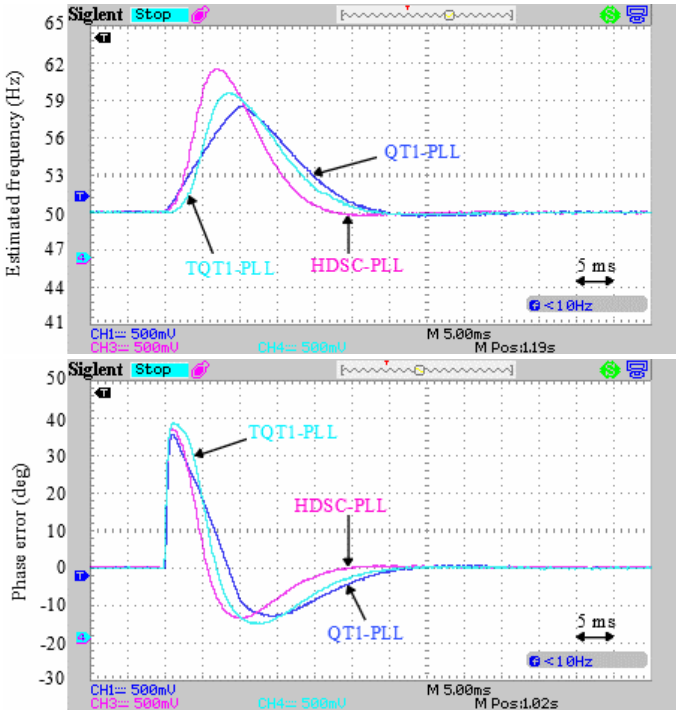

Fig. 14. Test-2: Experimental results under a +40° phase jump.

TABLE I
NUMERICAL RESULTS OBTAINED IN EXPERIMENTS

	HDSC-PLL	QT1-PLL [15]	TQT1-PLL [16]	DSOGI-PLL [31]	MAF-PLL [19]
Test-1					
2% settling time	16.9 ms (0.85 cycles)	35.1 ms (1.75 cycles)	21.2 ms (1.06 cycles)	52.8 ms (2.64 cycles)	59.3 ms (2.96 cycles)
Frequency overshoot	0.056 Hz (1.87%)	0.09 Hz (3%)	0.054 Hz (1.8%)	1.32 Hz (44%)	0.026 Hz (0.87%)
Phase overshoot	3.7°	4.4°	4.7°	7.6°	11.4°
Test-2					
2% settling time	22.3 ms (1.12 cycles)	30 ms (1.5 cycles)	28 ms (1.4 cycles)	42.8 ms (2.14 cycles)	73.3 ms (3.67 cycles)
Frequency overshoot	11 Hz	8.75 Hz	9.73 Hz	13.4 Hz	3.4 Hz
Phase overshoot	14.6° (36.5%)	13.5° (33.75%)	15.6° (39%)	15.4° (38.5%)	14.3° (35.8%)
Test-3					
2% settling time	17.5 ms (0.88 cycles)	-	21.7 ms (1.09 cycles)	-	59.1 ms (2.96 cycles)
Peak-to-peak frequency error	≈ 0 Hz	0.094 Hz	≈ 0 Hz	0.46 Hz	≈ 0 Hz
Peak-to-peak phase error	≈ 0°	0.364°	≈ 0°	0.09°	0.01°
Phase margin (PM)	42°	45°	38.8°	44.76°	43.3°

During the experiments, sampling frequency and amplitude of the grid voltages are tuned as 10 kHz and 1 p.u., respectively. As shown in Fig. 12, to monitor the signals of estimated grid frequency and phase angle error on an oscilloscope, these signals obtained from the enhanced pulse width modulator (ePWM) are passed through the external low-pass filter.

To show the performance of suggested HDSC-PLL, standard QT1-PLL and TQT1-PLL are also implemented in DSP and their performances are compared with those of the suggested technique. The parameter k_p of QT1-PLL and TQT1-PLL is set as in [15], where k_p is 92.34. Furthermore, the HDSC-PLL is also compared to the DSOGI-PLL [31] and MAF-PLL [19]. Note that the numerical results of these PLLs are given in Table I. This table also provides PM comparison between all PLL methods. As can be understood, all PLLs provide the system stability.

Three tests are designed as follows.

- *Test*-1: The grid frequency changes from its nominal value (50 Hz) to 47 Hz, which is the lowest allowed frequency according to the Std. EN50160 [29].
- *Test*-2: A +40° phase jump occurs at grid voltages. The frequency is fixed to 50 Hz.
- *Test-3*: The harmonic disturbances are injected to grid voltages. The magnitude of harmonics of order -5, +7, -11 is taken to be 0.04 p.u., and the magnitude of harmonic of order +13 is taken to be 0.02 p.u. according to IEEE 1547-2018 standard [32], which are the maximum permissible magnitudes. To test the harmonic rejection ability of PLLs in case of frequency drift, the frequency varies from 50 Hz to 52 Hz abruptly.

Fig. 13 illustrates the experimental results for test 1. The proposed HDSC-PLL presents a speedier transient response and a smaller phase overshoot than both standard QT1-PLL and TQT1-PLL.

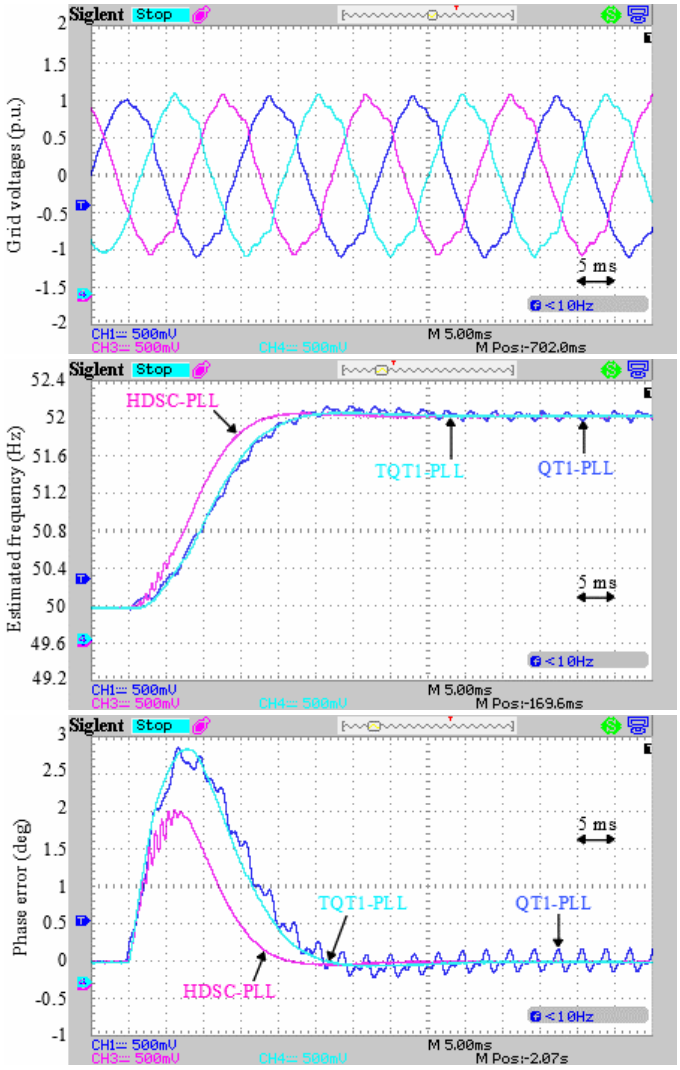

Fig. 15. Test-3: Experimental results under harmonically distorted grid voltages with a +2 Hz frequency step change.

The convergence time of HDSC-PLL is less than one period of nominal frequency. Table I shows the detailed numerical results of the compared methods. As can be understood from this table, the settling-time of proposed HDSC-PLL is around 16.9 ms (0.85 cycles). On the other hand, the settling-times of the QT1-PLL, TQT1-PLL, DSOGI-PLL, and MAF-PLL are around 35.1 ms (1.75 cycles), 21.2 ms (1.06 cycles), 52.8 ms (2.64 cycles), and 59.3 ms (2.96 cycles), respectively. The phase overshoot of QT1-PLL, TQT1-PLL, DSOGI-PLL, and MAF-PLL are 4.4°, 4.7°, 7.6°, and 11.4°, respectively. However, the proposed HDSC-PLL has a relatively small phase overshoot of 3.7%.

Fig. 14 demonstrates the experimental results for test 2. As observed from Fig. 14, the HDSC-PLL offers a faster dynamic performance than QT1-PLL and TQT1-PLL. Also, the detailed experimental results can be found in Table I. As can be seen from the table, the settling-time of proposed PLL is 22.3 ms whereas the settling-times of the QT1-PLL, TQT1-PLL, DSOGI-PLL, and MAF-PLL are 30 ms, 28 ms, 42.8 ms, and 73.3 ms, respectively. From the point of phase overshoot, the HDSC-PLL's response is moderate; however, its frequency overshoot is slightly bigger than that of the other PLLs except DSOGI-PLL. This overshoot can be considerably compensated by using the adaptive mechanism suggested in [33].

Fig. 15 illustrates the experimental results for test 3. The proposed HDSC-PLL and TQT1-PLL, thanks to their cascaded filtering mechanisms, demonstrate an excellent harmonic rejection ability even in case of frequency drift. They have no frequency and phase errors. The standard QT1-PLL, however, causes a large error in frequency and phase estimation. As given in Table I, peak-to-peak frequency errors of the QT1-PLL, DSOGI-PLL, and MAF-PLL are 0.094 Hz, 0.46 Hz, and approximately 0 Hz. Their phase errors are 0.364°, 0.09°, and 0.01°, respectively.

Grid-connected converters are required to satisfy the IEEE 1547-2018 standard [32], which specifies that the total harmonic distortion (THD) should be below 5% together with a specific limit on individual harmonic components. In this context, test 3 is particularly important to show the effectiveness of the proposed approach on improving power quality (PQ) issues. As shown in Fig. 15, the proposed technique has zero steady-state error in frequency and phase estimation despite the grid being heavily distorted, which could happen if highly nonlinear loads are suddenly connected to the grid [34].

V. Conclusion

In this work, a high-order delayed signal cancellation-based PLL (shortly named the HDSC-PLL) for the fast and accurate detection of the grid voltages under harmonically distorted grid conditions was suggested. The high-order DSC operators in the proposed HDSC-PLL consist of third-order $dq\text{DSC}_{12}$ operator and third-order $dq\text{DSC}_{24}$ operator to enhance the filtering ability of the suggested method under frequency drifts. The effectiveness of the HDSC-PLL was tested by a comparative performance evaluation with standard QT1-PLL and TQT1-PLL. The results from the experiments show that the HDSC-PLL exhibits a high filtering ability and a fast dynamic response. In terms of improving the dynamic performance of QT1-PLL, the proposed HDSC-PLL is superior to TQT1-PLL. It has approximately 5 ms less settling-time than TQT1-PLL. Furthermore, it requires a low memory requirement. Consequently, the proposed PLL is a better option compared to TQT1-PLL for improving the dynamic performance of standard QT1-PLL.

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