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Experimental Demonstration of a 1.2-kV Trench Clustered Insulated Gate Bipolar Transistor in Field-Stop Technology

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***Abstract*— In this paper a 1.2 kV, 50 A trench clustered IGBT is experimentally demonstrated in field-stop technology for the first time. Due to the optimized field stop layer design, the off-state leakage current is lower than 1 mA at 175°C. A low on-state voltage drop of 1.6 V is achieved at 150°C. The saturation current levels are effectively controlled by the self-clamping feature. Moreover, experimental results confirm that the fabricated devices exhibit dynamic avalanche-free switching performance as well as high dV/dt controllability.**

Keywords—IGBT, Clustered IGBT, field-stop technology, dynamic avalanche, dV/dt controllability

I. Introduction

The development of silicon IGBTs has always been targeting higher power efficiency and higher current handling capability for design optimization and cost reduction of power converter systems. Significant progress has been achieved by the introduction of trench geometry [1], Field-Stop (FS) technology [2] and Injection Enhancement (IE) effect [3] over the past three decades. However, further improvements in terms of on-state performance, switching frequency and long-term reliability are becoming difficult to realize. This is because Dynamic Avalanche (DA) plays a key factor in limiting the high current density operation capability [4-7]. To break the fundamental limits of conventional IGBTs and remain competitive against Wide Band Gap (WBG) power devices, innovative silicon technologies must be implemented in a reliable way to achieve DA free operations and significant reduction in power losses, while maintaining the cost competitivity of silicon compared to WBG alternatives. This is because DA-free operation can enable reduction in the gate resistance, reducing switching losses and enhancing reliability. The Trench Clustered IGBT (TCIGBT) is the only DA-free solution that has been experimentally proven so far [7-11]. Its self-clamping feature and PMOS operation are effective in managing the peak electric field distribution beneath trench gates. In addition, the inherent thyristor operation offers much lower on-state losses even when comparing the NPT-TCIGBT to the FS-IGBT [10, 11]. Therefore, TCIGBT provides a highly promising solution to move beyond the limits of current IGBT technologies.

In this paper, the electrical characteristics of the 1.2 kV, 50 A TCIGBT in field-stop technology are presented through experiments for the first time. The experiments were carried out at room temperature and at 150°C. Detailed analysis of the temperature dependence of leakage currents is studied with various anode doping profiles. Moreover, the thyristor effect is evaluated under different N-well injection efficiencies. Finally, the switching characteristics show that the FS-TCIGBT remain DA-free and with high dV/dt controllability.

II. Device Design and Cell Structure

The FS-TCIGBTs were fabricated on 8-inch wafers with a thickness of 140 µm. The photograph of a fabricated device is shown in Fig. 1. It features a central gate design and the cluster cells are paralleled within the active area. Fig. 2 shows the top view of the cathode design while Fig. 3 shows the SEM image of the cathode structure. As shown, the cathode cells feature a ladder design with several stripe trenches running in parallel across the cluster cells. The n^+ cathodes are penetrated by the p^+ cathodes to suppress latch-up. The 3-D cross-sectional view of a unit cell is shown in Fig. 4. The TCIGBT features a MOS-gated thyristor structure, which consists of P-anode, N-drift, P-well and N-well. The detailed mechanisms of turn-on, self-clamping feature and PMOS actions have been explained in [10, 12]. Moreover, the dummy regions are connected to the emitter, which provides a direct path for excessive holes to be evacuated during turn-off. The field-stop layer is implanted after the wafer is thinned to 140 µm.

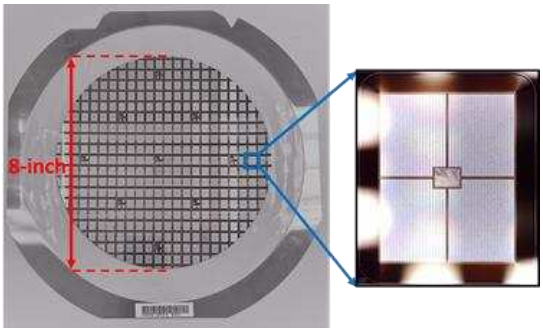

Fig. 1. Photography of the fabricated devices on an 8-inch wafer.

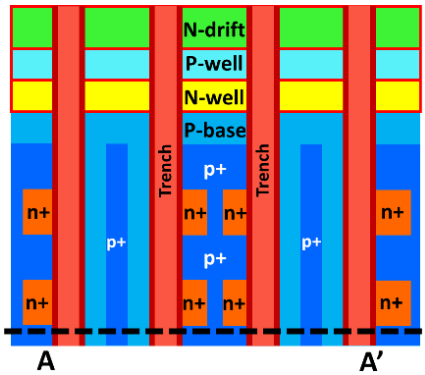

Fig. 2. Top view of the cathode design.

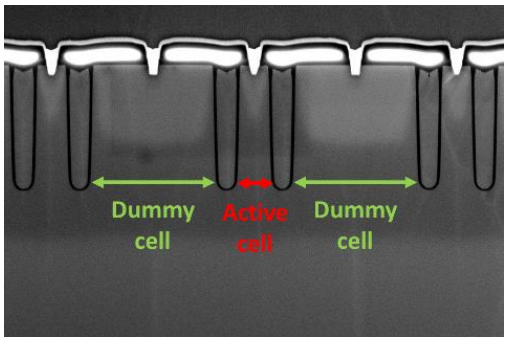

Fig. 3. SEM image of the cut line A-A' shown in Fig. 2.

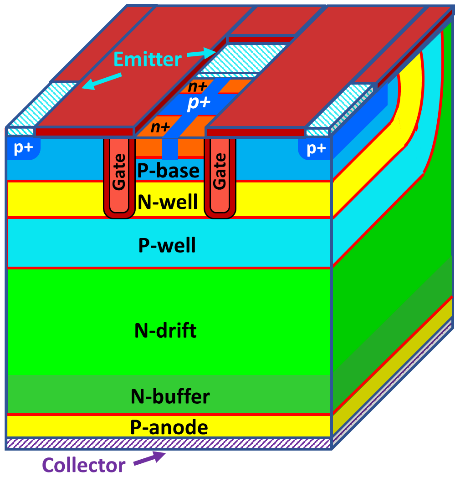

Fig. 4. 3-D cross-sectional view of the FS-TCIGBT unit cell.

III. Experimental Results

A. Breakdown Characterisitcs

Fig. 5 shows the breakdown characteristics of the FS-TCIGBT at room temperature while Fig. 6 shows the temperature dependence of leakage current levels. As shown, the device can withstand more than 1600 V at room temperature with less than 10 nA leakage current at 1200 V. Due to the optimization of the buffer design, the device can maintain low leakage currents even at 175°C. As the anode engineering plays a key role in determining the leakage current levels, the influence of N-buffer and P-anode doping levels on leakage currents are studied in detail. Fig. 7 shows the SRP results of the N-buffer doping profiles at various implant energy conditions. Laser annealing is employed to activate the dopant after implantation without affecting the front-side doping profiles. It is shown that higher implant energy results in a deeper N-buffer layer, which reduces the leakage currents at high temperatures, as shown in Fig. 8(a). However, Fig. 8(b) shows that the temperature dependence of leakage currents is independent of P-anode doping concentrations. Therefore, it can be concluded that the increase of leakage currents at high temperatures is mainly determined by the field-stop layer design.

B. Input Characterisitcs

Fig. 9 shows the input characteristics of the fabricated FS-TCIGBT at T_j = 25°C and T_j = 150°C. The threshold voltage (V_{th}) is designed to be 6.5 V at 100 mA at room temperature which reduces to 5 V at T_j = 150°C.

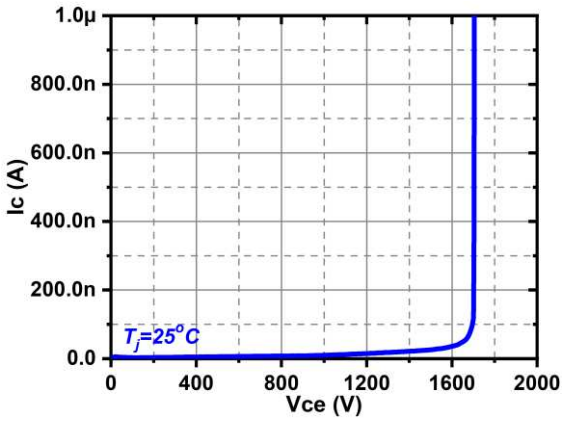

Fig. 5. Breakdown characteristics at room temperature.

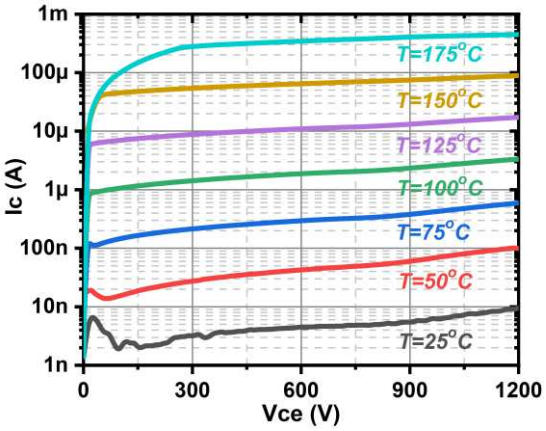

Fig. 6. Impact of temperature on leakage currents.

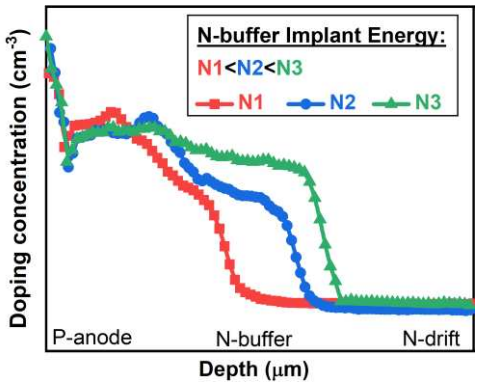

Fig. 7. SRP results for the anode-side doping profiles with various N-buffer implant energies.

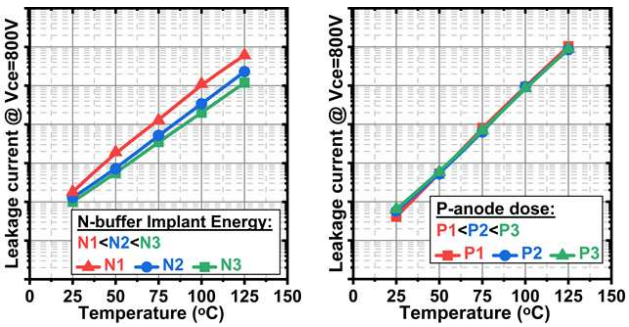

Fig. 8. Temperature dependence of leakage currents under (a) various N-buffer doping levels and (b) various P-anode doses.

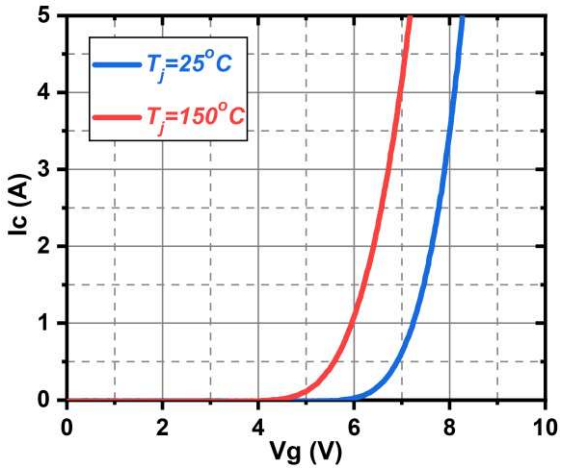

Fig. 9. Input characteristics at room temperature and at 150°C.

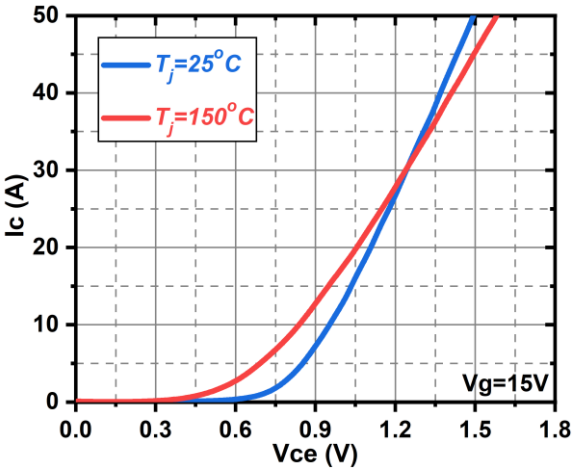

Fig. 10. I-V characteristics at room temperature and at 150°C.

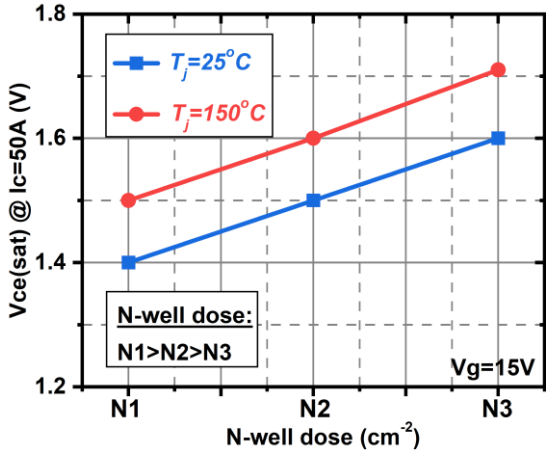

Fig. 11. Impact of the N-well dose on the on-state voltage drop.

C. I-V Characterisitcs

The *I-V* characteristics of the FS-TCIGBT at T_j = 25°C and T_j = 150°C are shown in Fig. 10. At V_g = 15 V, the on-state voltage drop ($V_{ce(sat)}$) at rated current 50 A are 1.5 V and 1.6 V at 25°C and 150°C, respectively. In contrast to the conventional IGBTs, which use the IE effect to lower the $V_{ce(sat)}$, the TCIGBT uses the thyristor effect to reduce the $V_{ce(sat)}$. Fig. 11 shows the impact of N-well dose on the $V_{ce(sat)}$.

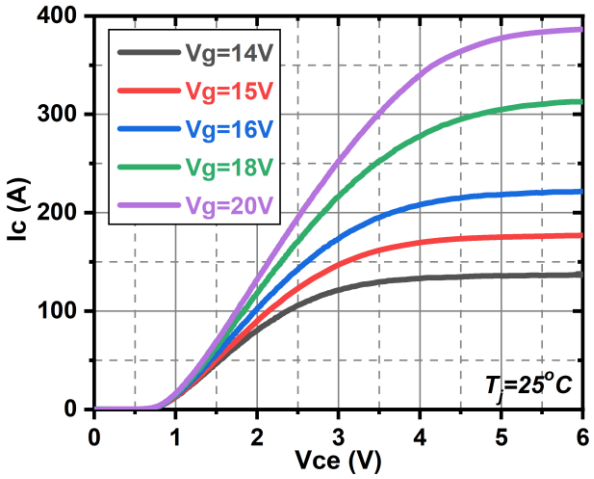

Fig. 12. Current saturation behavior at various gate voltages at room temperature.

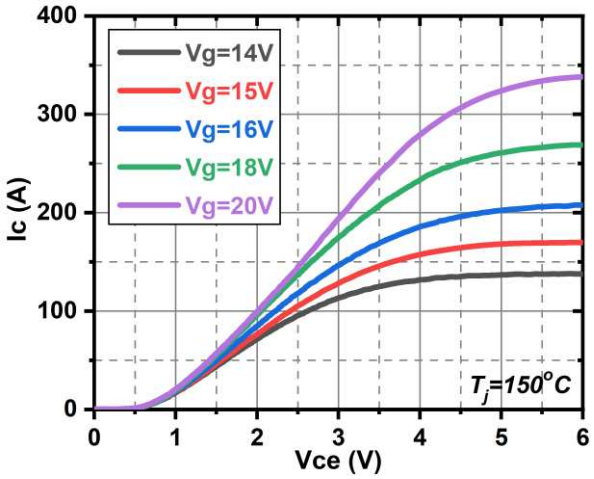

Fig. 13. Current saturation behavior at various gate voltages at 150°C.

A higher N-well dose results in a higher charge density of the N-well layer, which increases the current gain of the N-well/P-well/N-drift transistor. As a result, the thyristor effect is enhanced within the device during on-state, leading to a decreasing $V_{ce(sat)}$, as shown in Fig. 11.

D. Current Saturation Characterisitcs

As current saturation behaviour has a significant impact on short-circuit withstand capability, low saturation current densities (J_{sat}) are expected to improve the Short-Circuit Safe Operating Area (SCSOA). However, in IGBTs, there is a trade-off between $V_{ce(sat)}$ and J_{sat}. Several technologies including trench geometry [13] and scaling rules [14] can considerably improve the on-state behaviour of IGBTs but can significantly affect the short circuit capability due to increase in J_{sat}. In contrast, the unique self-clamping feature of TCIGBT enable control of the current saturation levels without affecting the on-state performance. Fig. 12 and Fig. 13 depict the current saturation behaviour of the FS-TCIGBT at various V_g at T_j = 25°C and 150°C, respectively. As shown, the saturation current is only 3.5 times higher than the rated current at 150°C. Due to the low saturation current, the devices have been tested to survive at least 10 µs during short circuit tests under a DC voltage of 800 V and T_j = 150°C.

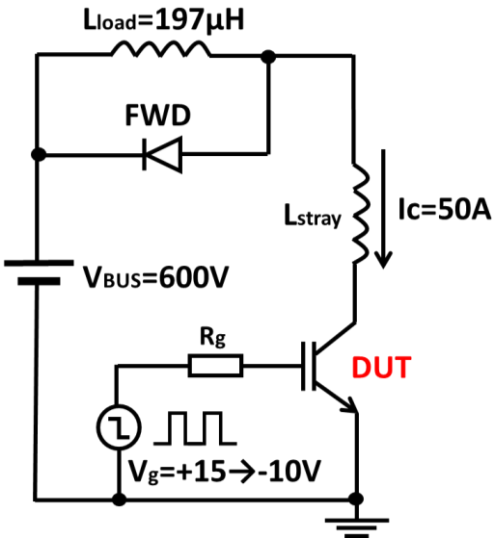

Fig. 14. Double pulse inductive switching test circuit configuration.

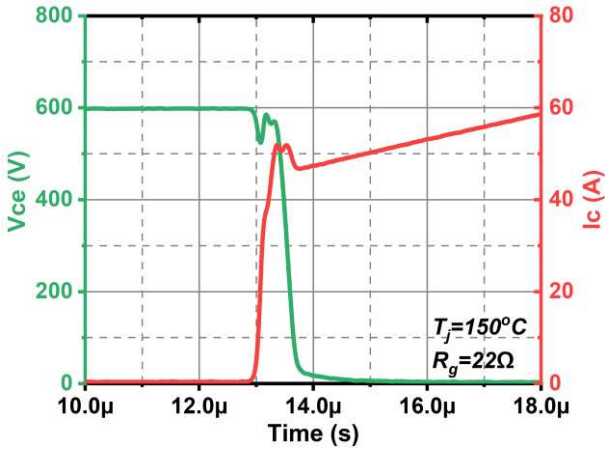

Fig. 15. Turn-on characteristics at 150°C.

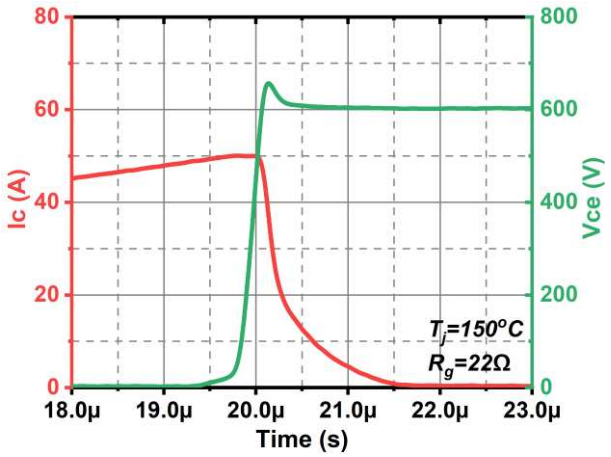

Fig. 16. Turn-off characteristics at 150°C.

E. Switching Characterisitcs

To evaluate the switching characteristics of the fabricated FS-TCIGBT, a double-pulse inductive switching test circuit is utilized to measure the turn-on and turn-off waveforms, as shown in Fig. 14. The DC supply voltage is 600 V and the load inductance is 197 μH. A silicon fast recovery diode is used as

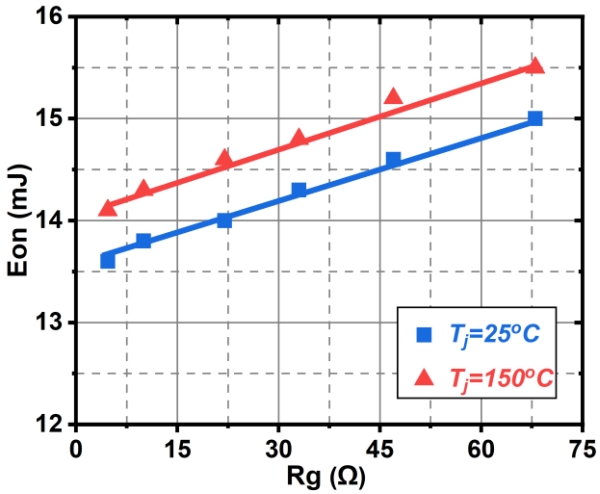

Fig. 17. Impact of R_g on turn-on switching losses.

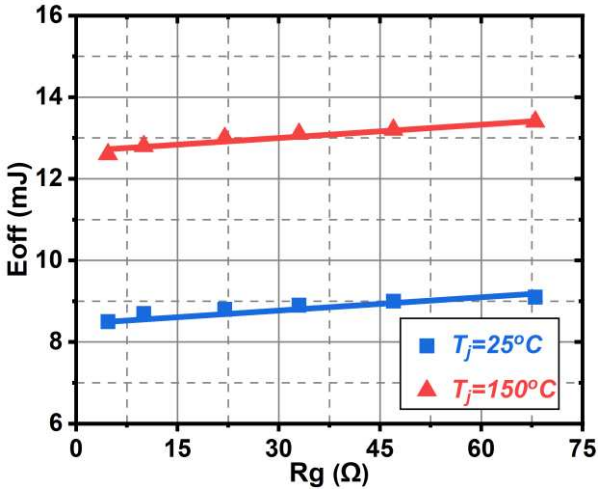

Fig. 18. Impact of R_g on turn-off switching losses.

the freewheeling diode. The experiments were carried out as a function of gate resistance (R_g) at T_j = 25°C and T_j = 150°C. Fig. 15 and Fig. 16 present the turn-on and turn-off switching waveforms of the FS-TCIGBT at R_g = 22 Ω and T_j = 150°C, respectively. The turn-on losses (E_{on}) as a function of R_g is shown in Fig. 17 while the turn-off losses (E_{off}) as a function of R_g is shown in Fig. 18. As shown, the E_{off} shows linear decreases with reducing R_g, which confirms that FS-TCIGBT is free from Dynamic Avalanche (DA). The results also show that the E_{off} and the E_{on} can be simply minimized by reducing R_g without DA-related concerns. In addition to low switching losses, high dV/dt controllability is also crucial to meet various IGBT applications as the switching slopes (dV/dt) are typically restricted to 5 kV/μs due to inherent limitation of the isolation systems in motors [15]. Fig. 19 and Fig. 20 depict the influence of R_g on turn-on dV/dt and turn-off dV/dt at room temperature and T_j = 150°C, respectively. As shown, both turn-on and turn-off dV/dt values can be easily controlled by adjusting the gate resistance and the maximum dV/dt does not exceed the typical limits for motor drives. Therefore, the FS-TCIGBT provides flexible design for inverter manufacturers.

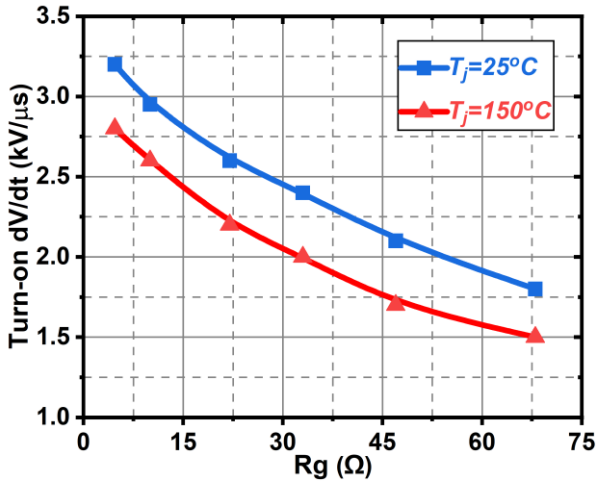

Fig. 19. Impact of R_g on turn-on dV/dt.

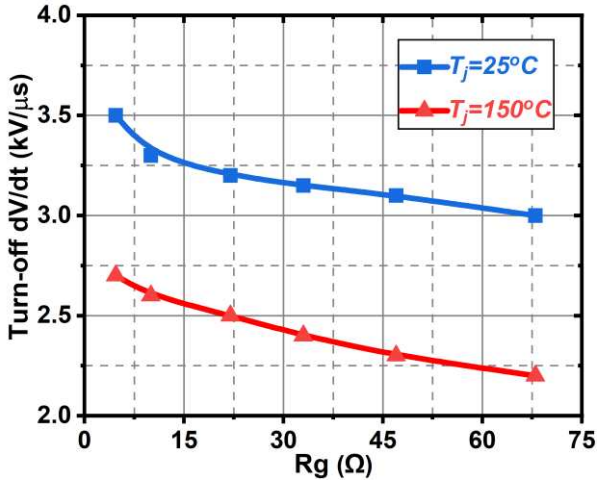

Fig. 20. Impact of R_g on turn-off dV/dt.

IV. Conclusions

The electrical characteristics of the newly developed 1.2 kV, 50 A Trench Clustered IGBT (TCIGBT) in Field-Stop technology are investigated under room temperature and T_j = 150°C. With the optimization of buffer design, the FS-TCIGBT remains low leakage current levels even at T_j = 175°C. Due to the inherent thyristor effect, a low on-state voltage drop of 1.5 V can be achieved at room temperature. Furthermore, the FS-TCIGBT shows dynamic avalanche-free switching performance as well as high dV/dt controllability under low R_g conditions. These features enable operation at high current densities with low power losses while maintaining the cost-competitivity of silicon technologies. With the further optimization of cathode design, the power density and efficiency of FS-TCIGBTs are expected to be further enhanced.

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