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Highly Efficient 3-Bit Digital Power Amplifier for OFDM Waveform Amplification

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***Abstract*— In this work, we present a digital power amplifier (DPA) and a signal-optimized control technique suitable for the amplification of orthogonal frequency division multiplexing (OFDM). OFDM is a high peak-to-average power ratio (PAPR) signal that is naturally arising from high spectrum efficiency modulations. A 3-bit DPA is implemented with three power-scaled transistors which are turned on and off based on the signal amplitude, while phase modulation is restored using the radio frequency (RF) input signal. The unavoidable nonlinearities at the DPA output due to PA switching are minimized by accounting for the OFDM signal probability density function (pdf). This pdf is *a priori* knowledge to design an optimal quantizer that minimizes distortion by distributing the DPA power levels where the signal amplitude is more similar to the original one. Back-off efficiency within $2^3 = 8$ possible states is then optimized by implementing a load-modulating power combiner. Theory and an example design of the combiner network are provided and demonstrated for this DPA. The reported DPA prototype operates at 1.5 GHz with a 3-bit control and achieves a maximum power-added efficiency (PAE) of 64.3% and maintains a drain efficiency greater than 47% over the output power range from 36.6 to 45.2 dBm (8.6-dB range).**

***Index Terms*— Digital power amplifier (DPA), linearity, load modulation, optimization, orthogonal frequency division multiplexing (OFDM), power efficiency.**

I. Introduction

POWER efficiency is one of the most challenging specifications in communication systems, especially in the emerging broadband cellular networks, where energy consumption leads to significant growth of the operators' power cost and carbon emissions [1]. Power amplifier (PA) is one of the most power-consuming radio frequency (RF) components within communication systems [2]. Maximizing power efficiency is challenging for PA designers. Orthogonal frequency division multiplexing (OFDM) is a nonconstant envelope-modulated waveform which improves spectrum efficiency, and it retains its promise in future networks [3]. However, a well-known problem of OFDM waveforms is the high peak-to-average power ratio (PAPR) signal [4]. Amplifying such high PAPR signals incurs steep penalties in power loss as most PAs function inefficiently at back-off.

To avoid such losses, designing a highly efficient PA is of utmost importance to address the significant energy challenges in communication systems. Well-known efficiency enhancement techniques to solve the back-off efficiency limitations of a single-transistor PA are outphasing, Doherty, and envelope tracking. Such techniques have been widely investigated [2], [5]–[8]. However, linearity degradation introduced by these efficiency enhancement architectures is challenging to overcome [2]. Moreover, implementing the outphasing and Doherty requires a narrowband phase shifter or power combiner [9]–[12]. Traditional envelope tracking PAs usually adopt dynamic power supplies [13] that can introduce instantaneous bandwidth limitations.

Another promising technique to enhance power efficiency is the digital PA (DPA). There exists a well-developed body of research in class-D switch capacitor PAs [14]. However, this approach is usually restricted to transmitting constant envelope waveforms, which is less spectrum-efficient than OFDM. To improve the back-off efficiency, paralleling multiple transistors are also intensively explored. The transistors are switched alternatively on and off to generate multiple efficiency peaks. However, they still mainly operate in a suboptimal linear region, and the output combining network dissipates most of the power [15], [16].

To maximize the power efficiency, switching mode multibit DPAs are also proposed [16]–[20]. A general switching mode multibit DPA consists of a baseband signal generator and distributor, upconverter, parallel DPA modules, power combiner, and baseband filter. The input baseband signal is modulated into parallel digital pulses. The constituent transistors switch between a peak efficient ON-state to a fully OFF-state to generate discrete output power levels.

However, switching mode DPAs shape the envelope signal into rectangular pulses containing a high-frequency content. The existing digital modulation schemes such as pulsewidth modulation [14] and delta–sigma modulation [21] keep the

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amplitude constant and encode the information into the width of the pulse. The main drawback of these modulation schemes is that they require a very high switching frequency compared with continuous amplitude modulation. Furthermore, these schemes are also generally limited by the minimum pulse duration [14], and this reduces the dynamic range. Therefore, modern wireless communication standards like OFDM use the nonconstant amplitude modulation to achieve linear and broadband amplification. To leverage the advantage of such nonconstant envelope modulation techniques, novel multibit DPA structures that combine their constituent PAs' output powers are proposed [22].

However, the modulated and amplified digital pulses generated at the output of a multibit DPA are a coarse approximation of the scaled-up original signal with a maximum difference equal to the least significant bit (LSB). The difference between them can be measured by the error vector magnitude (EVM) value, which is widely used as a metric for ascertaining transmitted waveform linearity. Another architecture to improve the back-off efficiency is the power-mixer array in which multiple PAs with the same RF power are paralleled. However, this approach is unsuited for high PAPR signals such as OFDM, whereas probability density function (pdf) is radically different from a uniform distribution [18]–[20].

This work presents a novel DPA architecture and control signal generation technique, which is suitable for high PAPR OFDM signals' efficiency and low-distortion amplification. This DPA uses three parallel PAs of different power levels (6, 15, and 25 W) combined through a load-modulating power combiner. The high efficiency of this DPA is also enabled using gallium nitride (GaN) transistors for a high switching speed with low losses compared with typical Si laterally diffused metal–oxide semiconductors (LDMOSs). To the best of the authors' knowledge, this is the first of its kind demonstration of a 3-bit DPA where analog-to-digital converter (ADC) quantization techniques are leveraged for linearity optimization in a 3-bit DPA. The inputs of the constituent PAs in the DPA are biased by applying quantized time-domain OFDM waveform while being driven by a continuous wave (CW) RF carrier. In other words, the digitally modulated information-bearing symbols are applied through an input gate bias modulation instead of an RF amplitude modulation, thus drastically simplifying the transmitter layout. Specifically, the contributions of this article are summarized as follows.

1) We propose a novel 3-bit DPA architecture with eight RF output power states, which can amplify the OFDM waveform with high efficiency and low distortion.
2) We provide an approach to optimize the linearity by selecting the output power levels through quantization of the OFDM envelope by considering the statistical distribution that minimizes the EVM.
3) DPA amplitude modulation is accomplished through a low-power gate bias switching of the constituent PAs in the DPA.
4) We design an optimized power combiner network that performs the load modulation of the constituent PAs to improve the back-off efficiency over a broad range of output powers.
5) Rigorous analytical modeling, systematic simulation, and fabrication are undertaken to validate the approach and characterize the performance of the DPA.

This article is organized as follows. Section II introduces the theoretical analysis and optimization of the proposed 3-bit DPA. In Section III, we explain the methodology and circuit implementation of the 3-bit DPA architecture. Section IV discusses the measurement results from the fabricated 3-bit DPA system. Finally, this article is concluded in Section V.

II. 3-Bit DPA

A. DPA Architecture

A block diagram of the proposed 3-bit DPA is illustrated in Fig. 1. A constant envelope phase-modulated RF input signal is fed to a three-way power combiner which splits the signal to three PAs. This power combiner is also designed to introduce the required phase difference between the inputs for maximum output power. The constituent PAs amplify the three signals concurrently, and their outputs are combined using a power combiner. All three PAs are connected to the same drain voltage of 28 V. Amplitude modulation is introduced by switching on and off the gate voltages. The goal here is to maximize the efficiency over a large back-off range. The eight output states mapping the constituent transistors into the eight DPA states are listed in the table of Fig. 1.

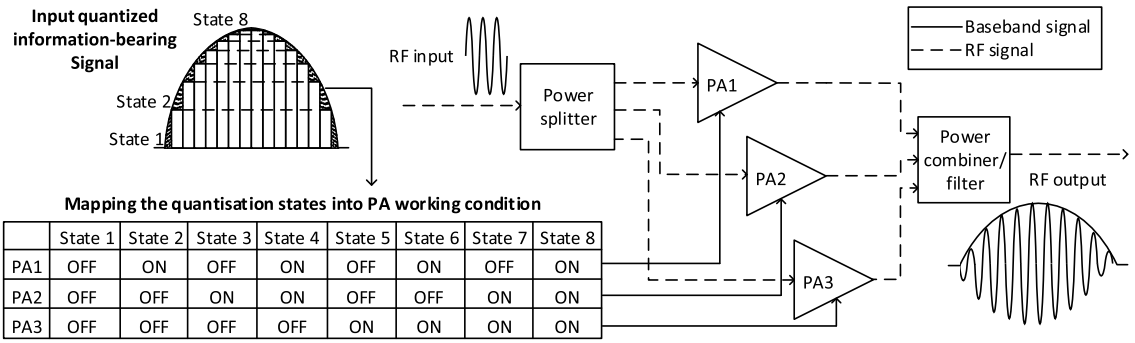
Theoretically, this architecture dramatically increases the output power range and system efficiency. Assuming there is no loss in the matching networks, power combiners, and splitters, the system efficiency can be very high. The three constituent PAs are continually driven in deep compression, thus with very high individual efficiency. The amplified waveform is quantized in eight output states, and the maximum quantization error is dictated by the LSB.

B. DPA Control Strategy

EVM is widely used as the metric for ascertaining transmitted RF waveform linearity [23]. Quantization noise occurs when a continuously varying signal is approximated with a finite number of levels [17]. In this work, we propose to consider the signal pdf to generate a quantization law that minimizes the EVM, on average. This is here done using the signal processing techniques of [24], [25] and optimization algorithms [26].

The input signal is partitioned into a discrete distribution after the quantization process. A period of time-varying signal and the pdf of a continuously distributed analog OFDM signal (input signal) are depicted in Fig. 2. Here, $\mathcal{X} \in \{x_1, \ldots, x_k, \ldots, x_K\}$ is the input signal partition set and $\mathcal{Y} \in \{y_1, \ldots, y_k, \ldots, y_K\}$ is the quantized output signal levels, also known as the codebook set. It is convention that an input signal between x_{k-1} and x_k has the corresponding output codebook y_k. In this article, the minimum codebook y_1 is set to zero since the minimum output power of the DPA is zero (when all the constituent PAs are turned off).

The EVM minimization for DPA in this article leverages the widely explored ADC quantization theory in [25]. First,



	State 1	State 2	State 3	State 4	State 5	State 6	State 7	State 8
PA1	OFF	ON	OFF	ON	OFF	ON	OFF	ON
PA2	OFF	OFF	ON	ON	OFF	OFF	ON	ON
PA3	OFF	OFF	OFF	OFF	ON	ON	ON	ON

Fig. 1. Simplified schematic of the 3-bit DPA architecture. The input amplitude-modulated signal is quantized with $2^3 = 8$ states which are used to turn on and off the three power-scaled PAs. The outputs of the PAs are combined to reconstruct the quantized envelope signal.

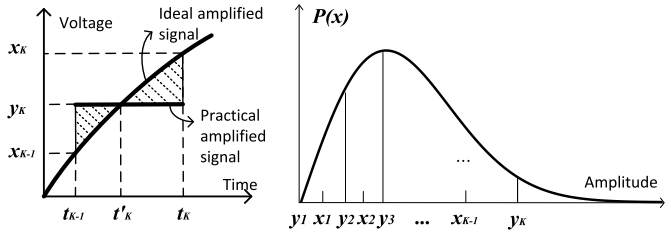


Fig. 2. Left: time varying signal to be quantized. Right: Rayleigh pdf of an OFDM signal. Any signal level between x_{k-1} and x_k, corresponding to the discrete time intervals t_{k-1} to t_k, is mapped to y_k.

a distortion function D is defined, which is expressed as

$$D = \sum_{k=1}^{K} \int_{x_k}^{x_{k+1}} f(x - y_k)\rho(x)dx \tag{1}$$

where the function $f(x - y_k)$ is an error function between the continuous input signal x and the quantized output signal y_k. K is the number of quantization levels, and $\rho(x)$ is the pdf of the input signal.

Suppose that the input data are independently distributed, the probability density of the real and imaginary parts of an OFDM signal with a large number of subcarriers N ($N \geq 256$) approaches a Gaussian distribution [27]. Because of the nonlinear envelope operation, the amplitude of the OFDM signal follows a Rayleigh pdf [28], namely,

$$\rho(x) = 2xe^{-x^2} \tag{2}$$

where x is the OFDM amplitude before quantization. This equation clarifies that the distribution of the OFDM signal only depends on the OFDM amplitude. Once the maximum amplitude is given, the OFDM distribution for any bandwidths (1.4, 5 MHz, etc.) or modulation schemes (4-quadrature amplitude modulation (QAM), 16-QAM, etc.) is immutable.

Next, EVM is defined as the difference between the input and quantized output signals. Thus, the root-mean-square (rms) value of the EVM is calculated as

$$\text{EVM}(\%) = 100 \cdot \sqrt{\frac{\frac{1}{N}\sum_{n=1}^{N}(s'_n - s_n)^2}{P_{\text{ave}}}} \tag{3}$$

where N is the number of symbols over a burst of length over which the value of EVM is calculated. $s_n \in \mathcal{S} = \{s_1, \ldots, s_N\}$ and $s'_n \in \mathcal{S}' = \{s'_1, \ldots, s'_N\}, 1 \leq n \leq N$, are the nth input and output symbol sets, respectively. P_{ave} is the input signal average power, which is recognized as a constant value for a given burst of the input signal.

TABLE I
POWER LEVELS NORMALIZED TO 1-W DPA FOR OPTIMAL LINEARITY

Levels	Input Partition	Output Codebook	Power Levels	Optimal EVM	Uniform EVM
8	**0.16**	0	0.00 W	**5.25%**	6.84%
	0.43	0.31	0.02 W		
	0.67	0.55	0.07 W		
	0.91	0.79	0.15 W		
	1.17	1.04	0.26 W		
	1.46	1.29	0.39 W		
	1.85	1.62	0.62 W		
		2.05	1.00 W		

Based on (3) and the following equation, to minimize the EVM value of the quantized signal, we then define the error function for the nth symbol as:

$$f(s'_n - s_n) = (s'_n - s_n)^2. \tag{4}$$

Replacing the error function and the pdf in (3) with (2) and the following equation, respectively, the new quantization distortion function D can be expressed as:

$$D = \sum_{k=1}^{K} \int_{x_k}^{x_{k+1}} 2(x - y_k)^2 xe^{-x^2} dx. \tag{5}$$

D can be minimized using the following two partial differentials with respect to x_k and y_k given by [25]:

$$\frac{\partial D}{\partial x_k} = |x_k - y_{k-1}| - |x_k - y_k| = 0 \quad \forall k \in \{2, \ldots, K\}$$
$$\frac{\partial D}{\partial y_k} = \int_{x_k}^{x_{k+1}} 2(x - y_k)xe^{-x^2} dx = 0 \quad \forall k \in \{1, \ldots, K\}. \tag{6}$$

The unknown variables x_k and y_k in (6) can be solved numerically in MATLAB to obtain the optimally quantized partition set $\mathcal{X}_{\text{opt}}$ and codebook set $\mathcal{Y}_{\text{opt}}$. The derived codebook set $\mathcal{Y}_{\text{opt}}$ is regarded as the optimal output amplitude levels, which are then transformed to the discrete output power levels. In this way, optimal power levels are elaborately selected to minimize the EVM. If an uniform quantization was selected, the EVM would be 3 dB lower on average [29]. With the presented algorithm, the resulting codebook and input signal partition for an eight-level DPA are reported in Table I.

C. Load Modulation Analysis

To maximize the overall DPA efficiency, the power combiner must be designed suitably to allow efficient, low loss,

combining for every state of the proposed 3-bit DPA. Multiport coupler structures encounter several challenges and trade-offs which urgently require proper solutions.

Unlike the three-way Doherty, the proposed 3-bit DPA has eight different power levels. With a nonisolated combiner, it is impossible to completely isolate the PAs for every possible state, and some RF power might leak to other PA output(s). This issue can be mitigated using the following design approach.

The RF power combiner is a multiport passive device that combines the signal power from multiple input ports to a single output port. Various power combining architectures are available, including Wilkinson combiner [30], rat-race combiner [31], coupled line combiner [32], and RF transformers [33]. Most power combiners in DPAs require the combiner to be isolated so that inactive PAs do not influence the performance of the rest of the active PAs. However, these combiners generally suffer from high insertion loss. A typical 40%–50% of the dissipated power inside these combiners will significantly reduce the efficiency improvement in any DPA architecture [15], [20], [34]. To realize higher back-off efficiency, researchers adopt tunable transmission lines to control the output characteristic impedance $Z_c = Z_{\text{opt}}$ while maintaining a constant phase shift [35]. However, this technique adds complexity and additional losses.

In this work, a fixed microstrip combiner is designed to reach high back-off efficiency while minimizing complexity. This section proposes a method to evaluate the combining power by formulating a theoretical model for a general multiport coupler. As a part of the 3-bit DPA, we focus on a four-port coupler, and its schematic is shown in Fig. 3. This four-port coupler has three input ports, which associate with the constituent PAs' outputs of the 3-bit DPA, and one output port. E_1–E_3 are the source voltages, whereas V_1–V_3 are the reference plane voltage at the input ports. a_1–a_4 denote the incident waves, while b_1–b_4 denote the reflected waves. Z_{s1}–Z_{s3}, Z_L are the normalized impedances to 50 Ω.

By exploiting the impedance variation in the transistor ON and OFF states, the output voltage levels are matched to the values from the quantized power level of Table I. Here, to analyze the output voltage levels, the S-parameter matrix is used to represent a generic passive combining network, which can be described using the following 4×4 scattering matrix [**S**] with 16 independent parameters. If the power splitter is a passive device and only contains isotropic material, the splitter is reciprocal, and its scattering matrix must be symmetric [36]. Thus, the scattering matrix can be further simplified to ten parameters in the following equation:

$$\mathbf{S} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{12} & S_{22} & S_{23} & S_{24} \\ S_{13} & S_{23} & S_{33} & S_{34} \\ S_{14} & S_{24} & S_{34} & S_{44} \end{bmatrix} \tag{7}$$

where S_{ij} refers to the voltage ratio of the signal that reflects from port j to port i. The power combiner and the connected components are illustrated in Fig. 3. The power combiner is a linear network so that the voltage at the output V_{out} can be

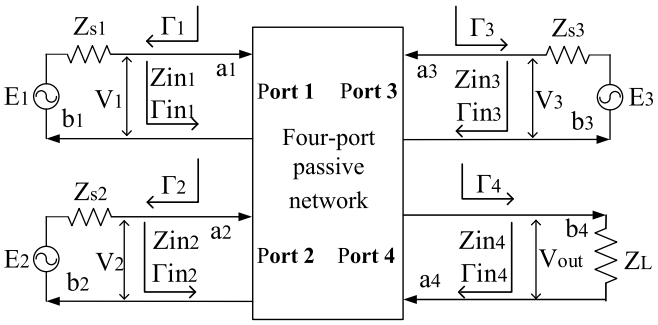


Fig. 3. Four-port passive network schematic with three input ports and one output port.

assessed using superposition, i.e.,

$$V_{\text{out}} = a_4 + b_4 \tag{8}$$

$$a_4 = b_4\Gamma_4. \tag{9}$$

The output power from port 4 is equal to the difference between the incident and reflected power given by

$$P_{\text{out}} = \frac{1}{2}(|b_4|^2 - |a_4|^2) = \frac{1}{2}|b_4|^2(1 - |\Gamma_4|^2). \tag{10}$$

The output amplitude of port 4 is equal to the transmitted amplitudes from three input ports according to

$$b_4 = a_1T_{14} + a_2T_{24} + a_3T_{34} + a_4\Gamma_{\text{in4}} \tag{11}$$

and after substituting (9), it results in

$$b_4 = \frac{a_1T_{14} + a_2T_{24} + a_3T_{34}}{1 - \Gamma_4\Gamma_{\text{in4}}}. \tag{12}$$

Then, the three input voltages are computed by

$$V_1 = a_1 + b_1 = \frac{Z_{\text{in1}}}{Z_{s1} + Z_{\text{in1}}}E_1 \tag{13}$$

$$b_1 = a_1\Gamma_{\text{in1}} \tag{14}$$

$$\Gamma_{\text{in1}} = \frac{Z_{\text{in1}} - 1}{Z_{s1} + Z_{\text{in1}}}. \tag{15}$$

Thus,

$$a_1 = \frac{1 - \Gamma_1}{2(1 - \Gamma_1\Gamma_{\text{in1}})}E_1. \tag{16}$$

Similarly

$$a_2 = \frac{1 - \Gamma_2}{2(1 - \Gamma_2\Gamma_{\text{in2}})}E_2 \tag{17}$$

$$a_3 = \frac{1 - \Gamma_3}{2(1 - \Gamma_3\Gamma_{\text{in3}})}E_3. \tag{18}$$

Therefore,

$$\begin{aligned} V_{\text{out}} &= a_4 + b_4 \\ &= \left\{\frac{1 - \Gamma_1}{2(1 - \Gamma_1\Gamma_{\text{in1}})}E_1T_{14} + \frac{1 - \Gamma_2}{2(1 - \Gamma_2\Gamma_{\text{in2}})}E_2T_{24} \right. \\ &\quad \left. + \frac{1 - \Gamma_3}{2(1 - \Gamma_3\Gamma_{\text{in3}})}E_3T_{34}\right\}\left\{\frac{1 + \Gamma_4}{1 - \Gamma_4\Gamma_{\text{in4}}}\right\}. \end{aligned} \tag{19}$$

In (19), we can observe that the output voltage depends on the transmission coefficients, the reflection coefficients, and the three input voltages. The transmission coefficients and the

reflection coefficients are related to the S-parameter response of the power combiner and the impedance connected to the power combiner. Thus, the performance of the proposed 3-bit DPA depends highly on the combination at the output.

To derive the equations of the output port voltage for the four-port power combiner, the Mason signal flow graph theory is applied to compute transmission coefficients T_{14}, T_{24}, and T_{34} [37]. The derivation of these coefficients based on the Mason signal flow graph theory is presented in Appendix.

Based on the theoretical analysis, we conclude that the performance of the 3-bit DPA depends on the S-parameter response of the power combiner. Multiple solutions can be found in the equations listed in Table VI, which means that the power combiner has enough degree of freedom to realize these output power states theoretically. However, another design target is system efficiency, which highly depends on the characteristic of the transistors. The hybrid quasi-Newton search algorithm optimizer in Keysight ADS software was used to design the power combiner. Section III explains the output power levels and the system efficiency optimization targets in detail.

III. Implementation

Generally, PA designers are provided with the signal that needs to be amplified. Based on the modulated OFDM signal distribution, the OFDM signal is modulated to the control bias voltages. The time-domain OFDM signal is quantized to eight different power levels in this work. The overall design process for switching mode DPA is summarized in the following steps.

1) Analyze the target OFDM signal distribution and select the output power levels to minimize EVM.
2) Choose proper transistors and analyze the upper bound system efficiency.
3) Design the constituent PAs and find the input power to maximize the efficiency for each PA.
4) Design of the input power splitter.
5) Design the output power combiner based on the joint optimization goal with the optimizer.

The output power levels are elaborately selected to optimize the linearity. To attain the best possible system efficiency, specific output impedances are maintained at the output of the constituent PAs through particular design of the optimal output power combiner. Off-the-shelf transistors are then chosen based on the output power levels. The design and optimization processes have been introduced in detail in Sections III-A–III-F.

A. Selection of the Target Output Power Levels

The target output power levels are listed in Table II. They are the nonlinear transformations following the optimal levels in the output codebook. This 3-bit DPA works for 1.5-GHz carrier frequency, and the target peak output power is 35 W. Based on the EVM minimization algorithm in Section II-B, we can derive the results of the optimal output codebook of the OFDM signal for a 3-bit DPA, listed in Table II. Given the maximum target output power $P_{\text{out}}[7] = 35$ W at state 7, the output power target for the rest of the states is proportional to $P_{\text{out}}[7]$ as

$$P_{\text{out}}[i] = \frac{\mathcal{Y}_{\text{opt}}^2[i]}{\mathcal{Y}_{\text{opt}}^2[7]} \times P_{\text{out}}[7] \tag{20}$$

where $\mathcal{Y}_{\text{opt}}(i)$ is the optimal output codebook for the ith state. $P_{\text{out}}(i)$ is the output power of the ith state in Watts, which can be transferred to the decibel value as

$$P_{\text{out}}(\text{dBm}) = 10 \log_{10} P_{\text{out}} + 30. \tag{21}$$

In this way, we select the output power levels to maximize the linearity of the 3-bit DPA. To generate the target $P_{\text{out}}(\text{dBm})$, constituent PAs contribute differently at different states. If only one PA is active, the target $P_{\text{out}}(\text{dBm})$ is equal to the output power of the active PA. If multiple PAs are active, the output power from a single PA is proportional to its maximum output power. Their output power contributions $P_1[i]$–$P_3[i]$ for the ith state can be derived from the following equations:

$$\frac{P_1[i]}{P_1[7]} = \frac{P_2[i]}{P_2[7]} = \frac{P_3[i]}{P_3[7]} \tag{22}$$

$$P_{\text{out}}[i] = P_1[i] + P_2[i] + P_3[i], \quad i \in \{1, 2, \ldots, 7\}. \tag{23}$$

The target $P_{\text{out}}(\text{dBm})$ and the constituent PA power contribution P_1–P_3 at each state are listed in Table II.

TABLE II
Target Output Power-Level Selection

State	Output Codebook $\mathcal{Y}_{opt}$	Target P_{out}(dBm)	P_1 (dBm)	P_2 (dBm)	P_3 (dBm)
0	0	0	OFF	OFF	OFF
1	0.31	29.0	29.0	OFF	OFF
2	0.55	34.0	OFF	34.0	OFF
3	0.79	37.2	31.7	35.7	OFF
4	1.04	39.5	OFF	OFF	39.5
5	1.29	41.4	34.3	OFF	40.5
6	1.62	43.4	OFF	39.1	41.4
7	2.05	45.4	36.6	40.6	42.7

B. Upper Bound System Efficiency Analysis

GaN high-electron mobility transistors (HEMTs) are chosen in this work due to their high breakdown strength, fast switching speed, and high efficiency in compression [38]. To generate eight different power levels with high efficiency, three different Wolfspeed general-purpose GaN transistors are chosen, which are CGH40006P, CGH27015F, and CGH40025F, respectively. As aforementioned, the design target of this 3-bit DPA is 35-W maximum output power at 1.5 GHz. Fig. 4 shows the simulated load—pull trajectories of three GaN transistors at 1.5 GHz. The intersecting (cross) points of the output power contours at each output state and the maximum PAE contours are chosen as the optimal output impedances of each transistor at every state. This is highlighted in Fig. 4. Furthermore, the optimal dynamic impedances at different states are maintained through the design of the output combiner, analyzed in detail previously in Section II-C.

The selection of the optimal output impedances of each transistor at every state allows us to estimate a theoretical upper bound of the achievable DPA system efficiencies at

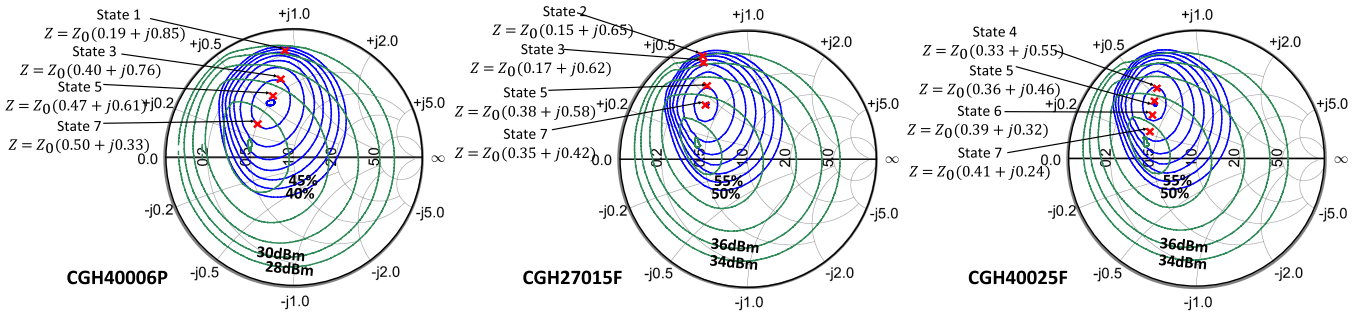


Fig. 4. Optimum load—pull trajectories of efficiency and output power contours. The cross points of different output states and maximum PAE contours are chosen as the optimal impedance.

TABLE III
COMPARISON OF THEORETICAL UPPER BOUND EFFICIENCIES FOR DIFFERENT STATES

State	0	1	2	3	4	5	6	7
$\varepsilon_1[i]$	N/A	49%	N/A	69%	N/A	73%	N/A	70%
$\varepsilon_2[i]$	N/A	N/A	60%	67%	N/A	N/A	74%	77%
$\varepsilon_3[i]$	N/A	N/A	N/A	N/A	81%	83%	81%	78%
$\Pr[i]$	0.04	0.15	0.19	0.19	0.18	0.14	0.08	0.03
$\varepsilon[i]$	100%	49%	60%	68%	81%	80%	78%	77%

each state. The average efficiency $\varepsilon[i](i \in \{0, \ldots, 7\})$ is of all three PAs in the ith state. The results of $\varepsilon[i]$ shown in Table III are derived from

$$\varepsilon[i] = \frac{P_1\varepsilon_1[i] + P_2\varepsilon_2[i] + P_3\varepsilon_3[i]}{P_1 + P_2 + P_3}. \tag{24}$$

In Table III, $\Pr[i](i \in \{0, \ldots, 7\})$ is the cumulative distribution of the OFDM signal in the ith state, which can be given by

$$\Pr[i] = \int_{x_{i-1}}^{x_i} \rho(x)dx. \tag{25}$$

Ignoring the loss from the power splitter and power combiner, the optimal system efficiency to amplify the OFDM signal ε with the selected three transistors is 77.1%, which is derived from

$$\varepsilon = \sum_{i=0}^{7} \varepsilon[i] \times \Pr[i]. \tag{26}$$

C. Design of the Constituent PAs

After choosing the transistors, three different PAs are designed separately at 1.5 GHz. To maximize the system efficiency, transistors are biased around the class-C operating point. Three PAs are designed with the same template, shown in Fig. 5. Each PA is composed of its respective input–output matching networks, stability, and bias networks.

The performance of the three constituent PAs from EM simulations is compared in Fig. 6. The maximum output power results for each PA are $P_{1\max} = 38.5$ dBm, $P_{2\max} = 41.1$ dBm, and $P_{3\max} = 43.9$ dBm, which are higher than the target output power contributions $P_1[i]$–$P_3[i]$ in Table II, respectively.

In this work, the input RF signal is constant, and the constituent PAs are always working at their peak efficiency or

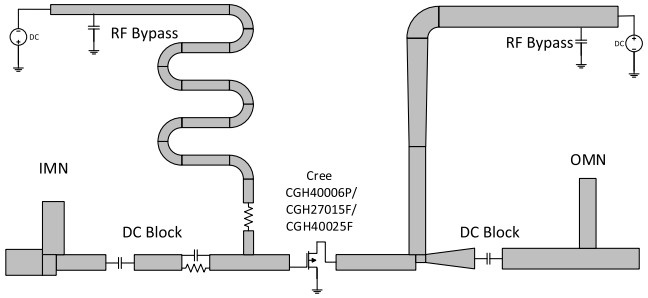


Fig. 5. Schematic of the designed PAs with input–output match network (IMN/OMN), bias, and stability networks.

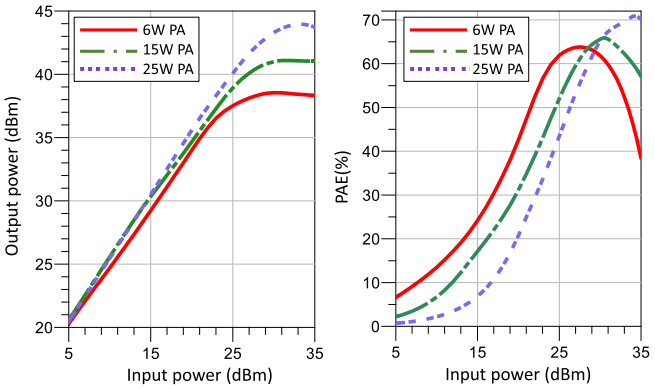


Fig. 6. Performance comparison of the constituent PAs from EM simulations showing input power versus output power (left) and input power versus PAE (right).

completely switching off. The maximum PAE values for the three PAs are 63.8%, 65.9%, and 70.9%, respectively. Those PAE values reach the peak when the input powers are 27, 30, and 30 dBm. Therefore, a proper input power splitter with a splitting ratio of 1:2:2 is required, and the input of the power splitter input power is always 34 dBm.

D. Design of the Input Power Splitter

The input RF signal is divided into three branches. To design an all-port matching and well isolation power divider, Wilkinson [30] proposed a lossy coupler by adding a resistor between two output ports. The resistor is used to dissipate the reflected power so that the output ports can also be matched.

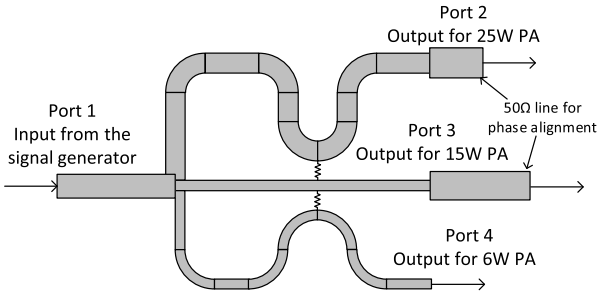


Fig. 7. Schematic of the designed Wilkinson power splitter.

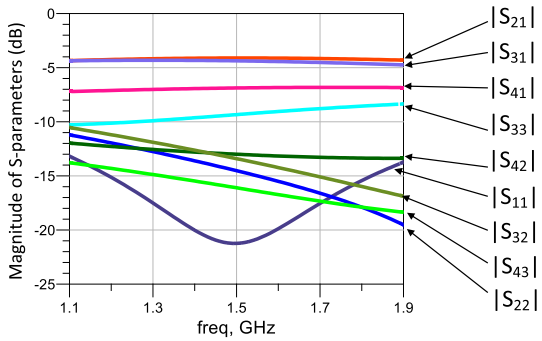


Fig. 8. Simulated performance of the designed Wilkinson power splitter.

In a more general circumstance, the Wilkinson power divider can be expanded to a multiport divider, where all the ports can be matched simultaneously, with isolation between any two ports [30]. However, one disadvantage of the N-way Wilkinson is its crossovers for multiple resistors. This structure is difficult to fabricate in planar form. A practical three-way Wilkinson planar divider is often used by ignoring one isolated resistor between two output ports. It is imperfectly matched, but the layout and fabrication are much more accessible. The splitter in this 3-bit DPA system is designed with only two resistors. The schematic structure is illustrated in Fig. 7. Since the input power of the 6-, 15-, and 25-W PAs are 27, 30, and 30 dBm, respectively, this three-way splitter is designed for a power splitter ratio of 1:2:2. Transmission lines are connected to the output of the power splitter to align the phases of the signals into the constituent PAs to achieve the optimal power combining. The simulated efficiency of the power splitter is 95.8%.

Fig. 8 reports the S-parameter simulation results of the designed power splitter. The magnitudes of the transmission coefficients S_{21}, S_{31}, and S_{41} show that the splitting ratio characteristic is as desired at 1.5 GHz. The remaining coefficients prove that the power splitter has low reflection and high isolation properties.

E. Design of the Optimal Output Power Combiner

A systematic design optimization approach must be adopted to maintain the overall DPA system efficiency for the output power combiner. Moreover, such an optimization approach also helps in the linearity performance of the 3-bit DPA since the output power combiner preserves the optimal impedances selected through load modulation analysis.

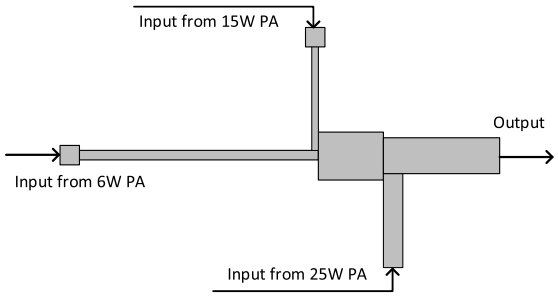


Fig. 9. Schematic of the power combiner after design optimization.

A mean squared error (mse) metric is adopted to minimize the difference between the simulated output power levels and the target output power levels P_{out} which are listed in Table II. Since P_{out} was elaborately selected to maximize the linearity of the 3-bit DPA, minimizing the mse as the strategy for the design optimization of the output power combiner also assists in enhancing the linearity of the DPA. It can be expressed as

$$\text{mse} = \sum_{i=0}^{7} (P_s[i] - P_{\text{out}}[i])^2 \cdot \Pr[i], \quad i = \{1, 2, \ldots, 7\} \tag{27}$$

where $P_s[i]$ is the simulated output voltage and $P_{\text{out}}[i]$ is the target output power for the ith state. $\Pr[i]$ is the cumulative distribution of the OFDM signal in the ith state, as shown in (25). The system drain efficiency ϵ can now be formulated as the ratio of the output power $P_{\text{out}}[i]$ and the input dc power $P_{\text{dc}}[i]$ for the ith state as

$$\epsilon = \sum_{i=0}^{7} \frac{P_{\text{out}}[i]}{P_{\text{dc}}[i]} \cdot \Pr[i], \quad i \in \{1, 2, \ldots, 7\}. \tag{28}$$

Next, we further formulate an optimization goal to realize the structure of the output power combiner by minimizing the mse and maximizing the drain efficiency ϵ jointly. Denoting the structure of the output power combiner by the set of optimized geometric dimensions $\hat{\mathcal{T}}$, the joint optimization goal is expressed as

$$\hat{\mathcal{T}} = \arg\min_{\mathcal{T}} \{\alpha_1 \cdot \text{mse}(\mathcal{T}) - \alpha_2 \cdot \epsilon(\mathcal{T})\} \tag{29}$$

where α_1, α_2 are the weights assigned for minimizing the mse (and hence enhancing the DPA linearity) and maximizing system efficiency, respectively. $\mathcal{T}$ is the initial set of assigned dimensions. The hybrid quasi-Newton search algorithm optimizer in Keysight ADS is used to optimize the joint optimization goal.

To assess the feasibility of our design optimization approach, we benchmark it with an ideal equation-based S-parameter model. With such a model connected to the outputs of three constituent PAs, the system efficiency ϵ achieved is 70.7%, while maintaining a low mse $= 0.85$. These results are close to the theoretical upper bound of the efficiencies derived from (26). It confirms that at least in theory, a power combiner can enable high efficiencies in each of the transistors while maintaining the high linearity in the DPA (attained through optimal selection of the output power levels at each state) with an OFDM waveform. Finally, based on the template and the optimization limitation, the best structure we found is illustrated in Fig. 9.

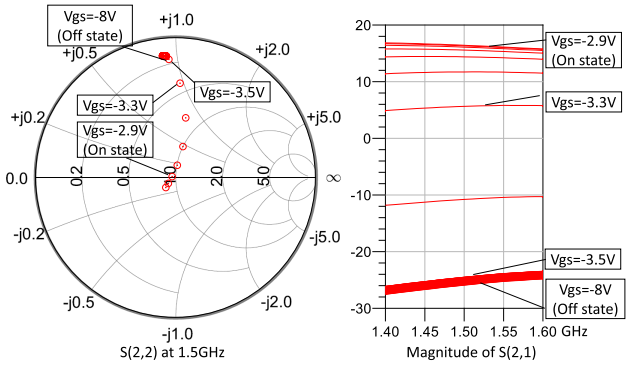


Fig. 10. Simulated output impedance and transmission coefficient S_{21} variation by sweeping the gate bias voltage of a single 15-W PA.

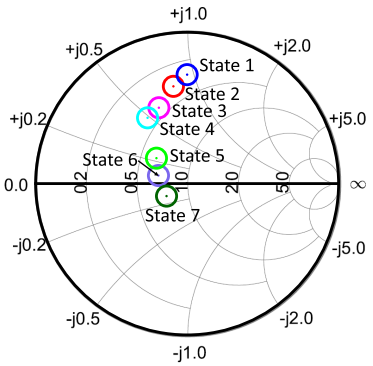


Fig. 11. Simulated impedance transformation trajectories at the output of the power combiner on the Smith chart at different states.

Fig. 10 shows the output impedance and the transmission coefficient S_{21} variation by sweeping the gate bias voltage of a single 15-W PA. The single PA output impedance variation influences the load impedance of other PAs and the impedance at the output power combiner. The Smith chart in Fig. 11 shows the simulated impedance transformation trajectories at different output power level states of the designed 3-bit DPA looking into the output port (port 4) at the power combiner. The output power combiner's impedance at different states is not constant, which causes a mismatching problem when connected to a terminate with constant impedance. However, the load modulation realizes the target output power levels and maximizes the system efficiency. This phenomenon also demonstrates that the integrity of the intended load modulation process is preserved through the designed coupler.

F. Simulations With Modulated OFDM Waveforms

To fully validate the preintegration performance of our 3-bit DPA system, an augmented simulation procedure is adopted by combining simulations in MATLAB and Keysight ADS. The input data are first modulated with QAM/OFDM and then quantized in MATLAB. The quantized data from MATLAB are imported into Keysight ADS, where the designed 3-bit DPA system is simulated. The output voltage data from ADS are further processed in MATLAB and normalized to the same average power level as the input waveform. Finally, the waveform can be demodulated to obtain the original data. The PA output power, average efficiency, EVM, and bit error rate can be computed.

TABLE IV
1.4-MHz OFDM Simulation Result Comparison

Modulation	Peak power	Aver. power	PAPR	EVM RMS	Aver. DE	Aver. PAE
4-QAM	35.6 W	9.4 W	5.8 dB	10.3%	51.3%	42.0%
16-QAM	35.7 W	9.5 W	5.7 dB	10.6%	50.9%	41.8%
64-QAM	35.5 W	9.3 W	5.8 dB	10.8%	51.5%	43.0%

Initially, an input 1.4 MHz OFDM waveform is applied, and the simulation results are listed in Table IV. For 4-QAM. 16-QAM, and 64-QAM, DPA reaches high efficiency to amplify the OFDM waveform without losing much linearity. Specifically, for a 16-QAM-modulated OFDM signal, the 3-bit DPA system average drain efficiency is 50.9%, and the EVM is 10.6%.

Then, 3- and 5-MHz OFDM waveforms are also simulated. The result shows that the 3-bit DPA drain efficiency is more than 55%, upholding the high system efficiency attained with the 1.4-MHz OFDM waveform. However, as shown in the constellation diagrams in Fig. 12, the EVM attained with the 3-MHz OFDM waveform is 11.2%, and with that of the 5-MHz OFDM waveform is 13.0%.

The result shows that the DPA can be used to amplify any bandwidth (1.4, 5 MHz, etc.) or modulation schemes (4-QAM, 16-QAM, etc.) OFDM signal with optimal quantization linearity. Higher resolution can be achieved with more quantization levels. However, with the increase in the switching speed, DPA linearity starts to degrade due to the transconductance and the nonlinear effects induced by the input capacitance [16]. Moreover, the fast-switching bias control signal is filtered by the parasitics in the PA gate bias. The shaped control signal causes EVM deterioration. Further work could be explored to increase linearity by enhancing the switching speed or by adding digital predistortion compensation to shape the control signal. The simulation with modulated OFDM waveforms proves the validity of 3-bit DPA to improve the system efficiency.

IV. Experimental Results

To demonstrate the feasibility of the proposed approach, a 3-bit DPA prototype is fabricated on an Isola substrate of 0.762-mm thickness with a dielectric constant of 2.8. A photograph of the prototype 3-bit DPA is shown in Fig. 13. The power splitter is at the top left in the photograph, which connects to the input of three PAs. The three constituent PAs are located at the top, right, and left of the photograph, and their outputs are attached to the power combiner.

To assess the performance of the 3-bit DPA, the test bed: 1) generates the input RF signal at 1.5 GHz; 2) measures the output signals; and 3) controls the ON–OFF states with the power supplies. The input RF signal is generated by a Keysight E8267D PSG vector signal generator and amplified by a Milmega AS0820-100R driving amplifier. The output power and the spectral characteristics are measured with a Rohde & Schwarz NRP-Z23 power meter. Two AIM-TTI MX100TP power supplies generate the gate bias that can be statically modulated based on the bit configuration. The same supplies also provide the drain voltage supply to the DPA. The schematic of the 3-bit DPA test bed setup is shown in Fig. 16.

OFDM Frame Configuration			
Bandwidth	1.4 MHz	3 MHz	5 MHz
Frame Duration	10 ms		
FTT Size	128	256	512
Resource Blocks	6	15	25
Data Subcarriers	72	180	300

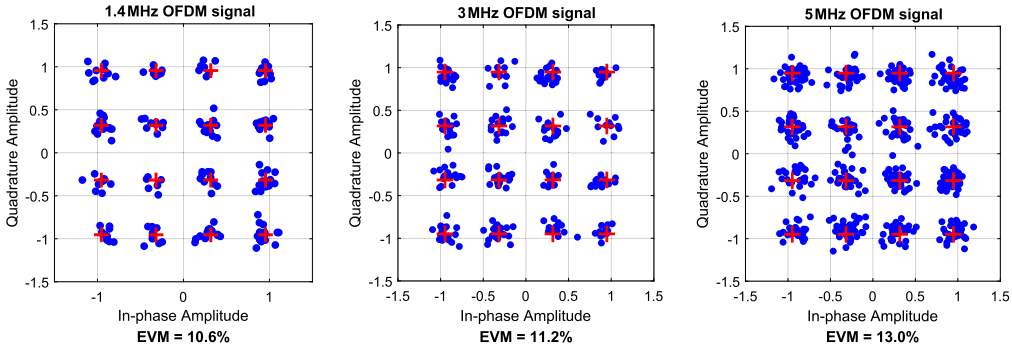


Fig. 12. OFDM frame configuration and constellation diagrams of the demodulated 16-QAM modulation OFDM waveforms with different bandwidths.

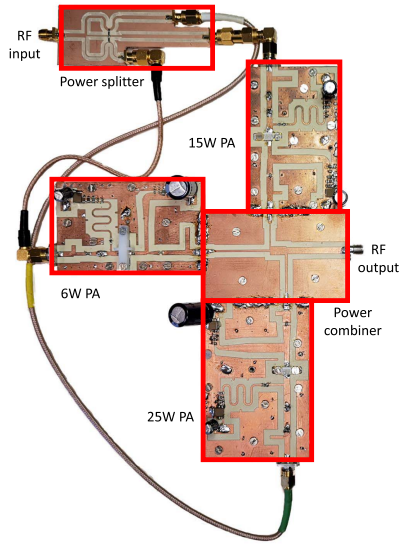


Fig. 13. Photograph of the fabricated 3-bit DPA.

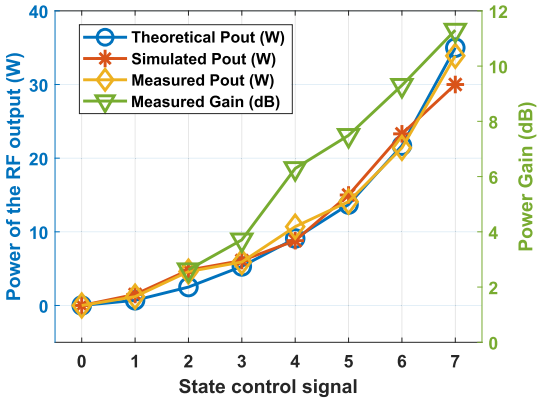


Fig. 14. Measurement of the DPA output power with the CW RF carrier.

A. CW Measurements

With a constant input of 34 dBm or 2.5 W, the power is split into the three constituent PAs based on the splitting ratio of the divider. When the three constituent PAs are turned on and off using −2.7 and −10 V, respectively, the 3-bit DPA provides an output power range from 33 to 45.2 dBm, in the eight distinct amplification states. These results are shown in Fig. 14 and are also in good agreement with the theory and simulations. The most significant difference is in the second state, where the measured output is 4.6 W instead of the theoretical value of 2.5 W. The measured gain is also shown in Fig. 14. This gain is reduced when the output power drops when the input RF signal has a constant power of 34 dBm.

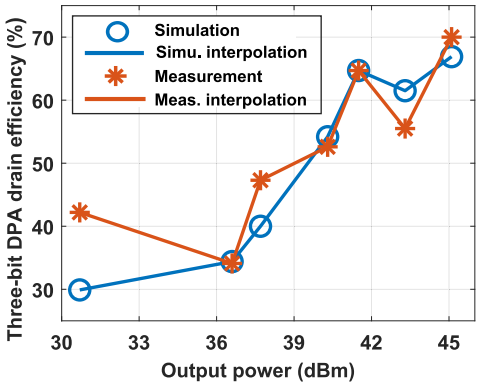


Fig. 15. Measured DPA system drain efficiencies.

Fig. 15 shows the drain efficiency as a function of different power states. The 3-bit DPA achieves a maximum drain efficiency of 70% at 33.9 W output power, which equals to 64.3% power-added efficiency (PAE). At 7.5-dB back-off, the drain efficiency is still 47.3%, thanks to this innovative architecture. In Fig. 15, the measured drain efficiency outperforms the simulation results at lower power levels. This is because the OFF-state PAs are fully switched off in the simulation. In contrast, the OFF-state PAs generate a low output power in the measurements, which is a significant part of the total output power in state 1. The same consideration applies to the PAE. It can be overcome possibly using an RF switch on the input side or an amplitude modulator.

B. Measurements With Digital Control and CW Input Carrier

In this section, the DPA is evaluated with an input CW carrier and amplitude modulation introduced by turning on and off the various constituent PAs. The test bed used for this is shown in Fig. 16. Because of the slow response of the power supplies, the switching between the states cannot be performed at MHz frequencies as in a typical OFDM waveform. Here, an OFDM signal is quantized according to the aforementioned strategy and used to control the power supplies of the bench. A MATLAB script controls the supplies and these are turning on and off the constituent PAs to achieve the required OFDM output power. The whole process consists of the following steps.

1) The input data (information) are modulated, for example, with a 16-QAM and OFDM symbols divided into 1024 subcarriers in MATLAB.

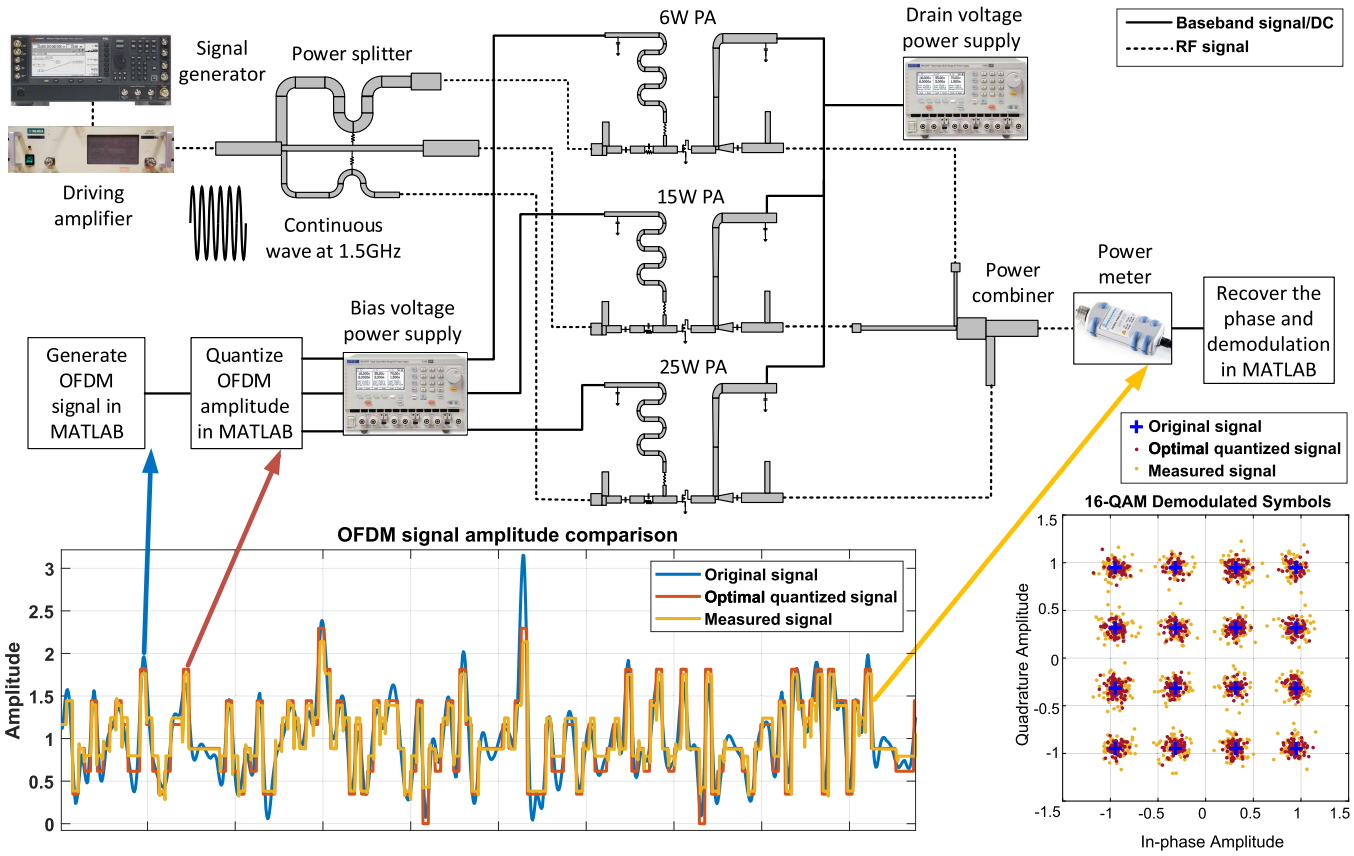


Fig. 16. Schematic to test the DPA performance under simultaneous application of the quantized OFDM waveform to bias the PAs and CW RF carrier driving them. At the DPA output, the measured waveform in the time domain having a nonconstant envelope power is in close agreement with the simulated waveform. The measured EVM from the output waveform indicates the successful transmission of the modulated (information-bearing) symbols from the gate bias to the DPA output.

TABLE V
MEASURED PERFORMANCE SUMMARY AND COMPARISON WITH THE CURRENT STATE-OF-THE-ART SWITCHING MODE PAS

Ref. (Year)	Architecture	Peak output power (dBm)	Peak drain efficiency (%)	Operating frequency (GHz)	Drain efficiency (%) improvement@PBO	Technology
TMTT 2018 [39]	Continuous-mode Doherty	45.2	75.3	1.6-2.7	63.5@6 dB	GaN
RFIC 2018 [40]	Multi-level Outphasing	29.7	34.7*	1.7	27@ 3dB*, 21@6 dB*	CMOS
TMTT 2019 [41]	Three-stage Doherty	46	66	1.6-2.6	63@6 dB, 53@9 dB	GaN
TMTT 2020 [42]	Doherty load modulation	43	72	1.5-2.7	61@6 dB, 58@10 dB	GaN
TMTT 2021 [43]	Sequential load modulation	45.8	69	1.80-2.75	69@8 dB	GaN
TMTT 2018 [44]	Dual-power-mode reconfigurable balun	27.3	40.7$^{\Psi}$	2.0	34.2@5.4 dB	CMOS
JSSC 2002 [20]	Switched-transmission -line-based polar	24.8	49$^{\Psi}$	1.4	43@2.6 dB$^{\Psi}$	CMOS
TMTT 2007 [45]	Switched-transmission -line-based polar	32	40$^{\Psi}$	1.9	17@16 dB*$^{\Psi}$	CMOS
RFIC 2014 [46]	Switched-transformer -based polar	27.3	32.5	3.10-3.98	23.5@5.4 dB*$^{\Psi}$	CMOS
IJMWT 2019 [19]	Switched-transmission -line-based polar	28.9	49	0.5	51@6.4 dB	GaAs
JSSC 2020 [15]	Switched-transmission -line-based polar	21.4	31.3$^{\Psi}$	1.5	27.7@6 dB,16.6@12 dB	CMOS
This work	**Switched-transmission -line-based polar**	**45.2**	**70**	**1.5**	**64.7@3.7 dB, 47.3@7.5 dB**	**GaN**

* Graphically estimated, $^{\Psi}$ Peak added efficiency (PAE).

2) The generated OFDM waveform amplitude is quantized with the optimal quantization strategy to generate three separate control signals based on the ON–OFF relationship among three PAs listed in Table II.

3) These control signals are fed to a voltage supply to switch the constituent PAs ON (−2.7 V) and OFF (−10 V) with a switching speed of about 100 ms.
4) The CW RF carrier at 1.5 GHz is generated by the signal generator and divided by the power splitter.
5) Drain voltage power supply provides constant voltage for each PA, in this case $V_{DS} = 28$ V.
6) The resultant output waveforms' envelope at the output of the DPA is measured.

The measured amplitude is normalized around the average power of the original signal. The result in Fig. 16 shows a good match between the simulated and measured results. The constellation plot also shows a good agreement, despite a small spread around the optimal signal with an EVM of −21.4 dB. The measured signal EVM is −18.2 dB, which is 2.8 dB less than the result from the optimal quantized signal due to imperfect matching to the optimal output power levels in Fig. 14.

C. Performance Comparison

Table V summarizes the performance of the current state-of-the-art switching PAs in literature. Compared with these reported high-performance switching mode PAs fabricated mostly in CMOS or GaAs, our work achieves high peak output power with the GaN transistors while the high back-off efficiency is enhanced between 36.6 and 45.2 dBm. Moreover, the different output power states in our DPA prototype are designed for the linearity improvement of OFDM signal amplification.

V. Conclusion

This article presents a high-performance 3-bit DPA for OFDM amplification. The DPA design process was explained in detail. The output power states are selected based on nonuniform quantization of the OFDM waveform by minimizing the EVM. The selection principles of the distinct output power states of the DPA were based on the load—pull trajectories. The DPA components were analyzed and designed, including three separate PAs and a power combiner. From the simulation results, the system drain efficiency in amplifying the 1.4-MHz 16-QAM OFDM waveform was 50.9%, while the EVM was 10.6%. In the measurements, the system achieved a peak output power of 45.2 dBm with a maximum PAE of 64.3%. At 7.5-dB back-off, the drain efficiency is 47.3%. The systematic simulation and measurement verify that our proposed 3-bit DPA architecture achieves high system efficiency without degrading the linearity during the amplification of the OFDM waveform. Information transmission of digitally modulated OFDM symbols from the DPA bias to the output was demonstrated to prove its switched mode operation. Finally, performance comparison with the current state-of-the-art switching PAs indicates that our proposed 3-bit DPA achieves high state-of-the-art output powers with high efficiency.

Appendix

This section presents the derivation of the output voltage waveform for an arbitrary four-port power combiner. The

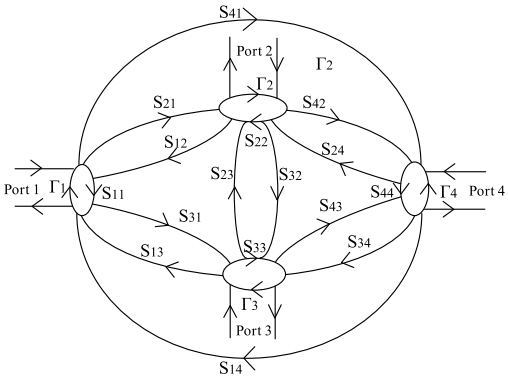


Fig. 17. Signal flow diagram of a four-port power splitter.

Mason signal flow graph theory is implemented to compute transmission coefficients T_{14}, T_{24}, and T_{34} [37]. Mason formula, which provides a general expression for graph gain, is written as

$$G = \frac{\Sigma_k G_k \Delta_K}{\Delta} \tag{30}$$

where

$$\Delta = 1 - \sum_m P_{m1} + \sum_m P_{m2} - \sum_m P_{m3} + \cdots \tag{31}$$

where G_K is the gain of the kth forward path, Δ_k is the value of Δ for that part of the graph not touching the kth forward path, and P_{mr} is the gain product of the mth possible combination of r nontouching loops.

The signal flow graph of a generic four-port splitter is shown in Fig. 17. The transmission coefficients based on the Mason theory are given by

$$\begin{aligned}
T_{14} &= (S_{41}(1 - \Gamma_2 S_{22} - \Gamma_3 S_{33} - \Gamma_2 S_{32}\Gamma_3 S_{23} + \Gamma_2 S_{22}\Gamma_3 S_{33}) \\
&\quad + S_{21}\Gamma_2 S_{42}(1 - \Gamma_3 S_{33}) + S_{31}\Gamma_3 S_{43}(1 - \Gamma_2 S_{22}) \\
&\quad + S_{21}\Gamma_2 S_{32}\Gamma_3 S_{43} + S_{31}\Gamma_3 S_{23}\Gamma_2 S_{42})/\Delta \\
T_{24} &= (S_{42}(1 - \Gamma_1 S_{11} - \Gamma_3 S_{33} - \Gamma_1 S_{31}\Gamma_3 S_{13} + \Gamma_1 S_{11}\Gamma_3 S_{33}) \\
&\quad + S_{12}\Gamma_1 S_{41}(1 - \Gamma_3 S_{33}) + S_{32}\Gamma_3 S_{43}(1 - \Gamma_1 S_{11}) \\
&\quad + S_{12}\Gamma_1 S_{31}\Gamma_3 S_{43} + S_{32}\Gamma_3 S_{13}\Gamma_1 S_{41})/\Delta \\
T_{34} &= (S_{43}(1 - \Gamma_1 S_{11} - \Gamma_2 S_{22} - \Gamma_1 S_{21}\Gamma_2 S_{12} + \Gamma_1 S_{11}\Gamma_2 S_{22}) \\
&\quad + S_{23}\Gamma_2 S_{42}(1 - \Gamma_1 S_{11}) + S_{13}\Gamma_1 S_{41}(1 - \Gamma_2 S_{22}) \\
&\quad + S_{23}\Gamma_2 S_{12}\Gamma_1 S_{41} + S_{13}\Gamma_1 S_{21}\Gamma_2 S_{42})/\Delta
\end{aligned}$$

where

$$\begin{aligned}
\Delta &= 1 - [S_{11}\Gamma_1(1 - S_{22}S_{33}\Gamma_2\Gamma_3) + S_{22}\Gamma_2(1 - S_{22}S_{33}\Gamma_2\Gamma_3) \\
&\quad + S_{33}\Gamma_3(1 - S_{11}S_{44}\Gamma_1\Gamma_4) \\
&\quad + S_{44}\Gamma_4(1 - S_{22}S_{33}\Gamma_2\Gamma_3)] \\
&\quad - [\Gamma_1\Gamma_2(S_{12}^2 - S_{11}S_{22}) + \Gamma_1\Gamma_3(S_{13}^2 - S_{11}S_{33}) \\
&\quad + \Gamma_1\Gamma_4(S_{14}^2 - S_{11}S_{44}) + \Gamma_2\Gamma_3(S_{23}^2 - S_{22}S_{33}) \\
&\quad + \Gamma_2\Gamma_4(S_{24}^2 - S_{22}S_{44}) + \Gamma_3\Gamma_4(S_{34}^2 - S_{33}S_{44})])] \\
&\quad - 2[\Gamma_2\Gamma_3\Gamma_4 S_{23}S_{24}S_{34}(1 - S_{11}\Gamma_1) \\
&\quad + \Gamma_1\Gamma_3\Gamma_4 S_{13}S_{14}S_{34}(1 - S_{22}\Gamma_2) \\
&\quad + \Gamma_1\Gamma_2\Gamma_4 S_{12}S_{14}S_{24}(1 - S_{33}\Gamma_3)
\end{aligned}$$

TABLE VI
OUTPUT VOLTAGE VALUES FOR 3-BIT DPA

State	Output voltage V_{out} (V)
0	0
1	$\frac{1}{2}E_1(S_{41}+\frac{S_{21}S_{42}(1-S_{33})+S_{31}S_{43}(1-S_{22})+S_{21}S_{32}S_{43}+S_{31}S_{23}S_{42}}{1-S_{22}-S_{33}-S_{32}S_{23}+S_{22}S_{33}})$
2	$\frac{1}{2}E_2(S_{42}+\frac{S_{12}S_{41}(1-S_{33})+S_{32}S_{43}(1-S_{11})+S_{12}S_{31}S_{43}+S_{32}S_{13}S_{41}}{1-S_{11}-S_{33}-S_{31}S_{13}+S_{11}S_{33}})$
3	$\frac{E_1(S_{41}-S_{33}S_{41}+S_{31}S_{43})+E_2(S_{42}-S_{33}S_{42}+S_{32}S_{43})}{2(1-S_{33})}$
4	$\frac{1}{2}E_3(S_{43}+\frac{S_{23}S_{42}(1-S_{11})+S_{13}S_{41}(1-S_{22})+S_{23}S_{12}S_{41}+S_{13}S_{21}S_{42}}{1-S_{11}-S_{22}-S_{21}S_{12}+S_{11}S_{22}})$
5	$\frac{E_1(S_{41}-S_{33}S_{41}+S_{31}S_{43})+E_3(S_{43}-S_{22}S_{43}+S_{23}S_{42})}{2(1-S_{22})}$
6	$\frac{E_2(S_{42}-S_{33}S_{42}+S_{32}S_{43})+E_3(S_{43}-S_{22}S_{43}+S_{23}S_{42})}{2(1-S_{11})}$
7	$\frac{1}{2}(E_1S_{41}+E_2S_{42}+E_3S_{43})$

$$+\Gamma_1\Gamma_2\Gamma_3S_{12}S_{13}S_{23}(1-S_{44}\Gamma_4)]$$
$$+S_{11}S_{22}S_{33}S_{44}\Gamma_1\Gamma_2\Gamma_3\Gamma_4.$$

In this work, the input PAs only have two states, ON and OFF. Specifically, assuming that the impedance Z_0 is normalized when PA is ON, whereas impedance is infinity when PA is OFF. The load impedance is constantly equal to Z_0, which means Γ_4 is zero. The output voltage levels can be simplified. The output voltages of eight different states are summarized in Table VI.

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