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On the Effect of SiC Power MOSFET Gate Oxide Degradation in High Frequency Phase Leg-Based Applications

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Abstract—**Silicon Carbide power MOSFET is a promising option for high power high density applications in the next generation of power electronic applications. Investigating the reliability issues and concerns, however, is a pre-requisite for enabling this technology to be widely used. Gate oxide degradation is a major chip-related failure mode in MOSFETs. The problem of gate oxide degradation is even more severe in SiC MOSFETs because of the thin gate-oxide layer. Interface trapped charge at SiC-SiO_2 interface is much higher than Si counterpart. The main effect of gate oxide degradation is changes in Miller plateau and threshold voltage value of the switch. These changes usually lead to having a longer rise time and shorter fall time in the switch. Although extensive research has been carried out on proposing precursors and characterization for SiC MOSFET gate oxide degradation, a circuit-level study is lacking. In this paper, the effect of gate oxide degradation on the operation of a half-bridge converter is studied. It is shown that the deadtime between the high side and low side switches in phase leg structure has been increased. In high frequency applications with short pulsewidth, the main consequence is that the average load voltage will be decreased. To show the effect of gate oxide degradation on phase leg operation, simulation in PSpice and experimental set-up are used. Commercial discrete SiC MOSFET 650V/22A is degraded in gate oxide layer using an adjustable degradation set-up. The brand-new and degraded switches are examined in a phase leg structure with switching frequency of 115kHz. The results showed that a 45% increment in deadtime is detected, which leads to decrement in the average voltage of the load.**

keywords– Dead-time, Degradation, Half bridge, MOSFET, Silicon Carbide (SiC)

I. Introduction

Silicon Carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) present low conduction power loss, high temperature endurability, and high frequency operation capabilities, which are the main specifications for the employed semiconductor switches in high-density power electronic applications [1]–[4]. SiC MOSFET reliability issues have been categorized into two main groups: Package-level (wire bond and solder layer failure modes) and chip-level (gate oxide layer and body diode failure modes) [1]. The focus of this paper is on gate oxide degradation modes.

Tunneling current into the gate oxide layer has been identified as the main reason of gate oxide degradation [5]. Due to thin gate oxide layer in SiC MOSFETs, a Fowler–Nordheim tunneling can inject additional electrons into oxide layer in high electric conditions [6]. Comparing SiC- and Silicon (Si)-MOSFETs, interface trapped charge at SiC-SiO_2 interface is much higher than Si counterpart [7]. As a consequence, the device mobility is decreased by high coulombic scattering and few numbers of free carriers [8]. A total positive charge created by oxide and interface trapped charges result in a negative shift of the threshold voltage (V_{th}) and vice versa. The effect of trapped charges on V_{th} depends on the distance between trapped charges in the oxide and SiC conduction channel [6].

In device-level studies, multiple online and offline precursors are proposed in the literature to detect and measure the gate oxide degradation level in the SiC MOSFETs. Drain leakage current [9], V_{th} [10], gate Miller plateau voltage (V_{GP}) [11], gate leakage current [12], gate Miller plateau time (t_{GP}) [5], switch turn-on delay [13], switch junction capacitance [6], and on-state resistance (R_{DS-on}) [14] have been employed as condition monitoring (CM) precursors in the literature. However, the effect of gate oxide degradation

on circuit-level should be investigated as well. Because as gate oxide degradation changes some deterministic parameters in the switch transient behavior, the turn-on/off behavior of the switch changes considerably. In circuit-level analysis, this transient behavior change of SiC MOSFET may lead to major changes in the operation of the switch in the circuit.

In a phase leg structure, to avoid shoot-through, a deadtime is usually considered in the commutation time interval of the switches. This deadtime is a minor percentage of the duty cycle of the inverter. However, in circuits with high switching frequency levels, the applied pulsewidth to both high side and low side switches is relatively short. In these occasions, the deadtime becomes deterministic in value of the average voltage of the load. In other words, although deadtime is still not a long time interval, it is important in calculating the average load voltage as the pulsewidth is so short. In this condition, any changes in deadtime may change the average load voltage [15].

Gate oxide degradation is SiC MOSFETs majorly changes the turn-on and turn-off transient behavior of the switch both in resistive load and inductive loads. In section II, it will be completely explained that gate oxide degradation increases the Miller plateau voltage, and consequently, the turn-on delay time and Miller plateau time in turn-on transient will be increased. Similarly, as the Miller plateau voltage has been increased, the turn-off delay time will be decreased, and Miller plateau time in turn-off time interval will be decreased too. These changes lead to having a longer rise time with shorter turn-on delay. Also, the switch turn-off behavior is changed to shorter fall time and less turn-off delay time. In circuit-level analysis, these changes can affect the timings in the switching pattern of the converter or inverter. In this paper, we have used half-bridge as a case study. In simulation and experimental results, we have shown that when the switch is transitioning from brand-new condition to fully degraded gate oxide layer condition, the turn-on/off behavior of the both high side and low side switches are changed. In a phase leg structure, it causes to have a longer deadtime in the commutation time interval of the switches. This basically leads to having less average load voltage, as the effective pulsewidth is decreased. This effect is more important and destructive in the high frequency applications with small pulsewidth.

The rest of the paper is organized as follows. In section II, gate oxide degradation process is studied, and the variations in the turn-on and turn-off processes are investigated. In section III, the effect of turn-on/off behavior of a single switch in the operation of a phase leg structure is explained. In section IV, using a developed simulation model in PSPICE, the deadtime dependency on the Miller plateau of the high side and low side switches is studied. Using 650V/22A discrete SiC MOSFET as the case study switch, a laboratory set-up of a half-bridge circuit is implemented in section V. Using a dedicated degradation set-up, different rates of gate oxide degradation is induced in the case study switch, and the deadtime variations are investigated.

II. GATE OXIDE DEGRADATION IN SIC MOSFETS

Due to the limited current path of traditional lateral MOSFETs with thin planar volume of silicon located in parallel to the gate, vertical gate structure designs are more common for power MOSFETs [6]. High electric field stress (HEFS) induces a gradual breakdown in the gate oxide layer which is named time-dependant dielectric breakdown (TDDB) in the literature [1], [16]. TDDB occurs due to defect accumulation within the gate oxide layer. During the gate oxide degradation process, if the defects line up, a short-circuit path is formed in the gate oxide layer, and consequently, the MOSFET loses its gate controllability. In other words, the fundamental reason behind TDDB is the accumulation of defect charges in the oxide layer [17]. In [18], the defect charges are categorised as: 1) fixed charge; 2) mobile ion; 3) interface trapped charge; and 4) oxide trapped charge. Among them, interface trapped charges and oxide trapped charges are mainly responsible for mobility reduction in MOSFET channel and V_{th} variations. As the stress time (t_{stress}) increases, V_{th} changes, and this has a detectable effect on V_{GP} and consequently on the transient behavior of the switch during the turn-on/off processes. V_{GP} can be written as (1) based on V_{th} [19].

$$V_{GP} = V_{th} + \sqrt{\frac{I_D L_{CH}}{\mu C_{ox} Z}} \tag{1}$$

, where I_D is the drain channel current, L_{CH} is the channel length, Z is the channel width, and μ is the channel carrier mobility. Since μ is a decreasing function with respect to t_{stress} [18], V_{GP} is an increasing function of t_{stress}.

Due to thin gate-oxide layer in SiC MOSFETs, a Fowler–Nordheim tunneling can inject additional electrons into oxide layer in high electric conditions. Comparing SiC- and Si-MOSFETs, interface trapped charge at SiCSiO2 interface is much higher than Si counterpart. As a consequence, the device mobility is decreased by high Coulombic scattering and few numbers of free carriers [8]. A total positive charge created by oxide and interface trapped charges result in a negative shift of the threshold voltage and vice versa. The effect of trapped charges on threshold voltage depends on the distance between trapped charges in the oxide and SiC conduction channel [6].

A. Gate Oxide Degradation Effect on Miller Plateau

During the turn-on process, the gate-source capacitance (C_{GS}) must be charged, and the gate-drain capacitance (C_{GD}) must be discharged. The main part of V_{DS} decrement occurs when V_{GS} is constant, and the output current of the driver ($i_G(t)$) discharges C_{GD}. This interval is known as Miller plateau. $i_G(t)$ in the turn-on process is described as (2).

$$i_G(t) = \frac{V_{Dr} - V_{GP}}{R_G} = -C_{GD,avg}\frac{dV_{DS}}{dt} \tag{2}$$

,where V_{Dr} is the applied voltage from the gate driver to the gate-source of the switch, R_G is the sum of the internal and external resistances of the gate, and $C_{GD,avg}$ is the average of the gate-drain capacitance of the switch. Assuming V_{DS} falls

linearly from V_{Bus} to 0V during switch turn-on process, (2) can be re-written as (3).

$$t_{GP-on} = R_G C_{GD,avg} \frac{V_{Bus}}{V_{Dr} - V_{GP}} \tag{3}$$

t_{GP-on} strictly depends on the Miller plateau considering (3). Since V_{GP} increases due to gate oxide degradation (according to (1)), it can be concluded that t_{GP-on} also increases over the degradation process. As a result, $d(V_{DS})/dt$ in turn-on process of the switch is decreased during the gate oxide degradation.

During the turn-off process, V_{DS} of the switch increases from 0V to V_{Bus}. To turn off the switch, the driver provides a zero-level voltage for the gate to discharge C_{GS} and charge C_{GD}. The same as the turn-on process, the major part of the changes in V_{DS} occurs in the Miller plateau. In this time interval, V_{GS} is approximately constant, and the driver current charges C_{DG}. Accordingly, t_{GP-off} is described as (4).

$$t_{GP-off} = R_G C_{GD,avg} \frac{V_{Bus}}{V_{GP}} \tag{4}$$

Regarding (1), V_{GP} increases over the gate oxide degradation, and t_{GP-off} decreases in the degradation process as the result.

B. Gate Oxide Degradation Effect on switch turn-on and turn-off delays

In SiC MOSFET turn-on/off time intervals, there is also a delay time interval. In that time interval, V_{DS} remains unchanged, and V_{GS} is being changed by the gate driver. In the turn-on delay interval, the driver increases V_{GS} from zero to V_{th} [20]. Therefore, the turn-on delay (t_{D-on}) is described as (5).

$$t_{D-on} = -R_G C_{GS} ln(1 - \frac{V_{th}}{V_G}) \tag{5}$$

Similarly, in the turn-off delay interval, the driver current decreases V_{GS} from V_G to V_{GP} [20]. Thus, the turn-off delay (t_{D-off}) is described as (6).

$$t_{D-off} = -R_G C_{GS} ln(\frac{V_{GP}}{V_G}) \tag{6}$$

In the gate oxide degradation process, both V_{GP} and V_{th} values experience an increment. These changes have two effects: 1) based on (5), t_{D-on} is increased; and 2) based on (6), t_{D-off} is decreased. As a result, in the rising edge of V_{DS}, related to the turn-off process of the switch, with a specific pulse width supplied by the gate driver, V_{DS} rise time will become shorter during the degradation. In Fig.1, the effect of gate oxide degradation on turn-off and turn-on transient behavior of the switch is shown for both high side and low side switches in a phase leg structure.

For the circuit with inductive loading effect on the switch, (3), (4), (5), and (6) are correct without any approximation. V_{GP} in turn-on and turn-off transient time intervals is fixed. Because of existence of the free-wheeling diode parallel to the inductive load, I_D is maintained constant when V_{DS} varies. This leads to having a constant value of V_{GP} over the turn-on

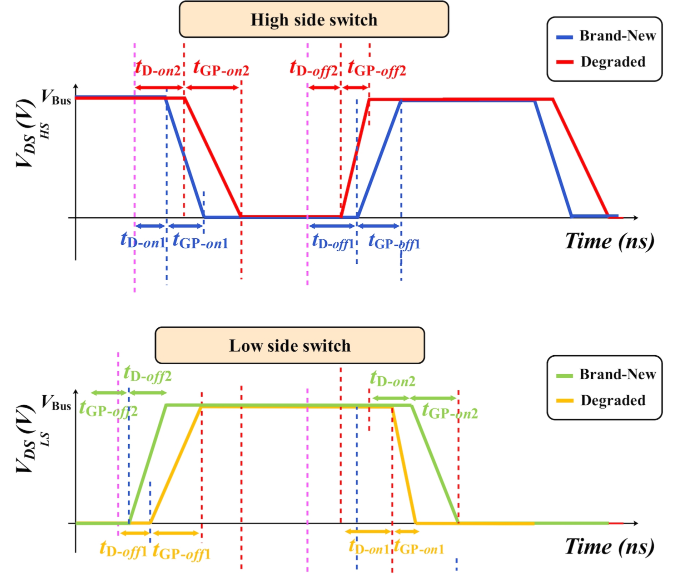


Fig. 1. Turn-on/off changes due to gate oxide degradation in low side and high side switches in a phase leg structure

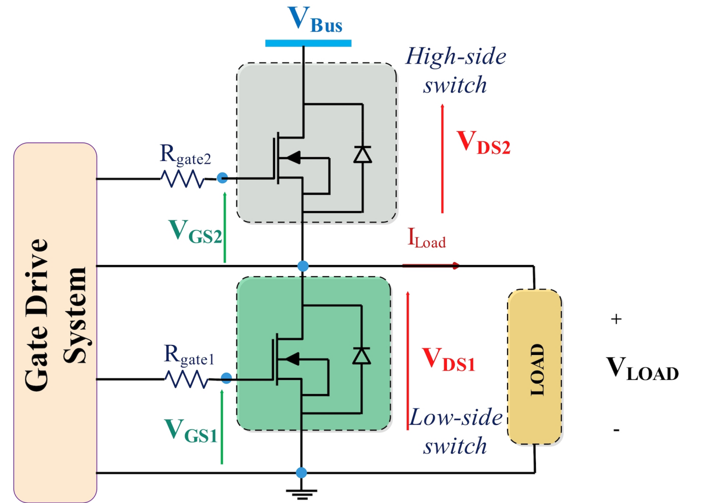


Fig. 2. Low side and high side switches in a phase leg structure

and turn-off transient time intervals. In resistive load, however, as I_D changes gradually with the change of V_{DS}, V_{GP} is not a constant value based on (1). Therefore, some degree of approximation is needed to be considered if we want to use (3), (4), (5), and (6) for power circuits with resistive load.

III. SIC MOSFET TRANSIENT BEHAVIOR EFFECT ON PHASE LEG OPERATION

To perform correct status change of the power switches in a phase leg structure (see Fig.2), the employed PWM generator should insert small amount of time between required switching edges for high side switch. This time is called deadtime. It depends on the type of the switch, supply voltage, and gate driver capabilities.

The deadtime is usually applied as a precaution for avoiding shoot-through of the two switches in the phase leg structure.

The deadtime percentage is usually a small portion of the duty cycle. However, in the applications with high frequcny of operation and small pulsewidth, the deadtime is a considerable value of the whole pulsewidth. Considering this, in high frequency applications, the deadtime can play a major role in determining the RMS value of the load voltage.

As discussed in section II, the gate oxide degradation affects both the turn-on and turn-off behavior of the switch. Rise time of the switch is increased, and fall time is decreased. In a phase leg-based structure with two switches, e.g. low side switch and high side switch, this change in rise time and fall time of the switches will change the deadtime value. In Fig.1, the effect of gate oxide degradation on high side and low side switches in a phase leg structure is shown. It can be seen that by transitioning of the switch from brand-new condition to degraded condition, the deadtime is increased. This is because of the fact that for a specific commutation, the rise time of one switch is increased, and the turn-on delay time is also increased, while for the other switch, the fall time is decreased, and the turn-off delay time is decreased as well. This causes to have a longer deadtime in the commutation time interval.

IV. Simulation Results

To examine the changes in the deadtime, a simulation model of half bridge circuit is simulated using PSpise. The circuit specifications and switch parameters are listed in Table.I. V_{GP} is used to model the gate oxide degradation effect in the simulation model. V_{GP1} is the Miller gate plateau voltage of the switch in brand-new condition, and V_{GP2} is the Miller gate plateau of the switch in degraded condition. The result of the simulation model is shown in Fig.3 to show the effect of gate oxide degradation on V_{GS} waveform.

In the deadtime interval, both the high side and low side switches are turned off, and V_{DS} of high side and low side switches equal V_{Bus}. Because of the existence of a freewheeling diode in the half-bridge circuit as well as the inductive loading effect, V_{LOAD} equals zero. It was explained that due to the gate oxide degradation, the deadtime will be increased. The main result of the deadtime increment is that the zero level voltage in V_{LOAD} has been increased, as shown in Fig.4.

TABLE I
THE OVERALL SPECIFICATIONS AND RATINGS OF THE SIMULATED HALF BRIDGE CIRCUIT

V_{Bus}	200V
C_{Bus}	34 μF
f_s	200 kHz
$R_{G_{ext}}$	10 Ω
V_{GP1}	7 V
V_{GP2}	13 V

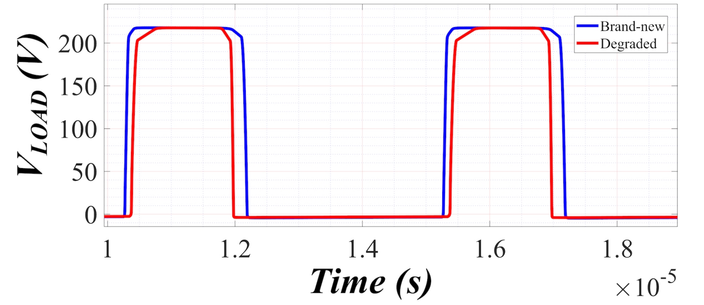


Fig. 4. simulation results of V_{LOAD} changes due to gate oxide degradation

V. Experimental Set-up

To evaluate the changes in deadtime in a phase leg structure, a laboratory set-up of a half-bridge inverter is implemented, as shown in Fig.5. The circuit specifications are listed in Table.II. The case study switch in these tests is C3M0120065D, 650V/22A, manufactured by Cree [21].

To be able to investigate the effect of gate oxide degradation on phase leg operation, we have used a dedicated degradation set-up for stimulating gate oxide degradation with different rates. In the literature, two stressors are introduced for the gate oxide degradation, i.e., HEFS and high temperature stress [1], [5]. In this paper, we have used HEFS method for inducing gate oxide degradation in the SiC MOSFET case study switches. In Fig.6, the employed degradation circuit, based on HEFS mechanism, is shown. Using different values of gate stressor voltage (V_{stress}), the deadtime changes in the phase leg structure can be investigated. The gate oxide

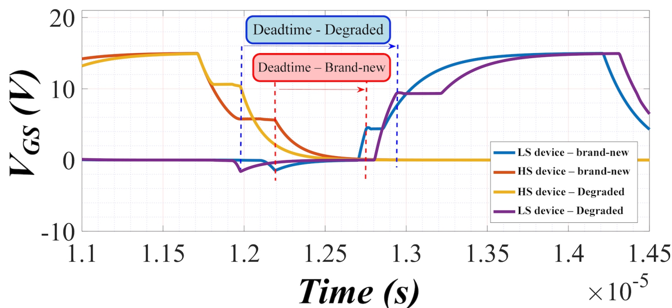


Fig. 3. simulation results of V_{GS} changes due to gate oxide degradation for high side and low side switches in a phase leg structure

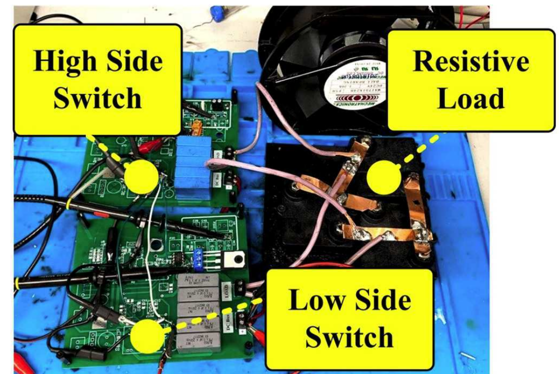


Fig. 5. Experimental set-up of the half bridge circuit

TABLE II
THE OVERALL SPECIFICATIONS AND RATINGS OF THE HALF BRIDGE LABORATORY SET-UP

V_{Bus}	220V
C_{Bus}	45 μF
f_s	115 kHz
$R_{G_{ext}}$	12 Ω
R_{LOAD}	20 Ω

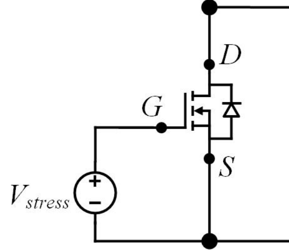


Fig. 6. HEFS circuit for gate oxide degradation

breakdown voltage of the SiC MOSFET case study switch is found as 39 V. In [22], it is shown that for a Si MOSFET with similar gate structure and similar ratings, the breakdown voltage is 65 V which clearly demonstrates the vulnerability of SiC MOSFET gate oxide layer against HEFS. Theoretically, smaller conduction band offset between SiC and SiO_2 leads to higher leakage current and hence, smaller breakdown field value [23].

Based on the gate breakdown voltage of the switch, V_{stress} is chosen as 37V, 37.5V, and 38V for the experimental tests. To bypass the effect of temperature in the process of gate oxide degradation, all the degradation tests are carried out at room temperature level (26°C) while switch case temperature is also 26°C. In Fig.7, the effect of gate oxide degradation on V_{GP} and t_{GP-on} of the switch is shown in V_{stress} = 37V and stress time of 90min. It can be seen that V_{GP} value is changed from V_{GP1}=11.9V to V_{GP2}=13.4V due to gate oxide degradation. Moreover, in the turn-on transient, t_{GP-on} has experienced a value change from 68ns to 114ns.

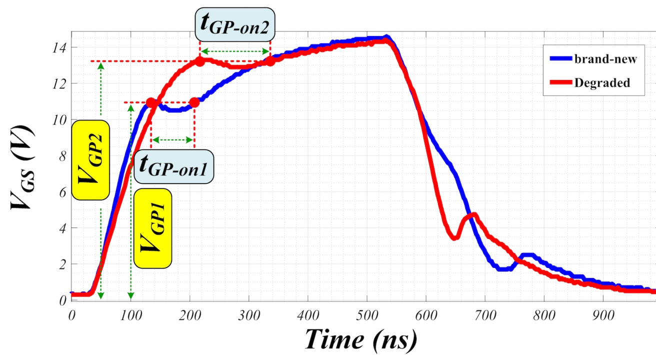
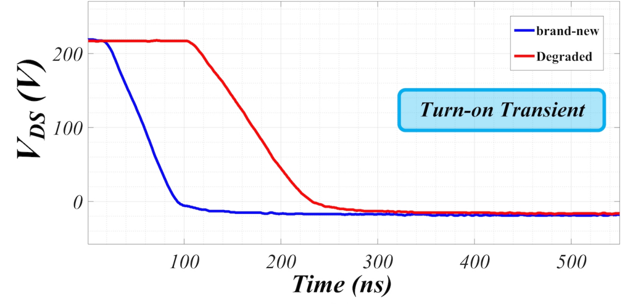


Fig. 7. V_{GP} and t_{GP-on} changes during the gate oxide degradation tests; V_{stress} = 37V and t_{stress} = 90 min



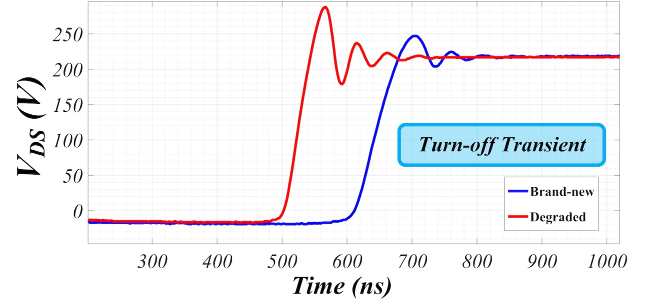


Fig. 8. (a) Turn-on and (b) turn-off transient behavior changes in switch transition from brand-new to gate oxide degraded condition

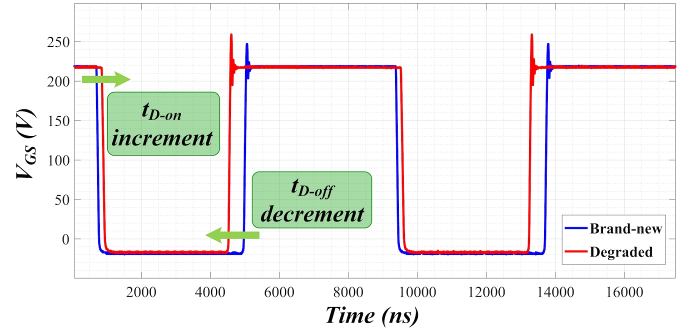


Fig. 9. Load voltage variations in half bridge circuit due to the gate oxide degradation of the high side and low side switches

A. Gate Oxide Degradation Effect on Low side and High Side Switches

Using the above-explained degradation set-up, gate oxide degradation is induced in both the high side and low side SiC switches. V_{stress} = 37.5V and t_{stress} = 75 min are applied to the switches. Fig.8 shows the changes in turn-on and turn-off behavior of the low side switch. It can be seen that, as expected, t_{D-on} and t_{GP-on} have been increased for both the switches. However, t_{D-off} and t_{GP-off} have been decreased for both the switches.

The degraded switches are employed in the phase leg structure. In the first experiment, two brand-new switches are employed, and in the second experiment, the gate oxide

degraded switches are employed in the phase leg structure. In Fig.9, it can be seen that V_{LOAD} experiences more deadtime. because in the commutation time interval, the high side switch has become faster in fall time, while the low side switch has become slower in its rise time interval. These two changes have led to longer deadtime.

VI. Conclusion

Being focused on transient behavior of the Silicon Carbide power MOSFET, the effect of gate oxide degradation on turn-on and turn-off behavior of the switch was investigated. From the circuit-level analysis, the effect of this transient behavior change was studied for a phase leg structure with two SiC switches. In simulation and experimental results of this paper, it was proven that by inducing gate oxide degradation in SiC MOSFETs, the considered deadtime in the phase leg structure is increased. This is because of slower rise time and faster fall time of the switches due to the gate oxide degradation effect. This increment in deadtime in the high frequency applications with short pulsewidth of conduction in the switches can play a major role in the average value of the load voltage.

References

[1] Z. Ni, X. Lyu, O. P. Yadav, B. N. Singh, S. Zheng, and D. Cao, "Overview of real-time lifetime prediction and extension for sic power converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 7765–7794, 2020.

[2] J. Naghibi, K. Mehran, and M. P. Foster, "An online failure assessment approach for sic-based mosfet power modules using iterative condition monitoring technique," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–5, 2020.

[3] A. Griffo, J. Wang, K. Colombage, and T. Kamel, "Real-time measurement of temperature sensitive electrical parameters in sic power mosfets," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2663–2671, 2018.

[4] J. Naghibi, K. Mehran, and M. P. Foster, "High-frequency non-invasive magnetic field-based condition monitoring of sic power mosfet modules," *Energies*, vol. 14, no. 20, p. 6720, 2021.

[5] U. Karki, N. S. Gonzalez-Santini, and F. Z. Peng, "Effect of gate-oxide degradation on electrical parameters of silicon carbide mosfets," *IEEE Transactions on Electron Devices*, vol. 67, no. 6, pp. 2544–2552, 2020.

[6] M. Farhadi, F. Yang, S. Pu, B. T. Vankayalapati, and B. Akin, "Temperature-independent gate-oxide degradation monitoring of sic mosfets based on junction capacitances," *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 8308–8324, 2021.

[7] J. Naghibi and K. Mehran, "Multiphysics condition monitoring technique for reliability assessment of wide bandgap-based power modules in electric vehicle application," in *2020 Fifteenth International Conference on Ecological Vehicles and Renewable Energies (EVER)*, pp. 1–6, 2020.

[8] S. Potbhare, N. Goldsman, G. Pennington, A. Lelis, and J. M. McGarrity, "Numerical and experimental characterization of 4 h-silicon carbide lateral metal-oxide-semiconductor field-effect transistor," *Journal of Applied Physics*, vol. 100, no. 4, p. 044515, 2006.

[9] R. Green, A. Lelis, and D. Habersat, "Application of reliability test standards to sic power mosfets," in *2011 International Reliability Physics Symposium*, pp. EX.2.1–EX.2.9, 2011.

[10] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of sic mosfets," *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 316–323, 2014.

[11] S. Pu, F. Yang, E. Ugur, C. Xu, and B. Akin, "Sic mosfet aging detection based on miller plateau voltage sensing," in *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, pp. 1–6, 2019.

[12] R. Ouaida, M. Berthou, J. León, X. Perpiñà, S. Oge, P. Brosselard, and C. Joubert, "Gate oxide degradation of sic mosfet in switching conditions," *IEEE Electron Device Letters*, vol. 35, no. 12, pp. 1284–1286, 2014.

[13] S. Pu, E. Ugur, F. Yang, and B. Akin, "In situ degradation monitoring of sic mosfet based on switching transient measurement," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 5092–5100, 2019.

[14] Y. Zhang and Y. C. Liang, "A simple approach on junction temperature estimation for sic mosfet dynamic operation within safe operating area," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 5704–5707, 2015.

[15] M. Zarghani, S. Mohsenzade, A. Hadizade, and S. Kaboli, "An extremely low ripple high voltage power supply for pulsed current applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 7991–8001, 2020.

[16] J. Liu, G. Zhang, Q. Chen, L. Qi, Y. Geng, and J. Wang, "In situ condition monitoring of igbts based on the miller plateau duration," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 769–782, 2018.

[17] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois, "Radiation effects in mos oxides," *IEEE Transactions on Nuclear Science*, vol. 55, no. 4, pp. 1833–1853, 2008.

[18] A. J. Lelis, D. Habersat, R. Green, A. Ogunniyi, M. Gurfinkel, J. Suehle, and N. Goldsman, "Time dependence of bias-stress-induced sic mosfet threshold-voltage instability measurements," *IEEE transactions on Electron Devices*, vol. 55, no. 8, pp. 1835–1840, 2008.

[19] J. Liu, G. Zhang, Q. Chen, L. Qi, Y. Geng, and J. Wang, "In situ condition monitoring of igbts based on the miller plateau duration," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 769–782, 2018.

[20] M. A. Rodríguez-Blanco, A. Claudio-Sánchez, D. Theilliol, L. G. Vela-Valdés, P. Sibaja-Terán, L. Hernández-González, and J. Aguayo-Alquicira, "A failure-detection strategy for igbt based on gate-voltage behavior applied to a motor drive system," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 5, pp. 1625–1633, 2011.

[21] Cree-Wolfspeed, *650V, 22A Discrete SiC power MOSFET*, 2019.

[22] X. Ye, C. Chen, Y. Wang, G. Zhai, and G. J. Vachtsevanos, "Online condition monitoring of power mosfet gate oxide degradation based on miller platform voltage," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4776–4784, 2017.

[23] L. Yu, K. P. Cheung, J. Campbell, J. S. Suehle, and K. Sheng, "Oxide reliability of sic mos devices," in *2008 IEEE International Integrated Reliability Workshop Final Report*, pp. 141–144, IEEE, 2008.