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Critical design criterion for inductorless H-bridge driven piezoelectric-transformer-based power supplies

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Abstract—A methodology for predicting the ability of a piezoelectric transformer for achieving zero-voltage switching (ZVS) is presented. A describing function method is employed to obtain the PT equivalent circuit model operating under ZVS operation. This methodology is encapsulated within a critical criterion which, if fulfilled, guarantees efficient ZVS operation over a wide load range. The model provides a quantitative measure of a PT's ability to achieve ZVS using a H-bridge inductorless configuration. With the capacitance ratio profile provided by the analytical model, the limitations of the inductorless H-bridge driven PT-based inverters are indicated and guidelines for designing both PT and inverter control circuit are demonstrated.

Keywords—describing function, piezoelectric transformer, resonant power supply, zero-voltage switching

INTRODUCTION

Piezoelectric transformers (PTs) have raised great research interest for power electronic applications in the past few years owing to the development in materials science. PTs are generally made from hard piezoelectric materials (e.g. leadzirconate titanate), thus they exhibit low loss and high quality factor. PTs are exciting alternatives to traditional magnetic transformers since they offer many potential advantages including low electromagnetic interference, high power density (>40W/cm3), high efficiency, reduced weight and simpler manufacturing process [1]. Therefore, PTs have been extensively employed in LED lighting, battery charges, plasma generators and laptops [2]–[5].

In general, high efficiency operation can be achieved if PTs are operated close to their primary resonant frequency and this is usually achieved by using half-bridge, class-E and push-pull inverters. PTs typically exhibit large input capacitance owing to device geometry and thus it is difficult to achieve ZVS due to insufficient deadtime or charge provided by the resonant current. Although a series inductor can be used to ease ZVS, this reduces the power density, increase the size and cost [6]. For the inductorless configuration, the control circuit, deadtime and input-to-output-capacitance ratio should be carefully designed that resonant current is available to charge the PT input

capacitance to the DC rail during the deadtime period [7][8][9].

To guarantee ZVS, the circuit should be examined under all operating conditions to determine if sufficient charge can be provided to the PT input capacitor during the deadtime period [10]. Thus, the required deadtime can be a large proportion of the switching period and the assumption of constant current during the deadtime often used in the design of resonant converters is not valid [11]. In [12], a model is developed that describes the ZVS characteristics of an PT-based converter. However, inductorless overly conservative estimations regarding ZVS performance are provided due to the switching waveform shape assumption of the PT input capacitor voltage and the resonant current phase shift. An analytical model with improved accuracy is proposed in [13] using cyclic-mode analysis. The ZVS profile is generated as a function of deadtime, switching frequency and load. The ZVS boundary has been highlighted for different PTs and the appropriateness of PTs for different applications are assessed. This method, however, only provides a numerical solution. An alternative approach for the inductorless half-bridge configuration is developed in [8] using a describing function approach. A critical design criterion is derived to guarantee ZVS and the difficulty associated with multiple parameter control for ZVS operation is highlighted.

The novelty of this paper includes: 1) a new critical design criterion is developed for a H-bridge inverter; 2) the model develops a design rule based on the phase angle which extends the previous art; 3) limitations and design guidelines for both inverter and PT are indicated.

In this paper, an analytical model using the describing function approach is developed to evaluate a PT for achieving ZVS. A new critical design criterion for the inductorless Hbridge configuration is derived and the final model is only characterized by the input-to-output capacitance ratio and resonant current phase angle. The paper is organized as follows: Section II demonstrates the operation of the inductorless H-bridge PT-based inverter, PT equivalent circuit model and operating modes. Section III describes the derivation of the describing-function-based model for ZVS. The model is validated in section IV. In section V, the circuit

Jonathan N. Davidson Department of Electronic and Electrical Engineering University Of Sheffield Sheffield, UK jonathan.davidson@sheffield.ac.uk operating frequency and resonant current phase angle for achieving ZVS is demonstrated. Major findings are summarized in section VI and design guidelines are provided for both the H-bridge inverter and the PT.

II. OPERATION OF INDUCTORLESS H-BRIDGE PT-BASED POWER SUPPLIES

In general, when a PT operates near resonance, it exhibits high Q-factor band-pass filter behaviour and can be modelled by the Mason equivalent circuit, as shown in the dashed box in Fig. 1. The capacitances created between the electrodes of the PT are represented by the input capacitor (C_{in}) and the output capacitor (C_{out}). The mechanical resonant characteristics are represented by N, L_1 and C_1 , and the loss is modelled by R_1 . To achieve ZVS and to prevent a shootthrough event, sufficient deadtime should be applied between the MOSFETs gate signals.

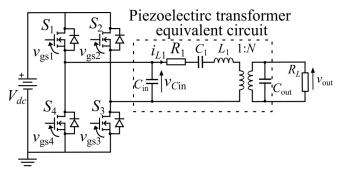


Fig. 1. Inductorless H-bridge PT-based inverter.

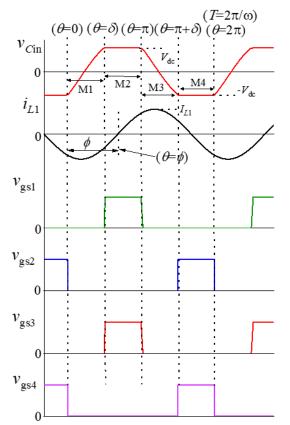


Fig. 2. Switching waveforms of the inductorless H-bridge PT-based inverter.

The typical switching waveforms of an inductorless Hbridge PT-based inverter under ZVS condition are shown in Fig. 2, where ω , i_{L1} and v_{Cin} are the switching frequency, resonant current and PT input capacitor voltage, respectively. The phase angles associated with the mode sequence are the deadtime interval δ and the resonant current phase lag ϕ . v_{gs1} , v_{gs2} , v_{gs3} , v_{gs4} are the MOSFETs gate signals. The resonant current, i_{L1} is assumed to be sinusoidal due to the high quality of the resonant tank and its magnitude is given as I_{L1} . To simplify the analysis of ZVS operation thereby reducing the number of piecewise description required for PT input voltage, it is assumed that the circuit exactly achieves ZVS and only operates under mode sequence M1 \rightarrow M2. As can be seen, ZVS can be achieved if $v_{Cin}(\delta) \geq V_{dc}$.

During a half-cycle period, the circuit shown in Fig. 1 can exist in one of the following operating modes.

M1: Prior to $\theta = 0$, both S_2 and S_4 are turned on and $v_{Cin}(0^-) = -V_{dc}$. At $\theta = 0$, all MOSFETs are turned off and therefore the resonant current, i_{L1} , circulates through C_{in} , thus v_{Cin} is being charged from $-V_{dc}$ towards V_{dc} .

M2: At $\theta = \delta$, C_{in} is fully charged by i_{L1} therefore $v_{Cin}(\delta) = V_{dc}$. S_1 and S_3 are turned on thereby achieving zero-voltage switching (ZVS).

To guarantee ZVS operation for an inductorless PT-based inverter, the critical criterion described in [8] from our previous work is adapted. ZVS can be achieved for all load conditions if the input-to-output capacitance ratio meets $C_{\rm in}/(N^2C_{\rm out}) \leq 2/\pi$ with $\pi/2$ (90°) deadtime angle. When the ZVS criterion is satisfied, the resonant current i_{L1} should be in-phase with the gate signals, and thereby ensuring the deadtime (or M1) begins at the negative peak of i_{L1} since this is where the quickest charging of $C_{\rm in}$ happens. Subsequently, the PT input voltage $v_{\rm Cin}$ is maximized by the end of the deadtime period.

III. MODEL DERIVATION

In this section, a mathematical model is derived to quantify the ZVS ability of a PT driven by an inductorless H-bridge inverter. The analysis is divided into two stages owing to the complexities of the derivation process. In stage I, the PT input voltage v_{Cin} at each operating mode is presented. In stage II, an expression for the input-to-output capacitance ratio is derived by equating the component-based circuit impedance to the signal-based equivalent impedance.

Key assumptions used in the model derivation are: 1) resonant current i_{L1} is sinusoidal since PTs are generally made by high Q-factor material; 2) ZVS is achieved exactly (i.e. $v_{Cin}(\delta) = V_{dc}$; 3) the deadtime angle $\delta = \frac{\pi}{2}$ based on the critical criterion developed from [8].

A ZVS factor K_{ZVS} can be defined as the voltage swing on C_{in} during the deadtime (assuming the body diodes do not conduct). ZVS is achieved exactly and $K_{ZVS} = 1$ when v_{Cin} swings from $-V_{dc}$ to $+V_{dc}$.

$$K_{\rm ZVS} = \frac{v_{\rm Cin}(\delta) - v_{\rm Cin}(0)}{2V_{\rm dc}} \tag{1}$$

A. Stage I- Switching waveforms of v_{Cin}

With reference to Fig. 2, the resonant current of the circuit i_{L1} can be expressed as

$$i_{L1}(t) = I_{L1}\sin(\omega t - \phi)$$

or
$$i_{L1}(\theta) = I_{L1}\sin(\theta - \phi)$$
(2)

where I_{L1} is the amplitude of the resonant current and ϕ is the phase angle.

As shown in Fig. 2, the PT input voltage can be decomposed into four piecewise sections during a full-cycle period. The general expression of the PT input voltage v_{Cin} can be found by evaluating the resonant current circulating through C_{in}

$$v_{\rm Cin}(\theta) = \frac{1}{\omega C_{\rm in}} \int -i_{L1}(\theta) d\theta + K$$
(3)

where K is the constant of the integration, and can be found by evaluating the capacitor voltage at the start of the corresponding mode.

During M1, $0 < \theta \le \delta(=\frac{\pi}{2})$, the PT input capacitor voltage can be expressed as

$$v_{Cin1}(\theta) = \frac{1}{\omega C_{in}} \int -i_{L1}(\theta) d\theta + K_1$$
$$= \frac{I_{L1}}{\omega C_{in}} \cos(\theta - \phi) + K_1$$
(4)

The constant of integration K_1 can be solved by evaluating the initial condition of M1, i.e., $v_{Cin1}(0) = -V_{dc}$. Thus,

$$K_1 = -V_{\rm dc} - \frac{I_{L1}}{\omega C_{\rm in}} \cos(\phi) \tag{5}$$

Hence,

$$v_{Cin1}(\theta) = \frac{I_{L1}}{\omega C_{in}} (\cos(\theta - \phi) - \cos(\phi)) - V_{dc}$$
⁽⁶⁾

The amplitude of the resonant current I_{L1} can be obtained by evaluating $v_{Cin1}\left(\frac{\pi}{2}\right) = V_{dc}$ from (6), thus,

$$I_{L1} = \frac{2C_{\rm in}V_{\rm dc}\omega}{\sin(\phi) - \cos(\phi)} \tag{7}$$

During M3, $\pi < \theta \leq \frac{3\pi}{2}$, the PT input capacitor voltage can be found by

$$v_{Cin3}(\theta) = \frac{1}{\omega C_{in}} \int -i_{L1}(\theta) d\theta + K_3$$
$$= \frac{I_{L1}}{\omega C_{in}} (\cos(\theta - \phi) + \cos(\phi)) + V_{dc} \qquad (8)$$

where the constant of integration K_3 is obtained by solving $v_{Cin3}(\pi) = V_{dc}$.

Substituting (7) into (6) and (8), provides the piecewise expression of the PT input capacitor voltage v_{Cin} in (9) (shown at the bottom of this page).

B. Stage II- Critical criterion for the H-bridge

In this stage, an expression for the input-to-output capacitor ratio C_n will be derived in terms of phase angle ϕ . The expression is obtained by equating the signal-based impedance of the PT to its component-based impedance. The signal-based impedance is found by dividing the fundamental component of the PT input voltage $v_{Cin<1>}$ by the fundamental component of the resonant current, $i_{L1<1>}$. $v_{Cin<1>}$ is obtained by extracting the fundamental component from the Fourier series of PT input voltage, v_{Cin} .

The sine-wave-referenced phasor of the fundamental component, $v_{Cin<1>}$ is

$$v_{Cin<1>} = \frac{j}{\pi} \int_0^{2\pi} v_{Cin}(\theta) e^{-j\theta} d\theta$$
(12)

Since the resonant current is assumed to be sinusoidal with its zero-crossing at $\theta = \phi$, the phasor of the resonant current $i_{L1 < 1>}$ is given by

$$i_{L1<1>} = I_{L1} e^{-j\phi}$$
(13)
= $I_{L1}(\cos \phi - j \sin \phi)$

Evaluating $v_{Cin<1>}$ and $i_{L1<1>}$ over a full switching cycle and substituting (7), leads to (10) and (11) (shown at the bottom of this page).

Therefore, the signal-based PT input impedance $Z_{in,sig}$ is given by using Ohm's law

$$Z_{\text{in,sig}} = \frac{v_{C\text{in}<1>}}{i_{L1<1>}} \tag{14}$$

The PT input impedance, $Z_{in,comp}$, determined by the circuit components, is the impedance looking into the PT input section ignoring C_{in} . Defining X_{series} as the series reactance of L_1 and C_1 combined (assuming R_1 is negligible) operating near the operating frequency ω ,

$$Z_{\text{in,comp}} = jX_{\text{series}} + \frac{1}{N^2 \left(j\omega C_{\text{out}} + \frac{1}{R_L}\right)}$$
(15)

To simplify following expressions, some normalisation factors and definitions are introduced: the series resonant

$$v_{Cin}(t) = \begin{cases} \frac{V_{dc}[2\cos(\theta - \phi) - \cos(\phi) - \sin(\phi)]}{\sin(\phi) - \cos(\phi)} & 0 < \theta \le \frac{\pi}{2} \\ V_{dc} & \frac{\pi}{2} < \theta \le \pi \\ \frac{V_{dc}[2\cos(\theta - \phi) + \cos(\phi) + \sin(\phi)]}{\sin(\phi) - \cos(\phi)} & \pi < \theta \le \frac{3\pi}{2} \\ -V_{dc} & \frac{3\pi}{2} < \theta \le 2\pi \end{cases}$$
(9)

$$v_{Cin<1>} = \frac{V_{dc}}{\pi(\cos(\phi) - \sin(\phi))} [(2\cos(\phi) - \pi\sin(\phi)) + j(2\sin(\phi) - \pi\cos(\phi))]$$
(10)
$$i_{L1<1>} = \frac{2C_{in}V_{dc}\omega}{\sin(\phi) - \cos(\phi)} (\cos(\phi) - j\sin(\phi))$$
(11)

frequency (ω_0) , operating frequency (ω_n) , input-to-output capacitance ratio (C_n) . It is assumed the circuit is operated with a matched load as this is the worst operating condition [8].

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}}, \omega_n = \frac{\omega}{\omega_0}, C_n = \frac{C_{\text{in}}}{N^2 C_{\text{out}}}, \omega_0 R_L C_{\text{out}} = 1$$
(16)

Substituting (10), (11) and (16) into (14), and equating (14) and (15) provides an analytical expression for C_n , (19) (shown in the bottom of next page).

Since C_n is a physical quantity, it must be real. Thus, (19) can be simplified by setting the imaginary part to zero and then solving for X_{series} which yields

$$X_{\text{series}} = \frac{4\cos(\phi)^2 + 4\cos(\phi)\sin(\phi) - \pi - 2}{4C_{\text{out}}N^2\omega(2\cos(\phi)^2 - 1)}$$
(17)

Finally, substituting (17) into (19) provides the relationship between the input-to-output capacitance ratio C_n and resonant current zero-crossing angle ϕ for the condition of K_{zvs} =1. Thus, to achieve ZVS,

$$C_n \le \frac{2 - 4\cos(\phi)^2}{\pi} \tag{18}$$

For certain values of ϕ , C_n will be negative and therefore ZVS cannot be achieved at these angles. This constrains the PT design space.

IV. MODEL VALIDATION

A. Ideal operating condition (lossless)

Fig. 3 shows a plot of C_n as a function of resonant current zero-crossing angle ϕ . The circuit operates at ω_n =1.02 with $\pi/2$ deadtime angle at the matched load condition, with the following Mason equivalent circuit parameters: L_1 =17.2mH, C_1 =77.8pF, R_1 =0 Ω , Q=1190, N=0.94, C_{in} =0.43nF and C_{out} =1.14nF. These are for the ring-dot PT shown in Fig. 5(b), assuming it has no damping.

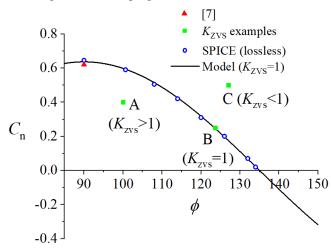


Fig. 3. Input-to-output capacitance ratio C_n as a function of resonant current phase angle ϕ in degrees.

As can be seen from Fig. 3, the proposed model correlates well with the SPICE simulation. For this particular operating

condition, the desirable operating region is between 90° and 135°, and the maximum achievable C_n is 0.63 at 90°. For completeness, a comparison is also made from the results presented in [7], indicated by the red triangle. It can be seen that the difference is negligible because that PT was made to meet the critical criterion with 90° phase shift to guarantee ZVS [8].

In general, ZVS can be achieved if v_{Cin} is charged to or above the DC rail during the deadtime interval. Fig. 4 shows the SPICE simulation of v_{Cin} for points labelled A, B, C in Fig. 3, demonstrating different types of v_{Cin} waveforms typically encountered for ZVS and non-ZVS condition and how K_{zvs} is determined. For the results presented in Fig. 3 and Fig. 4, the operating frequency is selected to provide $K_{zvs}=1$. For certain operating conditions, such as Fig. 4(c), ZVS cannot be achieved ($K_{zvs}<1$) since the input-to-output capacitance ratio is increased, more resonant current should be provided to charge C_{in} during the deadtime interval before the MOSFET turned on.

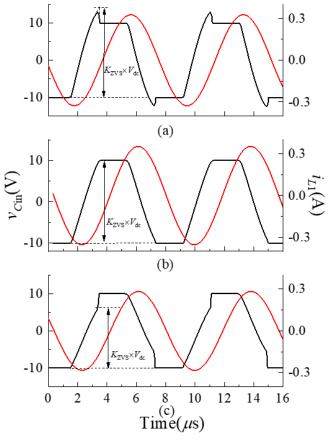


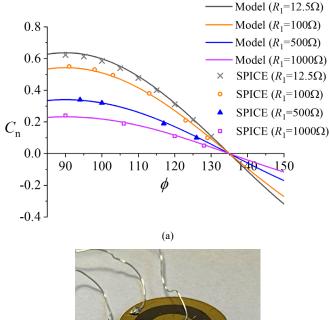
Fig. 4. v_{Cin} waveforms for (a) K_{zvs} =1 (b) K_{zvs} =1 and (c) K_{zvs} <1 (correspond to Fig. 3 points A, B and C, respectively).

B. Practical condition (with loss)

It should be noted that the damping resistor R_1 shown in the Mason equivalent circuit in Fig. 1 is not included in the model derivation, and therefore the critical criterion given in (18) is an ideal condition assuming efficient operation. The damping resistor, R_1 , typically models the mechanical and other losses.

$$C_n = \frac{\pi \sin(\phi) - 2\cos(\phi) + j[\pi \cos(\phi) - 2\sin(\phi)]}{\pi [2C_{\text{out}}N^2 \sin(\phi) X_{\text{series}}\omega + \cos(\phi) - \sin(\phi)] + j\pi [2C_{\text{out}}N^2 \cos(\phi) X_{\text{series}}\omega - \cos(\phi) - \sin(\phi)]}$$
(19)

Fig. 5 shows the validation of the proposed model using a ring-dot radial-mode PT, with the following Mason equivalent circuit parameters: $L_1=17.2$ mH, $C_1=77.8$ pF, $R_1=12.5\Omega$, Q=1190, N=0.94, $C_{in}=0.43$ nF and $C_{out}=1.14$ nF. It should be noted that only the damping resistor R_1 is increased compared with the PT parameters used in previous section. Various alternative values of the damping resistor R_1 are also evaluated to validate the model. As can be seen from Fig. 5(a), for achieving $K_{zvs}=1$ at practical values of damping resistors, the proposed model still correlates well with SPICE.



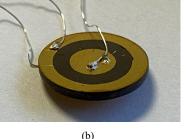


Fig. 5. (a) Model validation with losses and (b) the ring-dot radial-mode PT.

V. DISCUSSION AND DESIGN GUIDLINES

From the analysis presented in this paper, it can be seen that K_{zvs} =1 can be guaranteed for the inductorless H-bridge PT-based inverter if the input-to-output capacitance ratio C_n and resonant current phase angle ϕ meet the condition in (18). The capacitance ratio should be accounted for during the PT design process if the inductorless H-bridge configuration is employed, since C_n significantly limits the geometry of the input and output electrodes thereby restricting the PT design. Therefore, when designing a PT, in addition to normal considerations of operating temperature and suppression of spurious vibration [14], the ability to achieve ZVS in accordance with (18) should be considered.

The control circuit is a normal requirement for the practical implementation of a PT-based inverter. To ensure ZVS, the optimal frequency should be continuously tracked. This can be achieved in several ways, such as by synchronising bridge switching events to the resonant current using a phase-locked loop (PLL) [7] and phase compensation using a self-oscillating loop [2]. One design challenge of the PT-based inverter is that the resonant frequency drifts since it varies with respect to load and temperature [7]. Conventional approaches such as [2] and [7] assume a fixed phase angle ϕ

and therefore the maximum capacitor ratio for this type of design can be found directly from (18).

These findings demonstrated in this work are extensions to those presented in [8]. In [8], it is indicated that ZVS is guaranteed if the input-to-output capacitance ratio C_n meets $2/\pi$ and resonant current phase angle ϕ is $\pi/2$. This single operating point agrees with (18). In addition, the key assumption used in [8] is that the circuit operates at exactly the series resonant frequency (i.e. $\omega_n = 1$).

VI. CONCLUSIONS

An analytical model of the PT operating at $K_{zvs}=1$ is derived to obtain a criterion which guarantees zero-voltage switching. This criterion fixes the maximum input-to-output capacitor ratio for a given zero-crossing angle of the resonant current with respect to the gate drive signals. The general requirements regarding $K_{zvs}=1$ are provided for both lossy and lossless conditions. Simulation and experimental results demonstrate the accuracy of the criterion. The proposed model extends the previous art by developing the critical criterion based on the resonant current phase angle. Design recommendations in terms of both PTs and inverter control circuit are provided.

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