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Resonant current estimation and phase-locked loop control system for inductorless step-up single piezo element-based (SUPRC) DC-DC converter

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***Abstract*—An FPGA-based control system for the step-up piezo resonator-based DC-DC converter is presented. An all-digital phase-locked loop (ADPLL) is used to self-start the converter and locks on to the resonant current, which is extracted using a current estimator. The PLL and several analogue comparator outputs are used to generate the gate signals for both MOSFETS. A new method is presented for determining the optimal high side switch duty cycle, which ensures zero-voltage switching on both MOSFETS. A practical converter is constructed, and experimental results presented, showing the effectiveness of the converter across a range of operating conditions.**

Keywords— Piezoelectric Devices, Resonant Converter, Control, FPGA, DC-DC converter

I. Introduction

Piezoelectric power converters have surged in popularity in the past few years, with researchers finding several key applications for such converter [1]–[5]. Their low losses, high Q factors and high power densities make them ideal for low to medium power (<50W) applications [6].

Typical piezoelectric converters make use of piezoelectric transformers (PTs), which consist of one or more piezoelectric element, which transform energy from an input section to an output section using mechanical vibration. The half-bridge topology is popular in recent publications, with many converters requiring an inductor in series with the PT to achieve zero-voltage switching (ZVS). However, given one of the best features of a PT is its ability to be used in harsh environments with minimal EMI/EMC, an additional inductor is unattractive. Recent works [7],[8]–[10] have shown that, with careful design, the half-bridge resonant converter can be built without an external inductor while still achieving ZVS. As a result, inductorless half-bridge resonant converters have become a well-researched topic in recent years.

One of the challenges with the half-bridge converter is that the energy stored in the PT's resonant tank is responsible for charging the PT input capacitance during deadtime (thus allowing ZVS). Since the input capacitance is typically large, large deadtimes are required. Most commonly, a 25% fixed deadtime is required to ensure ZVS is achieved for all load conditions [7]. If the deadtime is fixed, then PWM control cannot be used to control the output voltage as is common in power converters [11]. Therefore, especially given the very narrow range of operating frequencies (given the high Q factor), output voltage control is difficult in PT based converters, with many authors preferring burst-mode control or tunable PTs [12]–[14].

Several authors have presented piezo resonator (PR) based resonant converters [15]–[17]. These converters are similarly inductorless but, owing to the converter topology, a much wider range of output voltages can be achieved under ZVS conditions compared to a PT based converter. These more versatile converters can still achieve high efficiency whilst producing similar output power levels to PT based approaches. The converter described in [16] is of particular interest, as the authors present a method of step-up power conversion. However, as discussed in [16], one of the downsides of this converter is that complex control is required. Reference [18] presents a field programmable gate array (FPGA) based controller, running a state machine which operates at a fixed clock frequency and uses several analogue comparators to provide input to the state machine. However, the fixed clock frequency requires some manual interaction to account for changes in temperature, load, and duty cycle—all of which affect the ideal operating frequency.

This paper presents an improved control method for the PR converter presented in [16], named here as the inductorless step-up piezo resonator DC-DC converter (SUPRC). Similar to [18], an FPGA based controller is developed. An all-digital PLL (ADPLL) is used to optimally determine the operating frequency. The PLL locks on to the resonant frequency of the piezo resonator, which is measured using a current estimation technique. A new method to determine the optimal duty cycle of the high side switch is also presented. A practical converter is built, and the experimental results are presented.

II. Converter description

The SUPRC is shown in Fig. 1 which is a simplified version of the circuit presented in [16] where the number of MOSFETs have been halved, simplifying the control. The redundant MOSFETs are replaced by diodes D_1 and D_2. As [16] states, this topology can be used for both step-up and a step-down applications; however, the work in this paper will focus only on the step-up operation of the converter.

The operation of this converter can be decomposed into six modes (circuit configurations), these are summarized below:

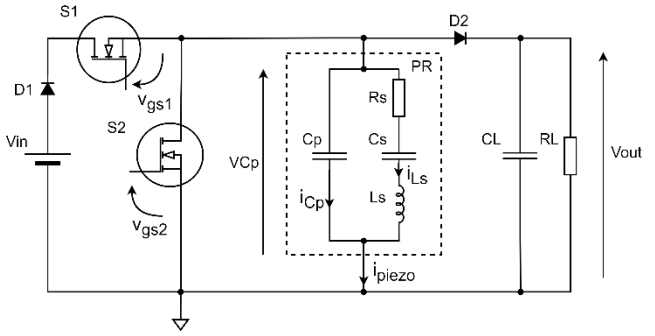

Fig. 1 – *SUPRC*, dashed box indicates the piezo resonator element

M1 ($t_0 \rightarrow t_1$): Prior to start of a cycle, D_2 is conducting such that $V_{Cp} = V_{out} + V_{DF}$, where V_{DF} is the forward voltage drop of D_2. Both MOSFETs S_1 and S_2 are turned off at t_0, as the current i_{Ls} undergoes a positive zero crossing. Diode D_2 also turns off. During M1, i_{Ls} circulates within the PR discharging C_p and causing V_{Cp} to decrease until it reaches V_{in}. Since $V_{Cp} < V_{out}$, D_2 is reverse-biased and so C_L provides the energy to the load

M2 ($t_1 \rightarrow t_2$): At t_1, $V_{Cp} = V_{in}$ and so S_1 is turned on to achieve ZVS. Energy is supplied to the resonator during M2 through S_1.

M3 ($t_2 \rightarrow t_3$): S_1 is turned off at t_2, where t_2 is chosen to allow sufficient time for i_{Ls} to cause V_{Cp} to reach 0 at t_3

M4 ($t_3 \rightarrow t_4$): At t_3, i_{Ls} undergoes a negative zero crossing and $V_{Cp} = 0$, therefore, S_2 is turned on at t_3 to achieve ZVS, thus $V_{Cp} = 0$ for the duration of M4. i_{Ls} flows through S_2.

M5 ($t_4 \rightarrow t_5$): At t_4, S_2 is turned off, the negative i_{Ls} charges C_p, and increases V_{Cp}. At t_5, $V_{Cp} = V_{out} + V_{DF}$.

M6 ($t_5 \rightarrow t_6$): $V_{Cp} = V_{out} + V_{DF}$, D_2 is forward-biased, thus energy is provided from the resonator to R_L and C_L. At $t_6 = t_0 + T_s$ (where T_s is the cycle period), i_{Ls} undergoes another positive zero crossing and the whole cycle repeats.

If the converter is successfully operated from M1 → M6 then the waveforms in Fig. 2 are achieved. Several careful design choices should be made. Firstly, the resonator should have sufficiently high Q factor to ensure the resonator current is sinusoidal during operation, as other harmonics can cause unwanted charging/discharging of C_p and can make determining the phase of the resonant current (vital for optimal control) difficult. Secondly, the resonator should have minimal damping (losses) for high efficiency, low losses and low heat rise. Both D_1 and D_2 should be fast switching diodes, such as Schottky diodes, and should have low forward voltage drops and adequate PIV ratings. Finally, C_L such be sufficiently large such that it can sustain the desired output voltage across the load across the full cycle and to minimise output voltage ripple.

If appropriate control of the converter is achieved, the gain of the resulting converter (assuming no losses) can be estimated by [16],

$$G = \frac{2 + R_L C_0 \omega (1 + \cos(\omega t_4))/2\pi}{1 - \cos(\omega t_4)} \qquad (1)$$

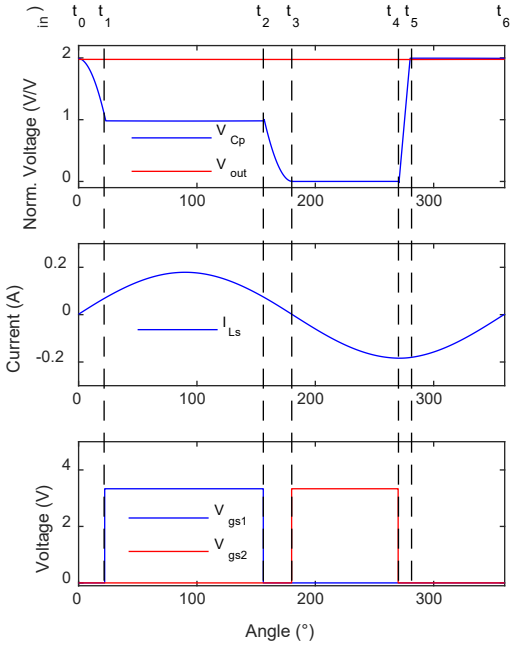

Fig. 2 – Waveforms for the SUPRC

Based on (1), it can be shown that the gain of the converter is controlled by t_4, with larger t_4 giving larger voltage gain. It is important to note that this equation is from the assumption that $Q_{in} + Q_{M3} + Q_{out} = 0$, and therefore assumes sufficient energy has been injected into the resonator during M2 to provide the desired output voltage and thus power. Fig. 3 summarizes the switch function of both S_1 and S_2.

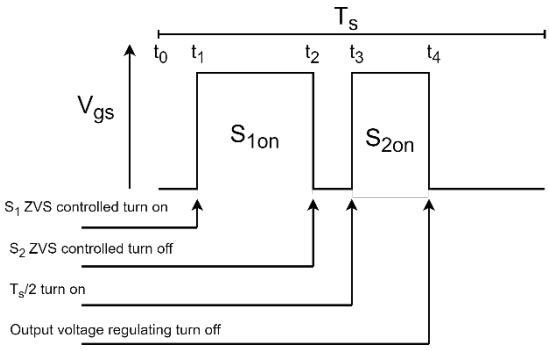

Fig. 3 – Description of the switch function

III. Controller

Control of this converter is more complex than many PT based converters [8], owing mainly to difficultly in determining the duty cycle of S_1 .Whereas PT based converters typically operate both switches in a complementary manner and with a duty cycle of 25 %, the duty cycle for S_1 must be chosen to ensure sufficient time for i_{Ls} to discharge V_{Cp} to 0 at t_3. The duty cycle of S_1 cannot be chosen *a priori*, as it depends on a variety of factors including frequency, the S_2 duty cycle, load and temperature.

Additional control challenges arise from using piezoelectric devices in converters. The resonant current cannot be easily measured as it is not strictly an electrical

property but rather equivalent to the vibration velocity of the device. Therefore, the resonant current must be estimated. As the timing of each mode should be synchronized to the resonant current, accurate measurement of this property is vital for optimum performance.

Initially, the PLL (which is not yet locked) will provide a starting signal at approximately the desired frequency for the other control elements. The PLL's frequency will increase until the PLL output signal is in phase with the resonant current (at resonance). t_3 can be easily determined as it occurs on the falling edge of the PLL output signal. Several comparators provide input to a novel control element which determines optimal t_1 and t_2 based on the V_{Cp} voltage at t_1 and t_3 respectively. Finally, t_4 is manually set to achieve the desired output voltage. In this implementation, the control system will be designed and implemented on an FPGA using VHDL. A block diagram for the controller is shown in Fig. 4

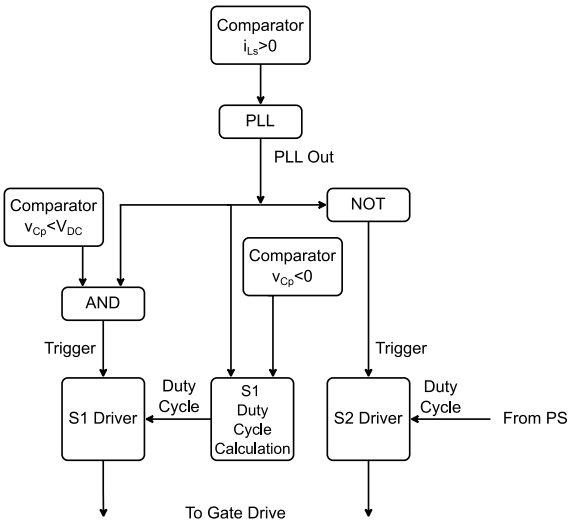

Fig. 4 - Simplified block diagram of the overall controller

A. Resonant current estimation

The resonant current i_{Ls} cannot be directly measured in piezo devices, as it is an equivalent-circuit analogue of mechanical vibration. However, the total current flowing into the resonator can be measured. This measured current has two parts: the resonant current and the current through C_p. As the current through C_p is 0 when V_{Cp} is constant, the resonator current is equal to i_{Ls} for modes 2, 4 and 6. However, for the following controller, the zero crossings in the current waveform are the main regions of interest and these occur on the boundaries of these modes. Therefore, detecting the zero crossings in the resonator current (i_piezo), should give the same zero crossings at the resonant current (i_{Ls}) but any inaccuracy (such as during start up) can cause instability in the PLL or cause the PLL to lock onto an incorrect frequency. We therefore use a current estimator to reconstruct the resonant current. This circuit is shown in Fig. 5 and is similar to that used in [8], [9].

In Fig. 5, three additional passive elements are added to the converter, $C_\mathrm{a}, R_\mathrm{a}$ and R_b. R_b is a current shunt which allows the resonator current (i_piezo) to be measured at V_B. C_a and R_a together form a differentiator, which generates a scaled version of the current through C_p (i_{Cp}), at V_A. By carefully selecting the values for these components, for example with $C_\mathrm{a} = C_\mathrm{p}/10$, $R_\mathrm{a} = 10\Omega$ and $R_\mathrm{b} = 1\Omega$, then the voltages (in volts) at V_A and V_B are identical to i_{Cp} and i_piezo (in amperes).

To estimate the resonant current from these signals, we subtract V_A from V_B. This is achieved using a differential amplifier, as shown in Fig. 5. The output of the differential amplifier, V_ec is given by [8],

$$V_\mathrm{ec} = V_\mathrm{B}\frac{R_\mathrm{f}/(R_\mathrm{f}+R_\mathrm{e})}{R_\mathrm{c}/(R_\mathrm{c}+R_\mathrm{d})} - V_\mathrm{A}\frac{R_\mathrm{d}}{R_\mathrm{c}} \quad (2)$$

Assuming the components given in the paragraph above are used and with $R_\mathrm{c} = R_\mathrm{d} = R_\mathrm{e} = R_\mathrm{f} = 10\mathrm{k}\Omega$, the resonant current is found as $V_\mathrm{ec} = V_\mathrm{B} - V_\mathrm{A}$. Finally, this signal goes to a fast comparator (MAX9201) which generates a square wave output which is in phase with the resonant current.

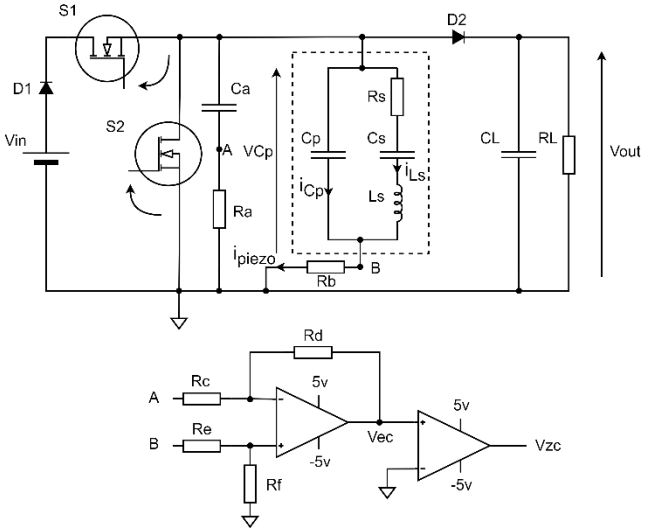

Fig. 5 - SUPRC with additional current estimation circuitry

B. Phase locked loop (PLL)

In this implementation an all-digital PLL (ADPLL) is used, based on similar PLLs in [19], [20]. This PLL design is simple to implement, does not require a filter and can easily to be tuned for a specific application. A block diagram of the implemented PLL is given in Fig. 6.

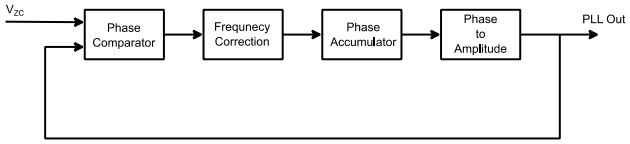

Fig. 6 – Block diagram of the ADPLL

1) Phase accumulator and phase to amplitude converter

The phase accumulator is a key part of most digital PLL implementations. In this implementation a 48-bit accumulator is used, which can store a maximum value of 2.81×10^{14}. For this PLL, on each clock cycle a value (PHASEADD) is added to the accumulator, incrementing the phase, with the accumulator's value wrapping to 0 on overflow. The value in the phase accumulator's register relates to the phase of the desired output signal; for example, a value of 0 in the phase accumulator relates to 0 phase, 1.41×10^{14} corresponds to 180° and finally, 2.81×10^{14} corresponds to marginally below 360°. Therefore, by

carefully choosing the PHASEADD that is added to the register each clock cycle, the desired output frequency is set.

The present value of the phase accumulator is passed to the phase-to-amplitude converter. This block generates an output signal based on the phase accumulator's value. For this application, a square wave output (PLL out) is required, therefore this block is simple. The phase to amplitude block outputs a '1' until the phase accumulator reaches $2^{48}/2$ (180°), where it then outputs a '0', producing a 50% duty cycle square wave at the desired frequency.

2) Phase comparator

The phase comparator compares the input signal (from the current estimator) and the output of the PLL and generates a 2-bit error signal, similar to phase comparator 2 in the 4046 analogue PLL. The least significant bit describes whether the two inputs are equal (either "1" or "0"), outputting a '0' if they are equal and a "1" if they are not. The other bit describes how to correct for any error, either by speeding up the PLL (higher frequency) or by slowing the PLL (lower frequency). This is achieved by keeping track of which state (either "1" or "0") the input and PLL output were in during the last point at which both signals agreed (i.e. "00" output). Then, by observing which input (PLL out or estimated current) changed first, allows this bit to be determined. An equivalent logic circuit for this block is shown in Fig. 7.

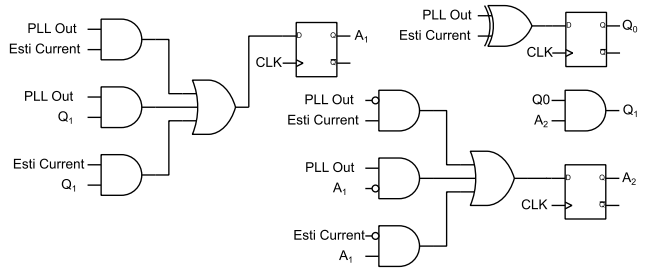

Fig. 7 - Phase comparator, with the PLL output and estimated current ($i_{Ls} > 0$) as inputs and a 2-bit output Q

3) Frequency correction

The frequency correction block is tasked with supplying the phase accumulator with a value (PHASEADD) which is subsequently added to the phase accumulator on each base clock (100 MHz) cycle. Again, an accumulator is used here, with the initial value of PHASEADD determining the initial starting PLL output frequency. PHASEADD is then adjusted based on the 2-bit phase error signal from the phase comparator,

- If there is no error ("00") from the phase comparator, the frequency correction block outputs the present PHASEADD value to the phase accumulator.
- If there is an error and the PLL frequency is too low ("01"), then PHASEADD is increased and then passed to the phase accumulator.
- If the PLL frequency is too high ("11") then PHASEADD is decreased and passed to the phase accumulator.

The amount by which the PHASEADD is changed upon an error from the phase comparator (either 01 or 11) should be carefully chosen to be large enough to ensure fast frequency adjustments but not too large as this will cause overshoot and frequency oscillation. In this implementation PHASEADD was only incremented or decremented by 1 on each clock cycle where there was a phase error.

Maximum and minimum PLL frequencies can be set here, by capping the max/min value allowed in the accumulator. These can be calculated using,

$$\text{Max}/_{\text{Min}}\ \text{PHASEADD} = \frac{2^{48}}{\text{CLK}/_{\text{Freq}}} \tag{3}$$

where Freq is the desired max or min frequency and CLK is the base clock of the FPGA, which is 100 MHz in this implementation.

C. S_1 and S_2 drive signals

The S_1 and S_2 drive signals are generated from the PLL output. The key element of both S_1 and S_2 drive signal blocks is a counter which increments on the FPGA base clock (100MHz). When a trigger signal to the block goes high, the counter starts counting and the output of each block goes high and stays high until the counter reaches a certain threshold value, at which point the output goes low. Therefore, the threshold value and the trigger signal to each block is of key importance, as this determines when the switch turns on and the duty cycle of the switch, respectively.

1) High side (S_1) driver – Trigger signal and threshold

The trigger signal and threshold for S_1 is difficult to generate as both t_1 and t_2 change dynamically based on the operation of the converter. S_1 should turn on when V_{Cp} drops to V_{in}. S_1 should then turn off to ensure enough time for V_{Cp} to drop to 0 at $T_s/2$. It is important to note here that, $(t_2 - t_1)$ should be maximised to maximise the time for energy to be injected into the resonator.

A comparator is used to determine when $V_{Cp} < V_{in}$. This signal goes through a SR flip flop ensuring stability in the input signal. This output of the SR flip flop is used to trigger the high side driver block, causing S_1 to turn on.

To generate the threshold value, an additional counter is used. A comparator is used to indicate when $V_{Cp} < 0$, then the counter increments on each base clock (100 MHz) cycle measuring how many cycles have passed between $V_{Cp} < 0$ and t_3. Based on the value of this counter at t_3 the threshold value is adjusted,

- If the counter is 0 at t_3, then S_1 has turned off too late, thus we should decrease the threshold value (lowering S_1 duty cycle).
- If the counter has a value of 1, then S_1 has turned off at exactly the correct point and the threshold value is kept the same.
- If the counter has a value >1, S_1 has turned off too early and so the threshold value is increased.

2) Low side (S_2) driver – Trigger signal and threshold

The low side switch S_2 should turn on at t_3 which should be at $T_s/2$, where $T_s = 1/f_s$. This can simply be created by inverting the output of the PLL using an NOT gate, which provides the trigger signal.

The threshold for this block is set according to the desired t_4 value, which, as discussed earlier, sets the desired output voltage or gain. In this implementation t_4 will be set manually; however, a simple closed-loop controller to regulate the output voltage could be used.

D. Additional considerations

As the on and off times of both switches are set by a combination of external signals and counters, there is potential for errors to occur especially during start up. One of the issues arising from these errors is both switches being on at the same time, leading to a shoot-through event and potential damage to one or both switches. A shoot-though-protection block is used which passes drive signals during normal (i.e. no shoot through) operation but, if both switches are set to be on, it inverts both switches (compared to their previous states) until the shoot-through condition clears.

IV. Implementation

The control system described above is implemented on a PYNQ-Z1 Xilinx ZYNQ FPGA. The PYNQ system allows the programmable logic (PL) in the FPGA to be interfaced with a python script running on the processing system (PS). The PYNQ-Z1 exposes a webserver running a Jupyter notebook, which allows fast prototyping from a browser. The proposed control system takes advantage of several Xilinx IP blocks, mainly the AXI GPIO which allow interfacing between PL and PS. This means max/min frequencies, propagation delays, S_2 duty cycle can all be set remotely from a Python script. The flip flop and LUT utilization for the main elements of the control system are shown in Table 1.

Table 1 – Flip flop and LUT usage for the proposed controller

Element	PLL	Low side S_2 driver	High side S_1 driver	Shoot-through protection
Flip flops (FFs)	82	17	117	5
Look up tables (LUTs)	186	284	92	4

From Table 1, we can calculate that only a very small (<3%) proportion of the available logic cells on this FPGA are being used, making this controller suitable for a smaller, lower cost FPGA. Additionally, extra logic is required to avoid issues with propagation delay occurring from the gate drive IC, therefore, reducing the propagation delay would further simplify and lower utilization in the S_1 and S_2 drivers. It is also worth noting that other elements (such as AXI GPIO and interconnects) use ~1500 FFs and ~1500 LUTs.

V. Validation

To validate this control method, a prototype converter is constructed using a SMD30T21F1000S piezo resonator from Steminc as shown in Fig. 8. The equivalent circuit properties for the piezoelectric disk are estimated using [21] and are given in Table 2.

Fig. 8 - Piezo resonator

Table 2 - SMD30T21F1000S equivalent circuit properties

R_s	L_s	C_s	C_p	F_0	R_a	R_b	C_a
2.22 Ω	4.47 mH	1.02 nF	2.54 nF	74.51 kHz	10 Ω	1 Ω	470 pF

The experimental waveforms for this converter are shown in Fig. 9, when driven with a 12V input, with a 1 kΩ load and a 28% S_2 duty cycle. For this resonator, the min and max operating frequency of the PLL is set to 70 kHz and 80 kHz respectively. As shown in Fig. 9, the controller achieves ZVS on both S_1 and S_2, maximising S_1 duty cycle.

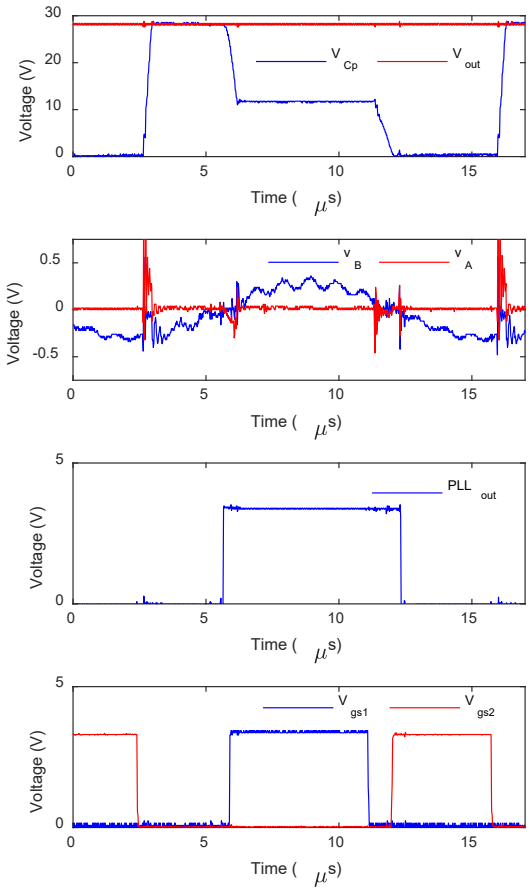

Fig. 9 - Experimental waveforms of the SUPRC during operation with the proposed control method and with a S_2 duty cycle of 28%

Fig. 10 shows V_{Cp} at several different S_2 duty cycles. As expected, with greater duty cycle, the larger the output voltage [16]. Additionally, S_1 duty cycle increases with increasing S_2 duty cycle, as more energy must be provided to the resonator to account for the higher output voltage and subsequent higher power. Additionally, we can see that larger currents mean it takes less time for C_p to charge and discharge to the desired level. Additionally, we can observe that the controller is able to achieve ZVS on both switches

across the whole range of duty cycles tested. Finally, owing to the optimum operation of the converter across the range of duty cycles, it is clear the PLL, and current estimator is able to accurately determine and lock onto the optimum frequency of operation.

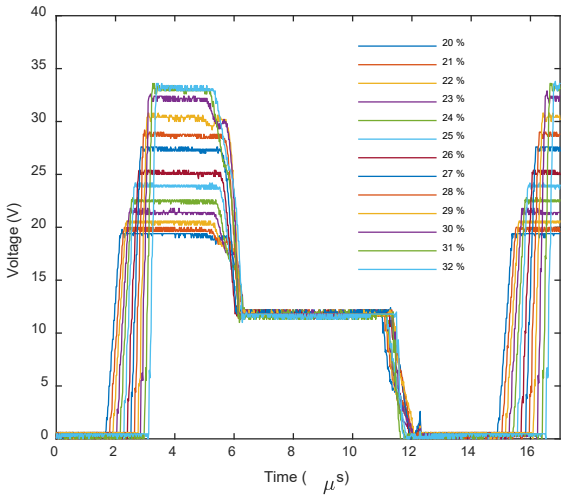

Fig. 10 – Experimental measurement of V_{cp} across several S_2 duty cycles

VI. Conclusions

This paper has presented an improved controller for the converter presented in [16]. It uses a current estimator and PLL to generate a main clock, self-starting the circuit and ensuring operation at the optimal frequency. A new method is presented for determining the high side switch duty cycle for maximising energy transfer and ensuring ZVS. The resulting converter is implemented on a PYNQ Z1 FPGA and experimental results are presented, showing optimal operation.

VII. Acknowledgment

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