This is a repository copy of *Fabrication of semi-polar (11-22) GaN V-groove MOSFET using wet etching trench opening technique*.

White Rose Research Online URL for this paper:
https://eprints.whiterose.ac.uk/190726/

Version: Accepted Version

Article:

Yin, Y., Pinchbeck, J., O'Regan, C. et al. (3 more authors) (2022) Fabrication of semi-polar (11-22) GaN V-groove MOSFET using wet etching trench opening technique. IEEE Electron Device Letters, 43 (10). pp. 1641-1644. ISSN 0741-3106

https://doi.org/10.1109/led.2022.3203633

© 2022 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other users, including reprinting/ republishing this material for advertising or promotional purposes, creating new collective works for resale or redistribution to servers or lists, or reuse of any copyrighted components of this work in other works. Reproduced in accordance with the publisher's self-archiving policy.

Reuse

Items deposited in White Rose Research Online are protected by copyright, with all rights reserved unless indicated otherwise. They may be downloaded and/or printed for private study, or other acts as permitted by national copyright laws. The publisher or other rights holders may allow further reproduction and re-use of the full text version. This is indicated by the licence information on the White Rose Research Online record for the item.

Takedown

If you consider content in White Rose Research Online to be in breach of UK law, please notify us by emailing eprints@whiterose.ac.uk including the URL of the record and the reason for the withdrawal request.

eprints@whiterose.ac.uk
https://eprints.whiterose.ac.uk/

Fabrication of Semi-Polar (11-22) GaN V-groove MOSFET Using Wet Etching Trench Opening Technique

Yidi Yin, *Graduate Student Member, IEEE*, Joseph Pinchbeck, Colm O'Regan, Ivor Guiney, David J. Wallis, and Kean Boon Lee

***Abstract*—In this letter, we report the fabrication of an enhancement-mode V-groove metal oxide semiconductor field-effect transistor on semi-polar (11-22) GaN platform. A wet crystallographic hydroxide-based etching approach to achieve a vertical inversion trench sidewall is utilized. This novel fabrication method enables the formation of the vertical trench sidewall channel conduction without the need for a conventional chlorine-based dry etching. The fabricated VMOSFET exhibit a threshold voltage of 9.49 V, a current ON/OFF ratio of >10^7, an ON-state resistance of 8.0 mΩ.cm^2, and an output current of 516 A/cm^2.**

***Index Terms*— Crystallographic etching, Semi-polar gallium nitride, GaN vertical transistors, V-groove MOSFET.**

I. Introduction

GAN and its related materials have great potential in the field of power electronics and light-emitting diodes (LEDs). Recent demonstrations of monolithic integration of c-plane GaN LEDs with vertical GaN transistors could provide a path for ultra-compact display applications such as virtual reality and augmented reality [1-9]. However, c-plane (0001) GaN materials has fundamental limitations: 1) for the LED, it is challenging to achieve a high quantum efficiency due to the quantum-confined stark effect and to incorporate a high indium content in the quantum wells for long wavelength emissions [10], [11]. 2) for the transistors, due to the wet chemical inert properties [12] of c-plane GaN, the demonstrated vertical transistors [13-18] have so far relied on complicated plasma dry etching techniques which can leave crystal defects and post-etching treatment and/or channel regrowth to achieve vertical sidewall channel conduction.

Semi-polar GaN and in particularly (11-22) GaN, on the other hand, has been shown to suppress the quantum-confined Stark effect as well as improve the indium incorporation efficiency compared to c-plane GaN [19]. Despite the promising results on semi-polar GaN LEDs, to date, the discussions of the transistor operations on the semi-polar (11-22) GaN are limited. The advantage of transistor fabrications on the (11-22) GaN is twofold: firstly, it allows monolithic integration with semi-polar LEDs. Secondly, wet etching is possible on the (11-22) GaN because the Ga-dangling bonds could be more easily attacked by the wet etchants [20], [21] which allows the formation vertical sidewall channel without the need for dry plasma etching.

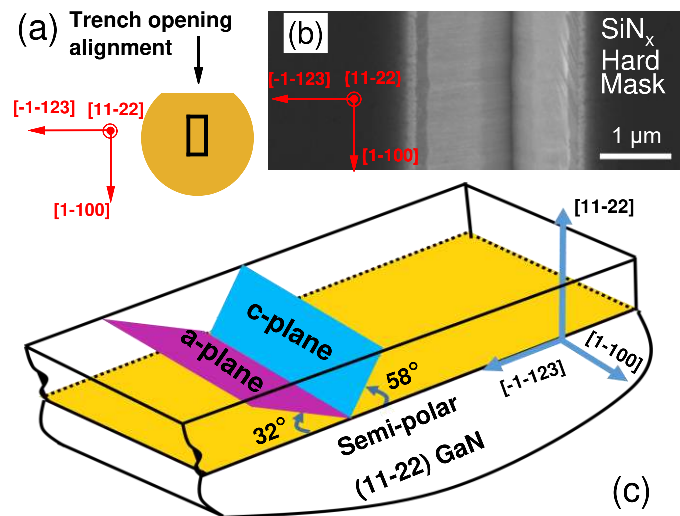

Fig. 1. (a) Schematic of the trench opening alignment orientation for the semi-polar (11-22) GaN VMOSFET, (b) top-view SEM image of the KOH etched trench sidewall and (c) schematic of the c-plane & a-plane in the semi-polar GaN layer.

In this work, we demonstrate the semi-polar (11-22) GaN V-groove metal oxide semiconductor field-effect transistor (VMOSFET) with a novel crystallographic hydroxide-based

Manuscript received xxxx; revised xxxx. This work was supported by the U.K. Engineering and Physical Sciences Research Council under Grant EP/P006973/1 and EP/T013001/1. The review of this letter was arranged by Editor xxx. (Corresponding authors: Yidi Yin; Kean Boon Lee.)

Yidi Yin, Joseph Pinchbeck, and Kean Boon Lee are with the Department of Electronic and Electrical Engineering, University of Sheffield, Sheffield, S1 3JD, U.K. (e-mail: yyin15@sheffield.ac.uk; kboon.lee@sheffield.ac.uk).

Colm O'Regan is with the Sorby Centre for Electron Microscopy, Department of Materials Science and Engineering, University of Sheffield, S3 7HQ, U.K.

Ivor Guiney is with the Department of Materials Science and Metallurgy, University of Cambridge, Cambridge, CB3 0FS, U.K.

David J. Wallis is with Cardiff University, Engineering, Queens Building, Cardiff, CF24 3AA, U.K. and Department of Materials Science and Metallurgy, University of Cambridge, Cambridge, CB3 0FS, U.K.

wet etching technique to form the vertical trench sidewalls for the channel conduction. The semi-polar (11-22) GaN transistor exhibits a threshold voltage (V_{th}) of 9.49 V, an ON-state resistance (R_{on}) of 8.0 mΩ.cm^2, an I_{ON}/I_{OFF} ratio > 10^7 and a breakdown voltage (V_{BD}) of 150 V.

II. Epitaxial Structure and Device Fabrication

The semi-polar (11-22) GaN epitaxial structure in this work was grown on an m-plane sapphire substrate using the metal-organic chemical vapor deposition method. The epitaxial structure is as follow: 0.25 µm n^+-GaN (Si: ~ 5×10^{18} cm^{-3}), 0.5 µm p^+-GaN (Mg: ~ 1×10^{19} cm^{-3}), 3.0 µm n^--GaN (Si: ~ 5×10^{17} cm^{-3}), and 0.5 µm n^+-GaN (Si: ~ 5×10^{18} cm^{-3}). The MOSFET fabrication started by depositing 300 nm of SiN_x using inductively coupled plasma chemical vapor deposition (ICPCVD) to serve as a hard mask. The via opening window aligned to [1-100] and [-1-123] orientations [21], [22], as shown in Fig. 1 (a), was defined using optical photolithography and the SiN_x hard mask was etched using reactive ion etching.

30 M potassium hydroxide (KOH) solution at 95 ℃ was used for etching the (11-22) GaN to form a trench. The etching rate of the semi-polar *n*-GaN and *p*-GaN was ~98 nm/min and ~13 nm/min, respectively, along the - [11-22] direction established from the etching trials. The slower etch rate of the *p*-GaN is due to the repulsion of OH^- by p-type doping [23]. The total wet etch time for the trench is 50 mins and the trench depth is ~1.5 µm.

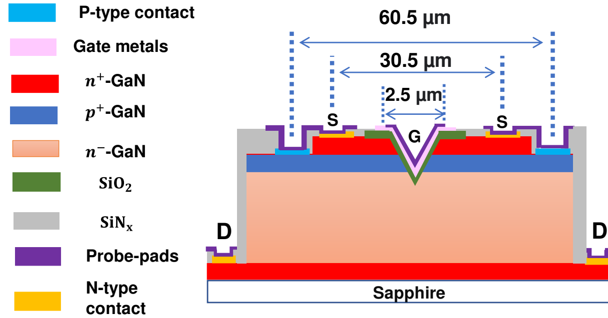

Fig. 2. Schematic diagram of the semi-polar (11-22) GaN VMOSFET.

Once the trench opening was wet-etched to the n^--GaN drift region as shown in Fig. 1 (b), hydrofluoric acid was used to remove the SiN_x hard mask. Following this, a 60 nm SiO_2 layer was deposited by plasma enhanced chemical vapor deposition at 300 ℃ to serve as the gate dielectric. Afterwards, the ICP dry etching was used for accessing the middle *p*-GaN and bottom n^--GaN, following by thermal annealing at 500 ℃ in N_2 for 10 mins to remove the plasma induced damage on the dry-etched sidewalls and to attempt to activate the Mg in the *p*-GaN layer. The activation temperature of 500 ℃ is limited by the deposition temperature of the gate dielectric. Metal stacks of Ti/Al/Ni/Au (20 nm/ 120 nm/ 20 nm/ 40 nm) were deposited on the top and bottom n^+-GaN and Pd/Ni/Au (20 nm/ 20 nm/ 200 nm) stacks were deposited on the p^+-GaN. The sample was thermally annealed at 400 ℃ in N_2 for 10 mins to form ohmic contacts on the n^+-GaN and p^+-GaN. The sheet resistance and contact resistance of the p^+-GaN, extracted from circular transfer length method, was 1.7×10^6 Ω/□ and 1.6×10^4 Ω.mm, respectively. Ni/Au (20 nm/200 nm) were then deposited as gate metals. The sheet resistance and contact resistance of buried pGaN are Subsequently, a 300 nm bi-layer SiN_x was deposited using the ICPCVD and PECVD as a passivation layer and followed by the via opening. The device fabrication was completed by the probe pad metal deposition. The schematic diagram of the MOSFET is shown in Fig.2.

Fig. 3 shows a cross-sectional STEM image of the gated trench sidewall of the MOSFET. A sharp interface between the gate oxide and the wet-etched GaN sidewalls is achieved. A slope of ~32^0 on the left-hand side of trench was measured and it was identified as (11-20) a-plane as shown in Fig. 1 (c). On the right-hand side of the trench, a slope of ~58^0 was measured on the top n^+-GaN region which corresponds to the c-plane. However, the sidewall slope changes as the etching proceeds to the p^+-GaN and the n^--GaN layers (with a slope angle of ~ 41^0). This is likely due to: (1) the slow p-GaN etch rate and the slow lateral etch rate of the c-planes on the sidewall and (2) the top n^+-GaN layer has longer KOH exposure time compared with the n^--GaN layer. As a result, the deviation of the sidewall angle is observed. A higher molar concentration of hydroxide-based solution and/or a longer etching time are required to fully reveal the c-plane sidewall on the trench.

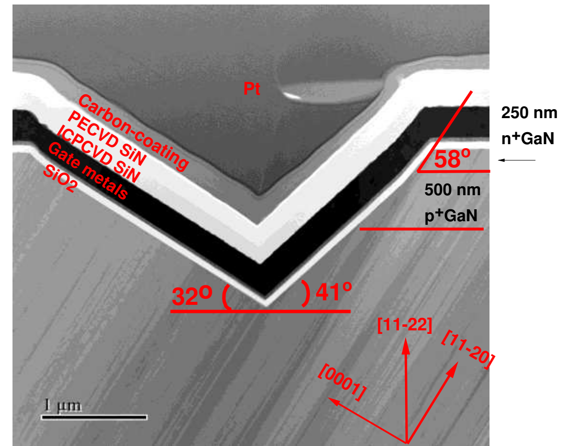

Fig. 3. Cross-sectional scanning transmission electron microscopy (STEM) image of the semi-polar (11-22) GaN VMOSFET.

III. Device Characterization

Fig. 4 demonstrates the gate transfer characteristics of the fabricated VMOSFET with an ON/OFF ratio of 10^7, V_{th} of 9.49 V (V_{th} defined using the linear interpolation method from the peak transconductance), and a peak transconductance of 30.9 S/cm^2. The field-effect mobility extracted is ~21.3 cm^2/(V.s) at V_{ds} = 1 V and V_{gs} = 15 V using Equation (1): [24]

$$I_{ds} = \frac{V_{ds}}{\frac{1}{\frac{W}{L} C_{ox}\mu_{CH}(V_{gs} - I_{ds}R_{GS} - V_{th})} + R_{other}} \quad (1)$$

where W is the gate width of 100 µm and L is the effective gate length, taking into account the sidewall slope, of ½(0.5 µm/sin 32° + 0.5 µm/sin 41°) = 0.852 µm, , C_{ox} is the gate oxide capacitance per unit are, R_{GS} is the source resistance (0.2

mΩ.cm^2), and R_{other} is the total source and drain resistances (2.6 mΩ.cm^2). The extracted mobility value is consistent with other reported mobility values of 20 – 30 cm^2/(V.s) with a similar p-GaN doping concentration (Mg: 1 - 2 ×10^{19} cm^{-3}) [15], [25]. The trench channel mobility can be improved by reducing the p-type doping concentration to reduce impurity scattering or by re-growth of the AlGaN/GaN 2-dimensional electron gas channel on the trench sidewall [18], [22].

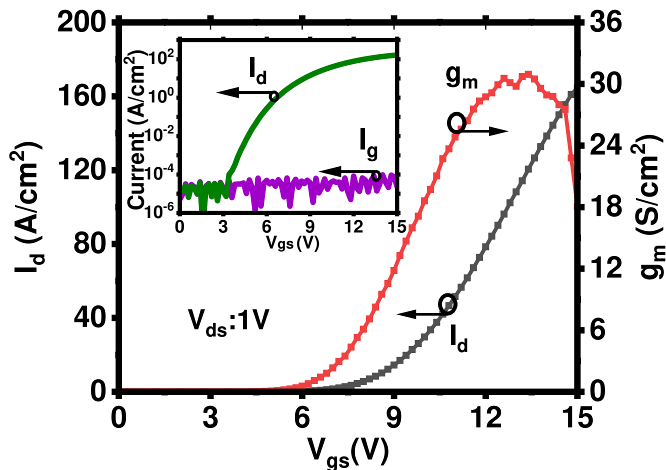

Fig. 4. Gate transfer characteristics of the semi-polar (11-22) GaN VMOSFET.

Fig. 5 shows the I-V characteristics of the VMOSFET with an output current density of 516 A/cm^2 at V_{ds} = 10 V and V_{gs} = 15 V. The extracted specific R_{on} from the linear region of the I-V characteristics was 8.0 mΩ.cm^2. The current density and R_{on} are normalized to the active area of (2.5 µm trench length + 3 µm drift region thickness) × (50 µm trench width + 3 µm drift region thickness) = 291.5 µm^2, taking the drift region current spreading length of 3 µm into account [16], [26]. It is noted that the drain current does not show saturation at higher V_{ds} in the I-V characteristics. It may indicate a low hole concentration in the p-GaN layer which can be the result of a low Mg activation [3]. It can be improved by optimizing the Mg activation in the *p*-GaN such as a higher activation annealing temperature prior to the gate dielectric deposition, increasing *p*-GaN layer thickness (to increase the channel length) and reducing n-GaN drift region doping concentration.

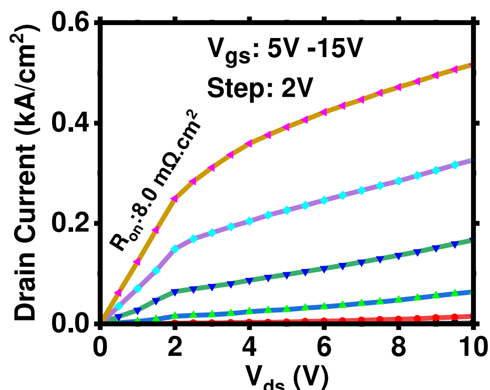

Fig. 5. I-V characteristics of the semi-polar (11-22) GaN VMOSFET.

Fig. 6 shows the 3-terminal off-state characteristics (V_{gs} = 0 V) of the VMOSFET with a gate breakdown of 150 V. The sharp corner at the bottom of the trench could lead to the electric crowding effect at the gate, introducing a thick bottom dielectric [16] or a trench filling regrowth method [27] to flatten the sharp corner could help to alleviate this issue. It is noted that the leakage between the source and drain terminals dominates the off-state leakage current. Fig. 7 shows the vertical leakage measurements of 2-terminal circular $p^+/n^-/n^+$ (0.5 µm/ 3 µm/ 0.5 µm) GaN structure (without the trench opening) with varying diameters. The leakage current is found to scale with device area, suggesting that the device leakage current is dominated by vertical leakage through the GaN bulk [28], [29]. Further improvement in the semi-polar GaN material quality as well as optimization on the *p*-GaN activations [30] are required to reduce the off-state leakage current.

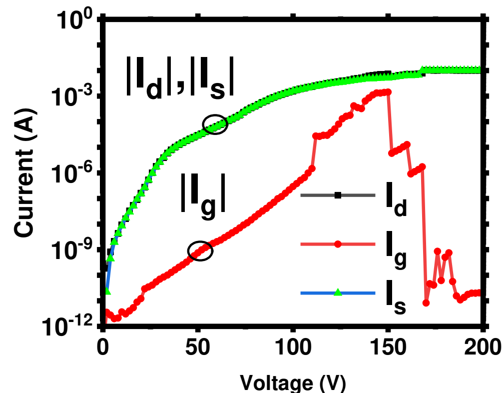

Fig. 6. 3-terminal breakdown characteristics of the semi-polar (11-22) GaN VMOSFET

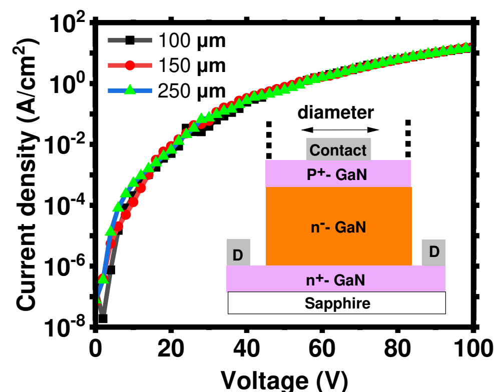

Fig. 7. 2-terminal I-V characteristics of the circular vertical structure.

IV. Conclusion

In summary, fabrication of the enhancement mode semi-polar (11-22) GaN VMOSFET with novel wet etching trench opening method is reported. A threshold voltage of 9.49 V, ON-state resistance of 8.0 mΩ.cm^2 and output current density of 516 A/cm^2 have been achieved on the VMOSFET. The breakdown voltage of the VMOSFET is 150 V. The plasma-etch free trench channel is achieved in the vertical GaN electronic devices using the hydroxide-based wet etching technique. Our wet-etch trench opening technique highlight the potential of plasma etch-free trench formations on the GaN-based electronic devices and is integrate-able with optoelectronics at a semi-polar GaN platform.

REFERENCES

[1] Y. J. Lee, Z. P. Yang, P. G. Chen, Y. A. Hsieh, Y. C. Yao, M. H. Liao, M. H. Lee, M. T. Wang, and J. M. Hwang, "Monolithic integration of GaN-based light-emitting diodes and metal-oxide-semiconductor field-effect transistors," *Opt Express,* vol. 22 Suppl 6, pp. A1589-95, Oct 20 2014, doi: 10.1364/OE.22.0A1589.

[2] X. Lu, S. Yang, H. Jiang, and J. Wu, "Monolithic integration of GaN LEDs with vertical driving MOSFETs by selective area growth and band engineering of the p-AlGaN electron blocking layer though TCAD simulation," *Semiconductor Science and Technology,* vol. 34, no. 6, 2019, doi: 10.1088/1361-6641/ab13e1.

[3] X. Lu, C. Liu, H. Jiang, X. Zou, A. Zhang, and K. M. Lau, "Monolithic integration of enhancement-mode vertical driving transistorson a standard InGaN/GaN light emitting diode structure," *Applied Physics Letters,* vol. 109, no. 5, 2016, doi: 10.1063/1.4960105.

[4] X. Lu, C. Liu, H. Jiang, X. Zou, and K. M. Lau, "High Performance Monolithically Integrated GaN Driving VMOSFET on LED," *IEEE Electron Device Letters,* vol. 38, no. 6, pp. 752-755, 2017, doi: 10.1109/led.2017.2691908.

[5] Z. Guo, C. Hitchcock, R. F. Karlicek, G. Piao, Y. Yano, S. Koseki, T. Tabuchi, K. Matsumoto, M. Bulsara, and T. P. Chow, "Integrable Quasivertical GaN U‐Shaped Trench‐Gate Metal‐Oxide‐Semiconductor Field‐Effect Transistors for Power and Optoelectronic Integrated Circuits," *physica status solidi (a),* vol. 217, no. 7, 2019, doi: 10.1002/pssa.201900615.

[6] Z. Guo, C. Hitchcock, C. Wetzel, R. F. Karlicek, G. Piao, Y. Yano, S. Koseki, T. Tabuchi, K. Matsumoto, M. Bulsara, and T. P. Chow, "Monolithically Integrated GaN LED/Quasi-Vertical Power U-Shaped Trench-Gate MOSFET Pairs Using Selective Epi Removal," *IEEE Electron Device Letters,* vol. 40, no. 11, pp. 1736-1739, 2019, doi: 10.1109/LED.2019.2943911.

[7] M. Hartensveld and J. Zhang, "Monolithic Integration of GaN Nanowire Light-Emitting Diode With Field Effect Transistor," *IEEE Electron Device Letters,* vol. 40, no. 3, pp. 427-430, 2019, doi: 10.1109/led.2019.2895846.

[8] S. Bharadwaj, K. Lee, K. Nomoto, A. Hickman, L. van Deurzen, V. Protasenko, H. Xing, and D. Jena, "Bottom tunnel junction blue light-emitting field-effect transistors," *Applied Physics Letters,* vol. 117, no. 3, 2020, doi: 10.1063/5.0009430.

[9] W. Y. Fu and H. W. Choi, "GaN PNP light-emitting bipolar junction transistor," *Journal of Physics D: Applied Physics,* vol. 55, no. 1, 2021, doi: 10.1088/1361-6463/ac296b.

[10] T. Wang, "Topical Review: Development of overgrown semi-polar GaN for high efficiency green/yellow emission," *Semiconductor Science and Technology,* vol. 31, no. 9, 2016, doi: 10.1088/0268-1242/31/9/093003.

[11] M. Monavarian, A. Rashidi, and D. Feezell, "A Decade of Nonpolar and Semipolar III-Nitrides: A Review of Successes and Challenges," *physica status solidi (a),* 2018, doi: 10.1002/pssa.201800628.

[12] D. A. Stocker, E. F. Schubert, and J. M. Redwing, "Crystallographic wet chemical etching of GaN," *Applied Physics Letters,* vol. 73, no. 18, pp. 2654-2656, 1998, doi: 10.1063/1.122543.

[13] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, "Vertical GaN-Based Trench Gate Metal Oxide Semiconductor Field-Effect Transistors on GaN Bulk Substrates," *Applied Physics Express,* vol. 1, no. 1, 2008, doi: 10.1143/apex.1.011105.

[14] D. Ji, C. Gupta, A. Agarwal, S. H. Chan, C. Lund, W. Li, S. Keller, U. K. Mishra, and S. Chowdhury, "Large-Area In-Situ Oxide, GaN Interlayer-Based Vertical Trench MOSFET (OG-FET)," *IEEE Electron Device Letters,* vol. 39, no. 5, pp. 711-714, 2018, doi: 10.1109/led.2018.2813312.

[15] R. A. Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli, "Fully Vertical GaN-on-Si power MOSFETs," *IEEE Electron Device Letters,* vol. 40, no. 3, pp. 443-446, 2019, doi: 10.1109/led.2019.2894177.

[16] R. Zhu, H. Jiang, C. W. Tang, and K. M. Lau, "Enhancing ON- and OFF-State Performance of Quasi-Vertical GaN Trench MOSFETs on Sapphire With Reduced Interface Charges and a Thick Bottom Dielectric," *IEEE Electron Device Letters,* vol. 43, no. 3, pp. 346-349, 2022, doi: 10.1109/led.2022.3146276.

[17] Y. Zhang, M. Sun, J. Perozek, Z. Liu, A. Zubair, D. Piedra, N. Chowdhury, X. Gao, K. Shepard, and T. Palacios, "Large Area 1.2 kV GaN Vertical Power FinFETs with a Record Switching Figure-of-Merit," *IEEE Electron Device Letters,* pp. 1-1, 2018, doi: 10.1109/led.2018.2880306.

[18] D. Shibata, R. Kajitani, M. Ogawa, K. Tanaka, S. Tamura, T. Hatsuda, M. Ishida, and T. Ueda, "1.7 kV/1.0 mΩcm^2 normally-off vertical GaN transistor on GaN substrate with regrown p-GaN/AlGaN/GaN semipolar gate structure," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 3-7 Dec. 2016 2016, pp. 10.1.1-10.1.4, doi: 10.1109/IEDM.2016.7838385.

[19] Y. Zhao, H. Fu, G. T. Wang, and S. Nakamura, "Toward ultimate efficiency: progress and prospects on planar and 3D nanostructured nonpolar and semipolar InGaN light-emitting diodes," *Adv. Opt. Photon.,* vol. 10, no. 1, pp. 246-308, 2018/03/31 2018, doi: 10.1364/AOP.10.000246.

[20] K. H. Baik, H.-Y. Song, S.-M. Hwang, Y. Jung, J. Ahn, and J. Kim, "Etched Surface Morphology of Heteroepitaxial Nonpolar (11-20) and Semipolar (11-22) GaN Films by Photoenhanced Chemical Wet Etching," *Journal of The Electrochemical Society,* vol. 158, no. 4, pp. D196-D199, 2011, doi: 10.1149/1.3544916.

[21] S. Jung, K. R. Song, S. N. Lee, and H. Kim, "Wet chemical etching of semipolar GaN planes to obtain brighter and cost-competitive light emitters," *Adv Mater,* vol. 25, no. 32, pp. 4470-6, Aug 27 2013, doi: 10.1002/adma.201301640.

[22] H. Qian, K. B. Lee, S. H. Vajargah, S. V. Novikov, I. Guiney, Z. H. Zaidi, S. Jiang, D. J. Wallis, C. T. Foxon, C. J. Humphreys, and P. A. Houston, "Novel GaN-based vertical heterostructure field effect transistor structures using crystallographic KOH etching and overgrowth," *Journal of Crystal Growth,* vol. 459, pp. 185-188, 2017, doi: 10.1016/j.jcrysgro.2016.12.025.

[23] J. Park and S. N. Lee, "Dopant-dependent chemical wet etching phenomena of semipolar (11–22) GaN film," in *2015 11th Conference on Lasers and Electro-Optics Pacific Rim (CLEO-PR)*, 24-28 Aug. 2015 2015, vol. 2, pp. 1-2, doi: 10.1109/CLEOPR.2015.7376080.

[24] M. Xiao, T. Palacios, and Y. Zhang, "ON-Resistance in Vertical Power FinFETs," *IEEE Transactions on Electron Devices,* vol. 66, no. 9, pp. 3903-3909, 2019, doi: 10.1109/ted.2019.2928825.

[25] R. Zhu, H. Jiang, C. W. Tang, and K. M. Lau, "Effects of p-GaN Body Doping Concentration on the ON-State Performance of Vertical GaN Trench MOSFETs," *IEEE Electron Device Letters,* vol. 42, no. 7, pp. 970-973, 2021, doi: 10.1109/led.2021.3080260.

[26] C. Gupta, C. Lund, S. H. Chan, A. Agarwal, J. Liu, Y. Enatsu, S. Keller, and U. K. Mishra, "In Situ Oxide, GaN Interlayer-Based Vertical Trench MOSFET (OG-FET) on Bulk GaN substrates," *IEEE Electron Device Letters,* vol. 38, no. 3, pp. 353-355, 2017, doi: 10.1109/led.2017.2649599.

[27] J.-P. Scholz, C. Chen, and F. Scholz, "Optimisation of trench filling in GaN towards vertical HEMT structures," *Journal of Crystal Growth,* vol. 587, 2022, doi: 10.1016/j.jcrysgro.2022.126629.

[28] C. Liu, R. Abdul Khadar, and E. Matioli, "GaN-on-Si Quasi-Vertical Power MOSFETs," *IEEE Electron Device Letters,* vol. 39, no. 1, pp. 71-74, 2018, doi: 10.1109/led.2017.2779445.

[29] Y. Zhang, H. Y. Wong, M. Sun, S. Joglekar, L. Yu, N. A. Braga, R. V. Mickevicius, and T. Palacios, "Design space and origin of off-state leakage in GaN vertical power diodes," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 7-9 Dec. 2015 2015, pp. 35.1.1-35.1.4, doi: 10.1109/IEDM.2015.7409830.

[30] W. Li, K. Nomoto, K. Lee, S. M. Islam, Z. Hu, M. Zhu, X. Gao, J. Xie, M. Pilla, D. Jena, and H. G. Xing, "Activation of buried p-GaN in MOCVD-regrown vertical structures," *Applied Physics Letters,* vol. 113, no. 6, 2018, doi: 10.1063/1.5041879.