



Deposited via The University of Sheffield.

White Rose Research Online URL for this paper:

<https://eprints.whiterose.ac.uk/id/eprint/189943/>

Version: Published Version

Article:

Ball, E.A. (2022) Predicting the performance of a 26 GHz transconductance modulated downconversion mixer as a function of LO drive and DC bias. *Electronics*, 11 (16). 2516.

<https://doi.org/10.3390/electronics11162516>

Reuse

This article is distributed under the terms of the Creative Commons Attribution (CC BY) licence. This licence allows you to distribute, remix, tweak, and build upon the work, even commercially, as long as you credit the authors for the original work. More information and the full terms of the licence here:

<https://creativecommons.org/licenses/>

Takedown

If you consider content in White Rose Research Online to be in breach of UK law, please notify us by emailing eprints@whiterose.ac.uk including the URL of the record and the reason for the withdrawal request.

Article

Predicting the Performance of a 26 GHz Transconductance Modulated Downconversion Mixer as a Function of LO Drive and DC Bias

Edward A. Ball

Department of Electronic & Electrical Engineering, The University of Sheffield, Sheffield S1 3JD, UK; e.a.ball@sheffield.ac.uk

Abstract: The dependency of RF performance on the local oscillator (LO) drive amplitude and DC bias is an important topic for RF mixers, especially as carrier frequency increases and generation of RF power thus becomes more complex. The prediction of mixer performance, without initial reliance on full circuit simulations, can provide important insights. In this work, mathematical models without the prior use of circuit simulation are developed, leading to a strategy to predict the conversion gain (Gc), DC current, 1 dB input compression point (IP1dB) and third order input intercept point (IIP3) for a SiGe bipolar transistor transconductance mixer. The models show the possibility to trade-off LO RF power and DC bias to achieve a desired performance. The concepts allow a prediction of the necessary DC bias required to support a chosen LO level and desired conversion transconductance or linearity. The mathematical model results, circuit simulation results, and measured hardware results from a 26 GHz prototype of a single-ended mixer are presented and compared, showing good agreement. In a lab-measured example, LO power reduction from +10 dBm to +3 dBm resulted in only a 1 dB reduction in conversion gain, by modifying the DC bias as predicted. The peak conversion gain predicted by the models is within 2.0 dB of circuit simulation and 2.5 dB of measured PCB results. The RMS error for predicted DC current, compared to circuit simulation, is 1.9 mA or better.

Keywords: RF; conversion gain; linearity; mixer design; bipolar transistor circuits; simulation

Citation: Ball, E.A. Predicting the Performance of a 26 GHz Transconductance Modulated Downconversion Mixer as a Function of LO Drive and DC Bias. *Electronics* **2022**, *11*, 2516. <https://doi.org/10.3390/electronics11162516>

Academic Editors: Heng-Tung Hsu, Jeng-Han Tsai and Kuniyuki Kakushima.

Received: 6 July 2022

Accepted: 9 August 2022

Published: 11 August 2022

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Copyright: © 2022 by the author. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

The millimeter wave (mmWave) 5G bands at n258 (26 GHz) and n257 (28 GHz) are examples of the increasing adoption of mmWave frequencies for 5G and future 6G wireless communications [1]. A particular focus for mmWave systems is massive MIMO [2] which will require a multiplicity of low power RF hardware solutions at each antenna element. However, the operation of radios in the mmWave bands still requires power efficient and cost-effective RF circuit techniques to realize practical radio systems.

Whilst RF mixers can be designed and performance accurately predicted using CAD tools from the outset, this can lead to a loss of understanding of what affects the mixer performance. This is where mathematical models for circuit operation become valuable and allow fundamental insights into why particular effects or performance is seen.

Most mixer design strategies nowadays focus on FETs, due to their use in MMICs and CMOS designs. Such designs are well documented, with many published recent examples in CMOS at 28 GHz [3] and for 5G FR2 [4], 2.4 GHz [5], and increasingly at 60 GHz [6].

It is well known that the local oscillator (LO) drive power used for a frequency mixer can affect its gain, linearity and noise figure (NF). However, the generation of significant LO power at mmWave frequencies is today still complex, costly, and DC power

inefficient. There is continued research interest in using simple, novel, and power-efficient RF architectures at mmWave, because of the generally higher DC bias currents and device costs as operational frequencies increase.

1.1. Paper Motivation

Development of mathematical models to allow the RF performance of a mmWave single-ended bipolar junction transistor (BJT) mixer design to be investigated, based on a known transistor, without the initial use of a circuit simulator. Existing published literature has focused extensively on FET mixers, with less recent attention on BJT mixers. This paper investigates the viability of trading LO RF power with DC bias in an SiGe NPN RF BJT transconductance modulated mixer, significantly expanding and improving the models and measurements developed in [7]. Mathematical models to predict the IF current generated by the mixing operation within the transistor are developed, leading to a prediction of the conversion transconductance (g_{m_c}) and conversion gain (G_c), 1 dB input compression point (IP1dB) and third order input intercept point (IIP3). The concepts are demonstrated using a commercial SiGe BJT.

Prediction of required DC bias for given LO power. A model is created for predicting the required DC base bias (V_b) to achieve a desired conversion transconductance with a chosen LO power, to allow the trading of RF performance in a predictable way. The concept can also be used to predictably control the conversion gain by adjusting V_b . Conventional mixer design approaches tend to set the DC bias and optimize the LO power for the best RF performance [8–10]. To the author's best knowledge, the mathematical prediction of RF mixer performance by jointly selecting LO power and V_b has not been extensively explored previously, particularly relating to SiGe BJTs, although empirical relationship results have been observed and reported, for example [11].

Investigation into the use of low-cost commercial BJT in mmWave downconverting mixer. Although the focus of this paper is on the performance prediction of a single transistor downconversion mixer at 26 GHz, a hardware prototype was created using a commercial packaged transistor. This useful prototype has facilitated lab testing.

1.2. Background

Most recent literature for downconversion transistor-based mixer analysis and design are focused on CMOS, mainly using the Gilbert Cell architecture, (for example [12] at 24 GHz), though these can have poor performance at mmWave frequencies [13]. The related circuit analytical design often focuses on noise reduction techniques, with examples at 3.1 GHz [14] and 5G 27.5 GHz–43.5 GHz [15]. Linearity improvement techniques are also popular research topics for CMOS, such as for IIP3 in 802.15.4 at 2.4 GHz [16] or for second order input intercept point (IIP2) improvement [17]. Published works tend rely on subsequent circuit simulation for validation of trialed design techniques.

Single device (i.e., single-ended) downconverting mixers using GaAs transistors have been widely reported, for example [18] demonstrating a 6–26 GHz mixer requiring 13 dBm LO and [19] demonstrating a 5–30 GHz mixer requiring 15 dBm LO. However, SiGe devices can generally operate at lower bias current than GaAs and are readily available as discrete surface mount devices.

Only a few prior works fully develop and consider mixers with first-principles analysis techniques, such as for IIP2 and DC offset control [20], FET modelling [21], MOSFET modelling (100 MHz–1.5 GHz) [22]—generally all at carrier frequencies below 6 GHz. Where LO waveforms at the drain or collector are considered, standard models of clipped sinusoids are relied on, such as for 5G 24 GHz–40 GHz [23], leading to transconductance mixer models. For Gilbert Cell mixers, a hard switching waveform is assumed for commutation, such in WLAN 2.4 GHz [24]. However, the Gilbert Cell architecture is more complex than the mixer used in this paper, requiring three or more active devices.

Very few reported works compare the mathematical model results jointly to *both* circuit simulation *and* to a built prototype (3 steps), which makes it hard to assess the relative

accuracies of approaches. They instead commonly focus on only comparisons between CAD simulation and lab measurements.

The mixer collector current is often modelled as a Taylor series in device transconductance, such as at 2.4 GHz [25], 1.7 GHz [26], 500 MHz–3.1 GHz [14] and this is the approach also taken in this paper for linearity analysis.

SiGe is an important semiconductor material for future mmWave communications systems due to its high performance and suitability for system integration [27–29]. Examples of its relevance to mixers are demonstrated in [30] for a 40 GHz mixer with 2 dBm LO drive. However, there are few recent works that consider BJT mixer design and analysis, even though this is relevant to SiGe BiCMOS at mmWave frequencies. This is because most mmWave designs have traditionally use GaAs PHEMTs or more recently CMOS (both using FET based models). Reported SiGe mixer designs are usually part of a larger integration, such as a front-end chip, with examples at 28 GHz for a phased array [31], IIP2 calibration techniques for 900 MHz WCDMA [32], 5G 26 GHz & 28 GHz receiver [33] and at 2 GHz [34]. However, the applicability of SiGe for higher mmWave operation is beginning to be reported in mixers, such as for 60 GHz ISM [35], a 0 dBm LO drive mixer at 60 GHz [36], and [37] presenting a 60 GHz Gilbert Cell with 3 dBm LO drive.

A design strategy for a single balanced BJT mixer in IC is provided in [38], though this uses 3 transistors. Also, like many Gilbert Cell designs, it also assumes the upper transistors act as switches with a 50% duty cycle. This is a simplification not used in this paper for the LO current model, with the whole waveform considered.

Reported results that compare modern CAD mixer circuit simulation to measured data at mmWave often show very good accuracies, often with circa 1 dB error for conversion gain, e.g.,: 77 GHz & 94 GHz mixer [39], 60 GHz [40], 5G 28 GHz [41], WIMAX [42], 5G 24 GHz–30 GHz [43], 26 GHz–40 GHz [44], though with up to 5 dB error for some designs [45]. Circa 3 dB simulator-referenced prediction errors for NF are reported, e.g., 77 GHz & 94 GHz [39], 5G 24 GHz–40 GHz [45] and 5G 28 GHz [41]. Fewer lab measurement to simulation comparisons of linearity have been published. However, [43] demonstrates IP1dB linearity measurements for a SiGe BiCMOS 5G 24 GHz–30 GHz mixer with LO operating at 20 GHz, which differs from simulations by circa 1dB.

A rare example that compares a calculated 950 MHz mixer conversion gain to measurements is reported in [46], showing a 1.5 dB overestimate from the calculation.

In general in the literature, mathematical models are used in the initial design process for selecting circuit values, with the CAD simulator then used to validate the design. The errors between models or simulations and measurements are often considered minor if circa 1 dB. However, the key requirements for a mixer (G_c , NF, IIP3) all have a great impact on the overall system performance. A difference of 1–3 dB can be significant for these parameters, hence the importance of model accuracy and a good understanding of the causes for performance, which theoretical models can provide.

1.3. Paper Contribution & Structure

The contributions of this paper are as follows: (1) new mathematical design models for predicting RF mixer IF and DC currents and hence G_c , considering both the base LO drive A_L and DC base bias V_b without circuit simulation. (2) Models for predicting the IP1dB and IIP3 levels due to A_L and V_b . (3) A model to guide the selection of base bias V_b , given a defined LO amplitude A_L and desired conversion transconductance g_{m_c} . (4) Comparison and validation of the modelling approach to conventional circuit time-domain simulation and a measured hardware prototype single-ended 26 GHz mixer.

The paper is organized as follows: in Section 2, the models for the collector current are introduced and in Section 3, mathematical models for the IF current are developed. The hardware test prototype is introduced in Section 4. In Section 5, the mathematical models are compared to circuit simulation results and hardware lab trials. Section 6 concludes the paper.

2. Transistor Collector Current Mathematical Models

To facilitate a practical analysis, a commercial transistor was selected as the basis of the investigation and the resulting mixer design. The SiGe transistor BFP740FH6 from Infineon Ltd. was selected, with a transition frequency (F_T) of 45 GHz. The first step in modeling the mixer operation is to create a representative collector current model. This requires an understanding of the device I-V characteristics at DC and at the center frequency of the LO. For the proposed mixer, an LO of 21 GHz was used. The conceptual representation of this initial test circuit for time-domain simulation is shown in Figure 1a. To allow a fully mathematical model to be created, a circuit model for the transistor's basic operation was developed, as shown in Figure 1b, based on the Gummel Poon (GP) model [47].

The total collector current (combined AC and DC currents) caused by the base-emitter voltage, is represented by I_o . I_o can thus represent $I_{bm} = I_o(V_b)$ due to DC base bias V_b , or $I_{pk} = I_o(A_L + V_b)$ due to the combined base AC LO signal and DC bias. The parameters of the GP model were obtained directly from vendor's data sheets. All components shown in Figure 1b must be included to capture the AC and DC operation of the transistor.

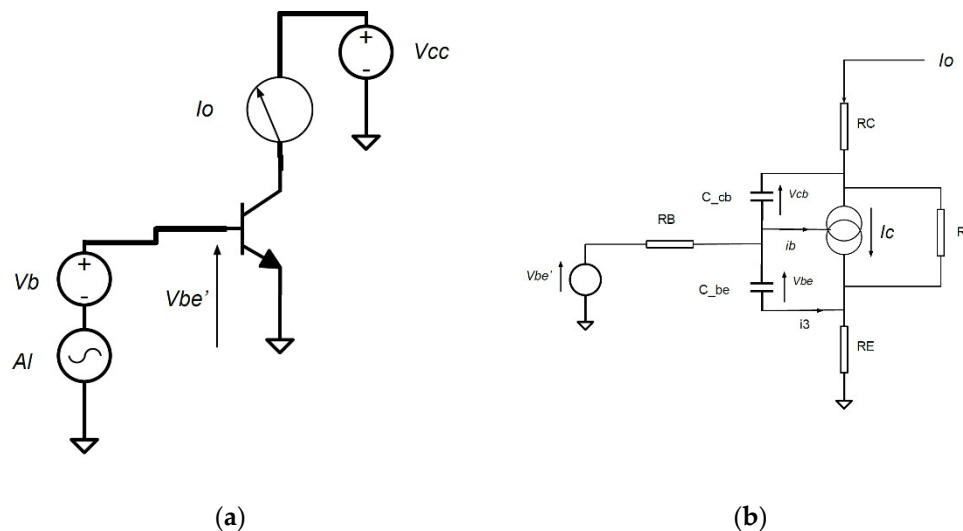


Figure 1. BJT model used: (a) Initial simulation circuit to extract I_o vs V_b and A_L ; (b) Mathematical model for transistor operation, using Gummel Poon BJT parameters.

The next step in building the mathematical model is to represent the relationship for I_o at the LO as a function of an externally applied total voltage V_{be}' , applied between the external base and emitter BJT pins. (Note: term V_{be} is the total voltage seen between the internal base-emitter junction). V_{be} can be related to V_{be}' using conventional circuit analysis techniques. I_o is determined via mathematical circuit analysis and the GP BJT model, relating V_{be}' to V_{be} and I_o . The BJT internal collector current I_c is related to V_{be} using Equation (1). In Equations (1)–(7), all terms are standard GP parameters, with values obtained from the BJT vendor's data sheet model.

$$I_c \approx \frac{I_s}{NqB} \left(e^{\left[\frac{V_{be}}{NF \times V_T} \right]} - 1 \right) \quad (1)$$

The GP term NqB of Equation (2) is important for capturing the effects of current reduction due to DC bias and the LO AC drive.

$$NqB = \frac{q_{1s}}{2} \left(1 + \sqrt{1 + 4q_{2s}} \right) \quad (2)$$

The GP parameters q_{1s} in Equation (3) represents the base-width modulation and q_{2s} in Equation (4) represents high-level injection effects (including Kirk effect approximation).

$$q_{1s} = \frac{1}{1 - \frac{V_{be}}{VAR} - \frac{V_{bc}}{VAF}} \quad (3)$$

$$q_{2s} = \frac{I_s}{IKF} \left(e^{\left[\frac{V_{be}}{NF \times V_T} \right]} - 1 \right) + \frac{I_s}{IKR} \left(e^{\left[\frac{V_{bc}}{NR \times V_T} \right]} - 1 \right) \quad (4)$$

The GP internal capacitors C_{be} of Equation (5) and C_{bc} of Equation (6) are also crucial in capturing the AC effects of the resulting collector current.

$$C_{be} = \frac{CJE}{\left(1 - \frac{V_{be}}{VJE}\right)^{MJE}} + \frac{TFF \times I_s}{NF \times V_T \times NqB} e^{\left[\frac{V_{be}}{NF \times V_T} \right]} \quad (5)$$

$$C_{bc} = \frac{CJC}{\left(1 - \frac{V_{bc}}{VJC}\right)^{MJC}} + \frac{TR \times I_s}{NR \times V_T \times NqB} e^{\left[\frac{V_{bc}}{NR \times V_T} \right]} \quad (6)$$

The GP parameter TFF represents the transit time and is defined by Equation (7).

$$TFF = TF \left(1 + XTF \left[\frac{I_c}{I_c + ITF} \right]^2 e^{\left[\frac{V_{bc}}{1.44VTF} \right]} \right) \quad (7)$$

Parameters C_{bc} , C_{be} , and NqB all have the effect of reducing the collector current achieved for a given V_{be} for AC signals, leading to differing performance at AC and DC. The GP parameters used in the model for the BFP740F are listed in Table 1.

Table 1. Gummel Poon Model Parameters for BFP740F.

BJT Model Parameter	Value	Unit	Description
I_s	1.249×10^{-15}	A	Transport saturation current
NF	1.002	-	Forward current emission coefficient
NR	1.01	-	Reverse current emission coefficient
V_T	25.9	mV	kT/q (25.9mV at 300K)
VAR	1.229	V	Reverse Early voltage
VAF	380.1	V	Forward Early voltage
IKF	0.1898	A	Forward Beta high current roll-off
IKR	0.02753	A	Reverse Beta high current roll-off
CJE	0.2531	pF	Base-emitter zero-bias depletion cap
VJE	0.9286	V	Base-emitter built-in potential
MJE	0.06125	-	Base-emitter junction exponential factor
TF	2.331	pS	Ideal forward transit time
XTF	1.159	-	TF bias dependence coefficient
ITF	0.3991	A	TF high current parameter
VTF	0.5242	V	TF dependency on V_{bc}
CJC	54.52	fF	Base-collector zero-bias depletion cap
VJC	0.4808	V	Base-collector built-in potential
MJC	0.5812	-	Base-collector junction exponential factor
TR	1.532	nS	Ideal reverse transit time
RC	4.1	Ohm	Internal collector resistance
RE	0.18	Ohm	Internal emitter resistance
RB	7.0	Ohm	Zero bias internal base resistance
Ro	VAF/I_c	Ohm	Output resistance
BF	987.1	-	Forward max Beta

Figure 2 shows the equivalent AC comparison of the mathematical model compared to a Keysight ADS simulation as per Figure 1, showing a good fit over most of the range of interest for A_L and V_b and so confirming the viability of the approach. This means the

collector current due to LO can be accurately predicted and includes DC and AC effects, without CAD circuit simulation. It will be seen later that the LO waveform is vital to accurate mixer modelling. Figure 2 also shows the root mean square error (RMSE) between the ADS simulation and the model.

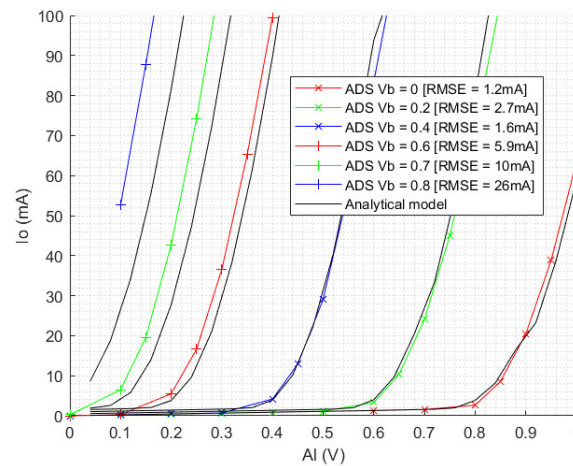


Figure 2. Comparison of peak AC I_o vs. A_L for test ADS circuit simulation and GP mathematical model, showing good agreement.

In general, let the applied external (base-emitter) voltage V_{be}' consists of three components: a base DC bias V_b , the LO signal of form $A_L \cos(\omega_L t)$ and the incoming RF signal $A_R \cos(\omega_R t)$, combined for analysis as represented in Equation (8).

$$V_{be}' = V_b + A_L \cos(\omega_L t) + A_R \cos(\omega_R t) \quad (8)$$

3. IF Current Mathematical Models

The prediction of the IF transconductance mixer current produced by the nonlinear action of the transistor is central to the calculations in this paper. This knowledge allows the proper and full consideration of base LO amplitude A_L and base DC bias V_b on the creation of the IF current to be explored, supporting predictions of conversion transconductance g_{m_c} and IP1dB, etc. The mixer model uses the peak collector current $I_o(A_L + V_b)$ and DC current $I_o(V_b)$ obtained using the device circuit mathematical model for the transistor described in Section 2. These current amplitudes are then applied to subsequent time-domain mathematical models representing the mixer action—this being more suitable for subsequent simple mathematical manipulation.

3.1. LO Currents

A conceptually valuable and well-known approach to modeling the operation of a transconductance mixer starts with the simple assumption that the collector current due to the LO produces a clipped sinusoidal waveform [48,49], as shown in Figure 3. I_{pk} is found using the model Equations (1)–(8) for $I_o(A_L + V_b)$, providing the peak collector current due to the combined effect of base DC bias V_b and the AC LO signal A_L , as applied to the external base-emitter. A simple time-domain sinusoidal current model, defined as $i(t) = I_{bm} + (I_{pk} - I_{bm})\cos(\theta)$ is then used for subsequent mixer modeling, where θ is the phase of the LO in the cycle, I_{pk} is the peak collector current, and I_{bm} is the DC current due to V_b . Note that for all practical BJTs, there will be negligible current flowing in the period T_1 to $T_p - T_1$ because the collector will be off—hence the use of a clipped sinusoid model.

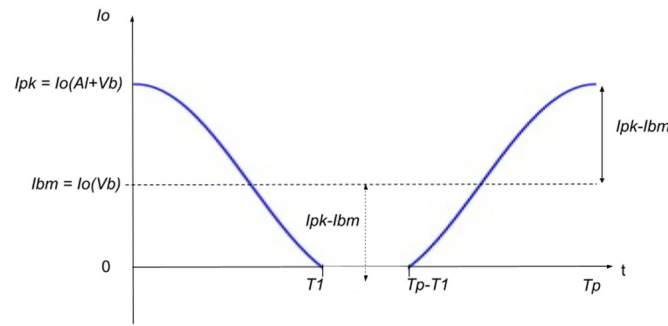


Figure 3. BJT collector LO current I_o approximated by $I_{bm} + I_o(AL + V_b)\cos(\theta)$.

From Figure 3, parameter T_p is the period of the LO cycle and T_1 is the time, as measured from the start of the waveform, where the collector current has fallen to a negligible value (i.e., transistor V_{be}' below knee). However, it has been found that as V_b is reduced and A_L increased significantly, the collector current waveform is better modeled by $(I_{pk} - I_{bm})\cos(2\theta)$. Between these states, transitional definitions are required, allowing the collector current time-domain model to better represent the actual transistor current waveform. The time-domain representation of this new fitting can be defined by Equations (9)–(11) which incorporates parameter k , which can vary from 1.0–2.0 thus representing $(I_{pk} - I_{bm})\cos(k\theta)$.

$$I_{Tk} = I_{bm} + (I_{pk} - I_{bm}) \cos\left(\frac{2k\pi t}{T_p}\right), \text{ for } t = 0..T_1 \tag{9}$$

$$I_{Tk} = I_{bm} + (I_{pk} - I_{bm}) \cos\left(2\pi[1 - k] + \frac{2k\pi t}{T_p}\right), \text{ for } t = T_p - T_1..T_p \tag{10}$$

$$I_{Tk} = 0, \text{ for } t = T_1..T_p - T_1 \tag{11}$$

The Fourier coefficient for the resulting first harmonic C_1 current is then represented by Equation (12) and Equation (13) for DC C_0 . Equation (12) defines C_{1k} when k is not equal to 1; when k equals 1 Equation (14) should be used.

$$C_{1k} = \frac{2I_{bm}}{\pi} \sin\left(\frac{2\pi T_1}{T_p}\right) + \frac{(I_{pk} - I_{bm})}{\pi} \left\{ \frac{\sin\left[\frac{2\pi T_1(k+1)}{T_p}\right]}{k+1} + \frac{\sin\left[\frac{2\pi T_1(k-1)}{T_p}\right]}{k-1} \right\} \tag{12}$$

$$C_{0k} = \frac{2I_{bm}T_1}{T_p} + \frac{(I_{pk} - I_{bm})}{k\pi} \left[\sin\left(\frac{2k\pi T_1}{T_p}\right) \right] \tag{13}$$

$$C_{11} = \frac{2I_{bm}}{\pi} \sin\left(\frac{2\pi T_1}{T_p}\right) + \frac{2(I_{pk} - I_{bm})T_1}{T_p} + \frac{(I_{pk} - I_{bm})}{2\pi} \left[\sin\left(\frac{4\pi T_1}{T_p}\right) \right] \tag{14}$$

Parameter T_1 can be defined by the simple geometry of the collector current waveform or the applied base voltage waveform V_{be}' . Considering Equation (8) and ignoring the negligible contribution from A_R , the point where V_{be}' intercepts BJT DC knee voltage V_{tt} (circa 0.75 V) can be used to define T_1 , using Equation (15). Although V_{tt} can be hard to predict in a real device, for the purposes of the simple model here it can be predicted as required from Equation (1).

$$T_1 = \frac{T_p}{2\pi} \arccos\left(\frac{V_{tt} - V_b}{A_L}\right) \tag{15}$$

The equivalent steady-state DC current I_{bm} , the middle of the collector current amplitude cycle in Figure 3, is determined from Equation (1) by considering only V_b , without an AC A_L signal applied. The value of k for a particular time T_1 and T_p is determined using

Equation (16), where m and f are linear parameters for a straight-line approximation, dependent only on Vb .

$$k = Vb \times m + f \quad (16)$$

The values for m and f are found via time domain comparison over one LO period, using BJT instantaneous current I_o using Equations (1)–(8) when compared to Equation (9) and Equation (10) over the Vb and A_L ranges of interest. They do not require circuit simulation and only need evaluating once for a design. The BFP740F extracted values are $m = -1.75 \text{ V}^{-1}$ and $f = 2.6$.

3.2. Relating A_L to Required Port LO Power

The mathematical models are driven by the LO amplitude A_L and DC bias Vb , both applied directly at the base. In practice, the LO power will be applied to a port away from the transistor, passing through various LO/RF combining networks and RF matching, before reaching the base. An approximation of the actual LO power required at the port can be calculated using the following steps:-

1. Select a target A_L and Vb and let the mathematical model Equation (13) produce the resulting equivalent DC current draw C_{ok} .
2. Use C_{ok} and the BJT small-signal S parameters to estimate the base input reflection coefficient Γ_i Equation (17), with Γ_L set to -1 , representing a collector short circuit to ground at the LO, as required for good mixer operation.

$$\Gamma_i(C_{ok}) = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \quad (17)$$

Then, convert from Γ_i to the equivalent base input impedance $Z_i(C_{ok})$ and then to the equivalent base shunt input resistance R_p .

1. Use A_L as applied to R_p to calculate the RF LO power LOP_b , as would be seen at the base.
2. Translate the power LOP_b back to the connector port, accounting for any expected intermediate RF stage insertion losses, due to combiners, etc.

The above approach has been used in this study and shows good agreement with Keysight ADS simulations for A_L vs. applied port LO power.

3.3. Extracting the Transconductance Mixing Current

The C_{1k} Fourier component Equation (12) can be converted to a transconductance at the LO using Equation (18). C_{1k} and A_L are both 'large signals', however they both properly capture the transistor operation in the large signal regime and so (18) is a valid approach for the time varying transconductance due to the LO in the BJT.

$$gm_{LO} = \frac{C_{1k}}{A_L} \quad (18)$$

The product of the LO modulated transconductance, Equation (18), and the RF signal entering the mixer at the carrier, $A_R \cos(\omega_R t)$, will result in an IF current, due to the conversion transconductance. This product of the RF input voltage and the time varying transconductance is fundamental to the mixer's operation [48,50]. The conversion transconductance at one of the resulting sidebands can then be represented by Equation (19).

$$gm_{c,max} = \frac{gm_{LO}}{2} \quad (19)$$

Note that gm_c is a function of both A_L and I_{pk} (itself a function of A_L and Vb) and as such the transistor is not operating in a class-A linear bias due solely to Vb .

The resulting IF current is then the product of Equation (19) and the applied RF voltage A_R . The resulting DC current C_{ok} may result in the BJT's effective input and output match changing from the initial design target (used to create the matching networks).

Therefore, the BJT input and output match change, due to a change in the effective bias, must be considered when evaluating the resulting conversion gain. A simple strategy for this is to consider the effect of the impedance change at the base (RF) and collector (IF) and represent it as a reduction in effective conversion gain, with respect to the target design value, which would usually be a conjugate match. This effect is incorporated into the model using Equation (20), Equation (21) and Equation (22).

$$gm_c = gm_{c_max} \times M_B(C_{0k}) \times M_C(C_{0k}) \quad (20)$$

$$M_B(C_{0k}) = \frac{R_b(C_{0k})}{\sqrt{(R_b\ target + R_b(C_{0k}))^2 + (X_b\ target + X_b(C_{0k}))^2}} \quad (21)$$

$$M_C(C_{0k}) = \frac{R_c\ target}{\sqrt{(R_c\ target + R_c(C_{0k}))^2 + (X_c\ target + X_c(C_{0k}))^2}} \quad (22)$$

Parameter R_b is the real part of the base impedance, X_b is the imaginary part and with the *target* assumed to be the conjugate of the base impedance at the target design DC current. Similarly, parameter R_c is the real part of the collector impedance, X_c is the imaginary part, and the *target* is collector conjugate impedance at the DC operating target.

3.4. IP1dB & IIP3 Prediction Models

The IP1dB for the mixer can be predicted as a function of A_L and V_b , using the LO currents for the fundamental (C_{1k}) and third harmonic (C_{3k}) and then relating them, as will now be introduced. A conventional approach is to define the IF current using derivatives of the conversion transconductance using a Taylor series [51,52], represented at the IF frequency by Equation (23). This model assumes there are no memory effects present.

$$I_{c_{IF}} = I_{c_0} + A r \times gm_1 + A r^2 \times gm_2 + A r^3 \times gm_3 + \dots \quad (23)$$

where, conversion transconductance $gm_1 = \frac{d(I_{c_{LO}})}{d(V_{AL})}$, $gm_2 = \frac{d^2(I_{c_{LO}})}{d(V_{AL})^2}$, $gm_3 = \frac{d^3(I_{c_{LO}})}{d(V_{AL})^3}$ are evaluated from the collector current due to the LO. Once the conversion transconductances are known, the IP1dB Equation (24) and IIP3 Equation (25) can be obtained directly for the equivalent base RF voltages.

$$A_{R_{IP1dB}} = \sqrt{\frac{gm_1}{gm_3} \left(10^{\left[\frac{-1}{20}\right]} - 1 \right)} \quad (24)$$

$$A_{R_{IIP3}} = \sqrt{\frac{gm_1^4}{gm_3^3}} \quad (25)$$

A technique will now be introduced that relates the magnitudes of the found Fourier LO harmonics C_{1k} , C_{3k} to the currents that would be produced by a simple Taylor exponential expansion and hence leading to the required gm_1 and gm_3 . The technique starts by defining the IF collector current from only the LO, as passed through the simple BJT AC model Equation (26) and then expanding into a Taylor series using Equation (27).

$$I_{c_{LO}} = I_{DC} \times e^{\frac{A \cos(\omega_{LO})}{V_T}} \quad (26)$$

$$I_{c_{LO}} = 1 + A \cos(\omega_{LO}) + \frac{A^2}{2} \cos^2(\omega_{LO}) + \frac{A^3}{6} \cos^3(\omega_{LO}) + \dots \quad (27)$$

Expanding Equation (27) and collecting terms produces Equation (28).

$$I_{c_{LO}} = \left(1 + \frac{A^2}{4} \right) + \left(A + \frac{3A^3}{24} \right) \cos(\omega_{LO}) + \frac{A^2}{4} \cos(2\omega_{LO}) + \frac{A^3}{24} \cos(3\omega_{LO}) \dots \quad (28)$$

Considering the fundamental LO term means we can immediately state that $C_{1k} = A$ and considering the third harmonic term $C_{3k} = \frac{A^3}{24}$. We can then find parameter A by evaluating the ratio of C_{3k}/C_{1k} , using Equation (29).

$$A = \sqrt{\frac{24C_{3k}}{C_{1k}}} \tag{29}$$

The magnitude of the third-harmonic collector current component C_{3k} can be determined using Equation (30), based on the techniques from Section 3.1.

$$C_{3k} = \frac{2I_{bm}}{3\pi} \sin\left(\frac{6\pi T_1}{T_p}\right) + \frac{(I_{pk} - I_{bm})}{\pi} \left\{ \frac{\sin\left[\frac{2\pi T_1(k+3)}{T_p}\right]}{k+3} + \frac{\sin\left[\frac{2\pi T_1(k-3)}{T_p}\right]}{k-3} \right\} \tag{30}$$

By considering the current generation action of Equation (28), we can now also directly state Equations (31) and (32) to relate the current components in terms of required transconductance.

$$gm_1 A_L = A \tag{31}$$

$$gm_3 A_L^3 = \frac{3A^2}{24} \tag{32}$$

As a penultimate step, the required ratio of gm_1/gm_3 can be found using Equation (33) and Equation (29).

$$\frac{gm_1}{gm_3} = \frac{8A_L^2}{A^2} \tag{33}$$

The base-referred IP1dB equivalent voltage amplitude is then determined by Equation (24). The base RF voltage corresponding to the third order input intercept point can also now be predicted using Equation (25).

3.5. Selecting V_b for a Fixed A_L and Conversion Transconductance

A key aim of the research was to identify the V_b required to support a particular desired conversion transconductance with a defined LO power. To lead to this, the expressions for $k = 1$ and $k = 2$ versions of Equation (12) using Equation (15) were derived. Applying the simplifying approximation of $I_{pk} > I_{bm}$ and $V_b < V_{tt}$ for practical mixers, allows usable simple expressions to emerge. However, in general we will not know early in a design whether to use $k = 1$ or $k = 2$ variants, so for a pragmatic approach an average is used. In addition, knowing that $0 < (V_{tt} - V_b) < A_L$ allows a further simplification. We also know from Equation (18) and Equation (19) that $C_{1k} = 2A_L gm_c$. The above strategy leads to Equation (34) to define a simple relationship between V_b and a given A_L and the desired gm_c . (To further simplify Equation (34) NqB can reasonably be approximated to 1).

$$V_{b_m} = V_T \log_e \left[\frac{2\pi gm_c \times A_L \times NqB}{I_S \left\{ 2 + \left[\frac{\pi + 11}{4} + \frac{11}{12} \right] e^{\left(\frac{A_L}{V_T} \right)} \right\}} \right] \tag{34}$$

It may be tempting to rearrange Equation (34) to obtain gm_c for a given V_b and A_L but this should be avoided. (The applied simplifications would lead to an overestimate of gm_c if used in this way. Accurate prediction of gm_c requires full use of models as described in Sections 3.1–3.3).

Once proposed input and output matching circuits are known, the conversion gain can be predicted and thus converted to a trial gm_c , following the architecture of Figure 4.

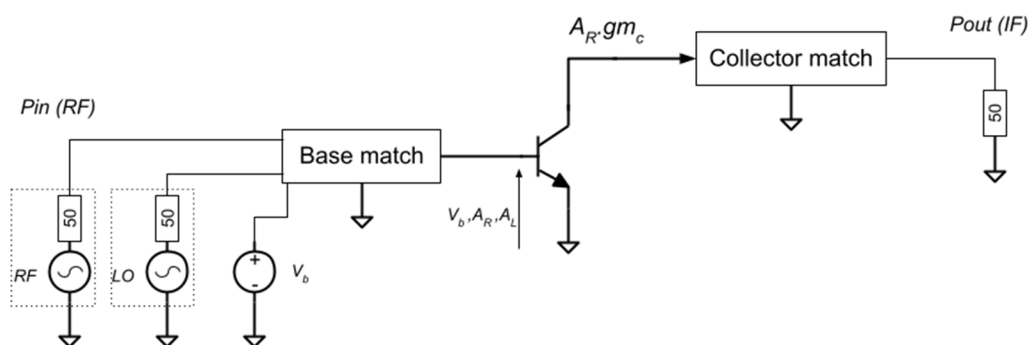


Figure 4. Mixer signal locations.

4. Trial Mixer Hardware for Model Validation

To evaluate the accuracy of the proposed IF current model (and subsequent conversion gain) required a BFP740F mixer prototype. The key requirement to ensure relevance to the mathematical model is that the mixer is base-driven for both the LO and RF signals and the IF current is extracted from the collector. A Keysight ADS circuit and planar EM simulation was created for the single-ended transistor mixer, as shown Figure 5, designed using conventional RF techniques.

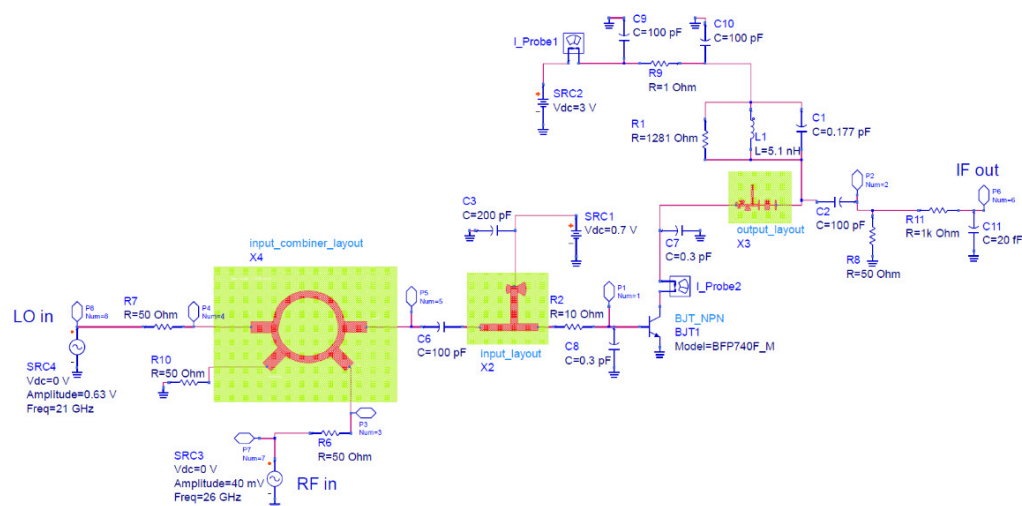


Figure 5. Single-ended 26 GHz mixer schematic.

The mixer LO range was 19–23 GHz and the RF range was 24–28 GHz. Rogers RO4003C substrate was used (0.5 mm thick, ϵ_r of 3.55, loss tangent of 0.0027). The input RF and LO signals are combined using a rat-race and then passed through a base conjugate matching network.

The output matching network is particularly important for transconductance mixers. Figure 6a shows the architecture used, with radial stub short circuits (S/C) at the collector port for the LO fundamental and its second harmonic, followed by an IF matching circuit and low pass filter (LPF). The collector network was biased at 3 V. To fully evaluate the mixer concepts, a 26 GHz PCB prototype was created from the developed ADS design. The assembled single-ended mixer PCB is presented in Figure 6b.

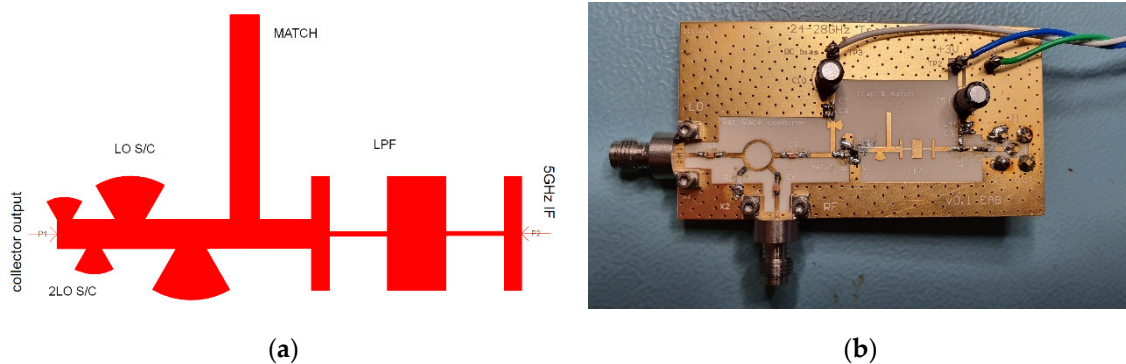


Figure 6. Single-ended 26 GHz mixer: (a) output network; (b) Built PCB (LO port on left and RF port on lower left, IF on right).

5. Comparison between Mathematical Models, Circuit Simulations and Measured PCB

The achievable RF performance and $A_L - V_b$ trade-offs were explored using the PCB prototype mixer with 3 V collector bias. Unless stated, single frequency lab tests used a 21 GHz LO with port LO drive powers of 10, 7, 3 and 0 dBm. Unless stated, the RF signal was set to 26 GHz at -20 dBm, resulting in a 5 GHz IF. The RF signal generator was an Agilent E8247C and the LO signal generator was a Gigatronix 2540B. IF signals were measured using a Rohde & Schwarz FSV40N spectrum analyser.

5.1. Initial Insights from Mathematical Model

The mathematical models based on Equations (1)–(22) were first used to explore the choice of V_b and A_L on the produced IF current magnitude, resulting conversion gains and DC current draw. DC bias V_b was swept from 0 to 0.9 V and amplitude A_L swept from 0 to 0.9 V, with RF input amplitude A_R fixed. The resulting mixer IF conversion gains are shown in Figure 7a and the DC current draw in Figure 7b. A ridge for local optimum conversion gain can be seen in Figure 7a, starting at low V_b /high A_L and showing a relationship between V_b and A_L pairings for local optimum gain over the surface. There is also a clear upper peak gain area centered near $V_b \sim V_{tt}$. The region adjacent to the peak gain also shows further possible tradeoff between A_L and V_b for a desired conversion gain near to peak.

The DC current consumption predicted by the mathematical model in Figure 7b highlights a rapid increase associated with increasing conversion gain towards maximum. Figure 7a shows that for a given fixed value of A_L and simply adjusting V_b , a wide range of conversion gains can be achieved. It is proposed that in many systems it will be easier to vary V_b to control performance, whilst A_L (LO power) will be fixed due to practical circuit implementation issues. By considering Figure 7a it can be seen that by adjusting V_b for a given A_L , the gain can be peaked, confirming what has been reported experimentally by others [11]. By jointly considering Figure 7a,b allows operational points to be found for A_L and V_b that give close to peak conversion gain but allow DC current to be minimized.

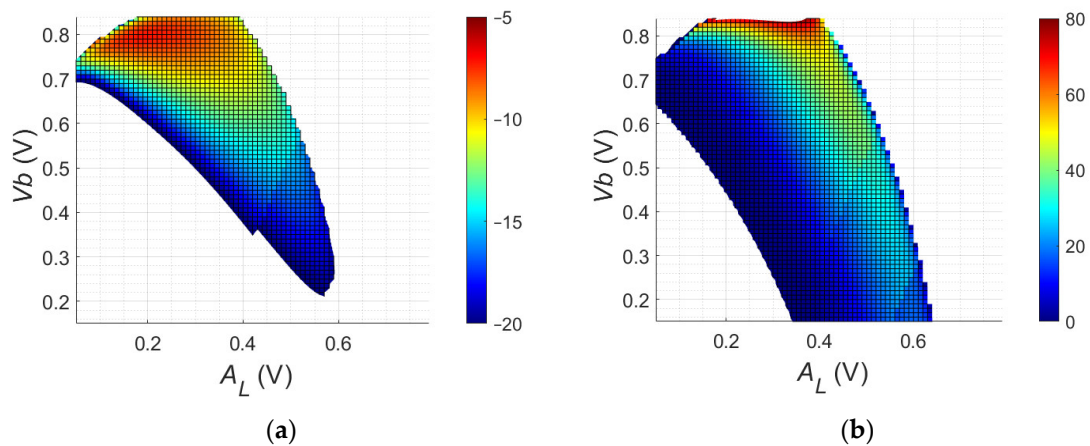


Figure 7. Mathematical model: (a) conversion gain (dB); (b) DC current draw (mA).

An example of predicting V_b for a given A_L using model Equation (34), compared to the ADS circuit time-domain simulation, is presented in Figure 8. This shows good agreement between the model Equation (34) and the ADS circuit simulation, for achieving a 30 mS conversion transconductance.

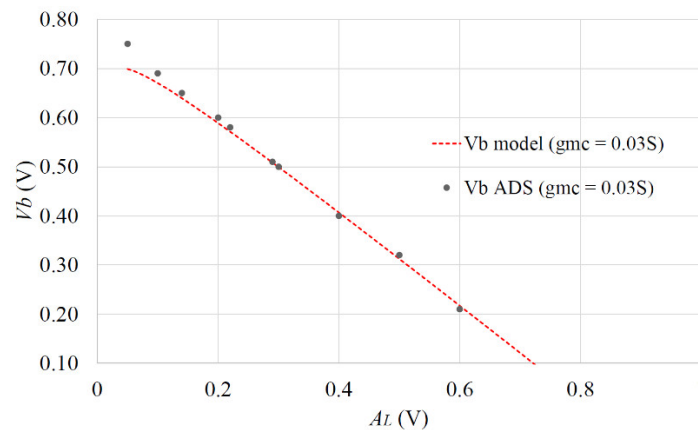


Figure 8. Comparison of Equation (34) vs. ADS simulation for V_b & A_L to obtain 30 ms g_m .

Figure 9a shows the simulation using Equation (24) to calculate IP1dB is sensitive to both V_b and A_L (LO power), with higher A_L and higher V_b generally improving the achieved IP1dB, as might be expected. The input RF voltage corresponding to IIP3 can also now be predicted, using Equation (25), and is shown in Figure 9b, showing a similar trend. The P1dBI and IIP3 can also be seen to be more sensitive to V_b for lower LO powers.

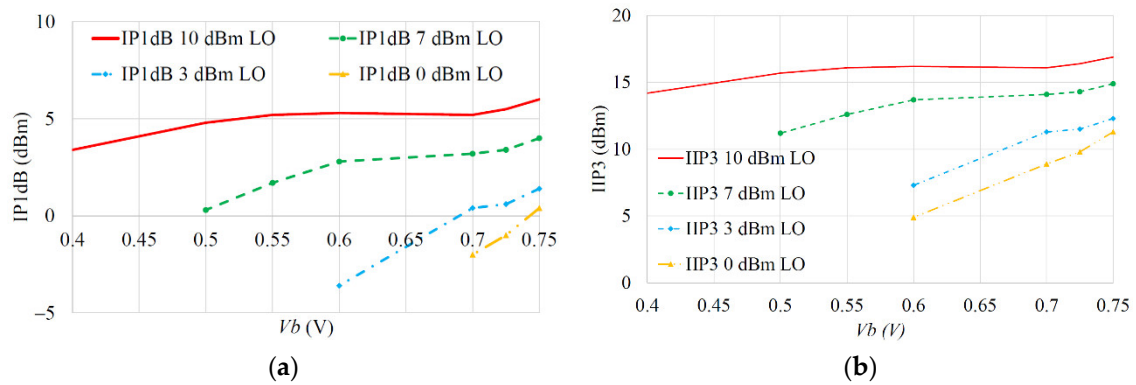


Figure 9. Linearity models as function of V_b and LO power: (a) IP1dB; (b) IIP3.

The collector current full model consisting of Equations (1)–(7) and Figure 1b are necessarily complex to sufficiently represent the current. Figure 10a shows conversion gain and Figure 10b DC current at 7 dBm and 3 dBm LO powers, when comparing the results for the full collector current model and a simpler version just using Equation (1). The simple collector current model leads to a significant overestimate of collector current so cannot be used. Thus, comparisons using the full model are shown in Section 5.2.

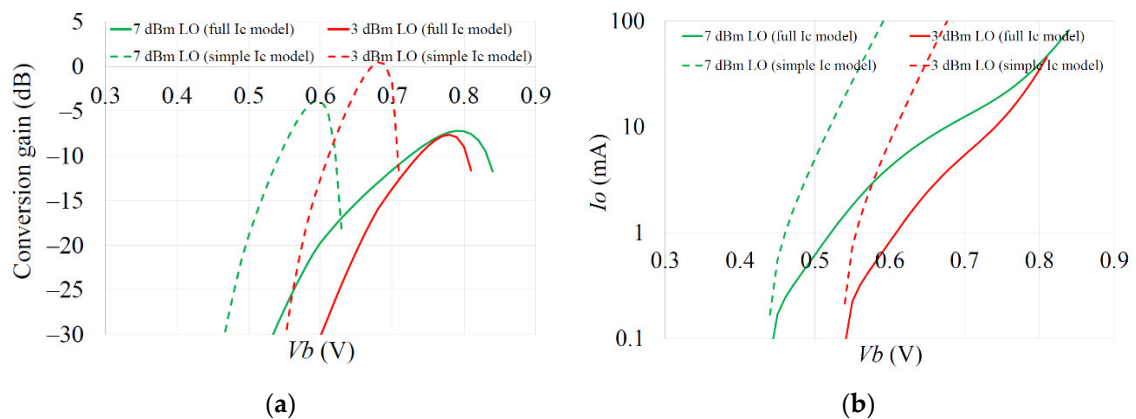


Figure 10. Comparison of effect of simple and full model for collector current, as function of V_b and LO power on: (a) Conversion gain; (b) DC current.

5.2. Lab Comparison Measurements of Hardware Mixer Prototype

The input rat-race combiner was tested within the implemented mixer, giving an LO to RF port isolation of 10 dB from 19 GHz to 25 GHz and 21 dB from 20 GHz to 23 GHz. The results of [7] show that simply defining a fixed consumed DC current and then adjusting V_b and A_L to achieve the DC current will not result in constant gain. Thus, lab tests for this paper swept V_b for each LO drive level and measured the resulting conversion gain.

The resulting trade-off between the LO drive A_L and bias V_b for a desired conversion gain can be observed in Figures 11 and 12, comparing the mathematical model, Keysight ADS simulation and measured results. The DC current draw was also measured for the mixer configurations and is presented in Figures 13 and 14. The various RMSE for the conversion gain and DC current are presented in Table 2. The errors in predicting the peak conversion gain are presented in Table 3. The DC currents show good agreement between the mathematical model, circuit simulations and measured PCB results, with RMSE errors better than 2 mA between the model and circuit simulations.

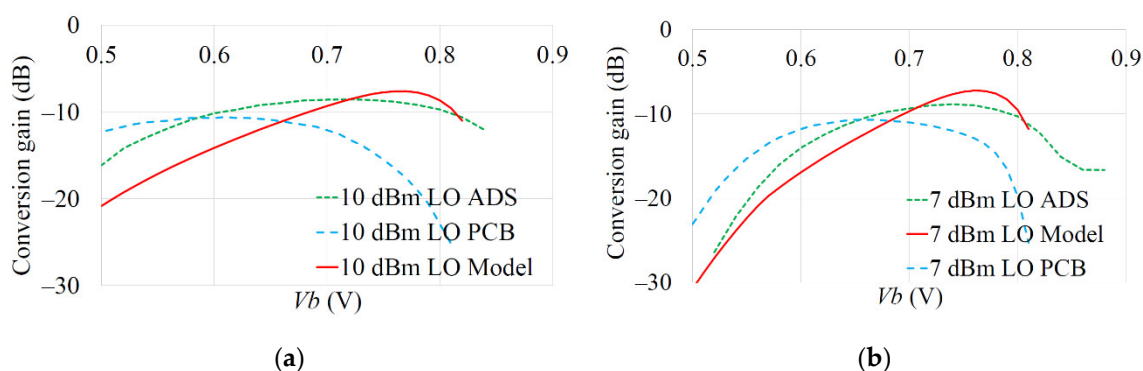


Figure 11. Model, ADS and measured PCB comparisons of mixer conversion gain as a function of V_b at: (a) 10 dBm LO drive; (b) 7 dBm LO drive.

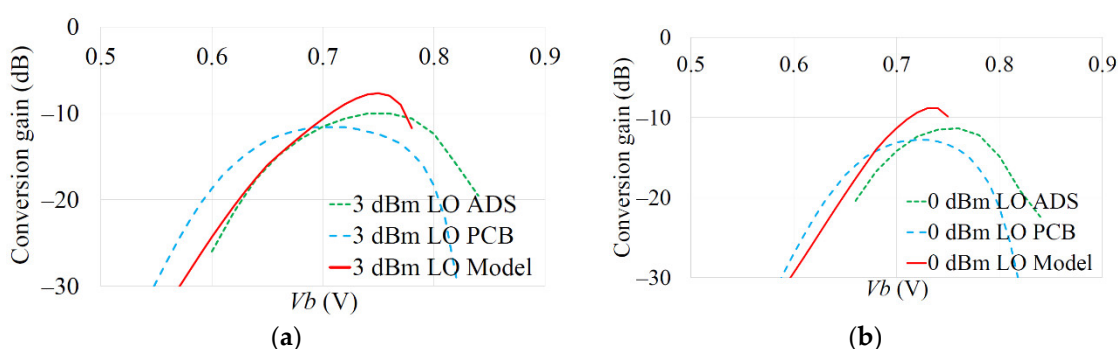


Figure 12. Model, ADS and measured PCB comparisons of mixer conversion gain as a function of V_b : (a) 3 dBm LO drive; (b) 0 dBm LO drive.

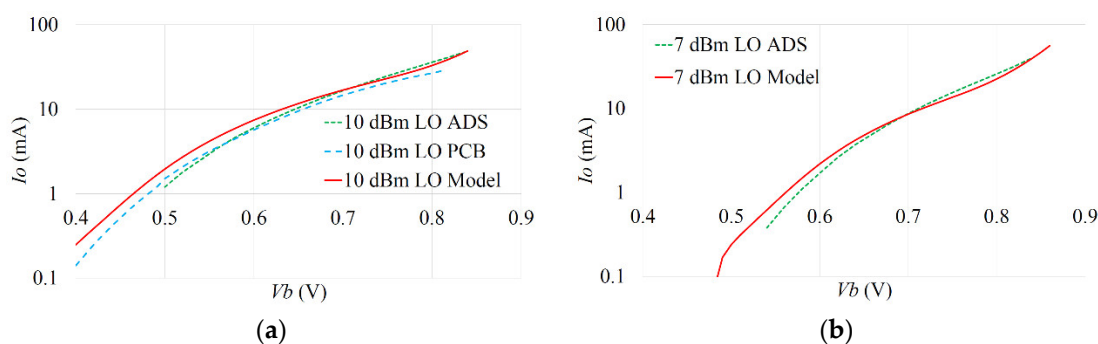


Figure 13. Model, ADS and PCB comparison of mixer DC draw as a function of V_b and LO drive at: (a) 10 dBm; (b) 7 dBm.

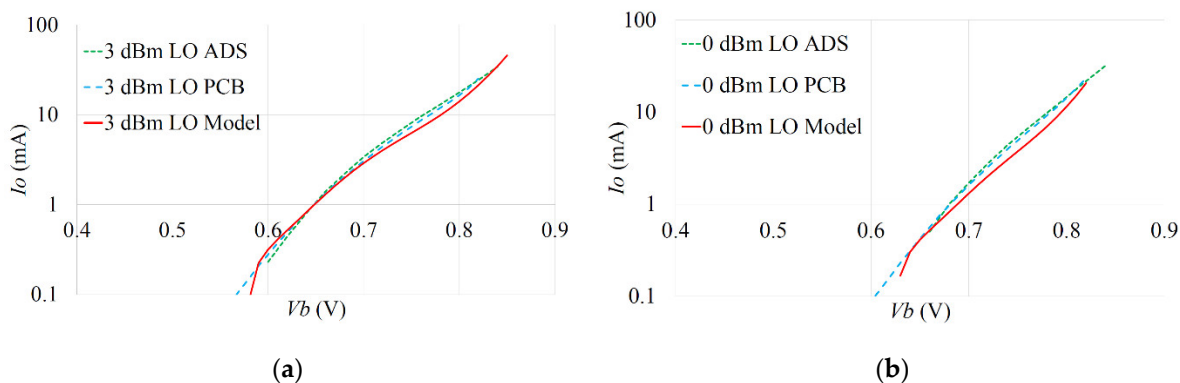


Figure 14. Model, ADS and PCB comparison of mixer DC draw as a function of V_b and LO drive at: (a) 3 dBm; (b) 0 dBm.

Table 2. RMSE fitting error for conversion gain & DC current.

	10 dBm LO	7 dBm LO	3 dBm LO	0 dBm LO	
Gc: Model-PCB	8.0	6.0	4.3	2.7	dB
Gc: ADS-PCB	5.2	5.5	5.3	5.2	dB
Gc: Model-ADS	3.0	1.8	1.3	2.7	dB
DC Draw: Model-PCB	2.4	-	1.1	1.2	mA
DC Draw: ADS-PCB	3.4	-	0.7	0.6	mA
DC Draw: Model-ADS	1.6	1.6	1.9	1.7	mA

Table 3. Error in peak conversion gain prediction.

	10 dBm LO	7 dBm LO	3 dBm LO	0 dBm LO	
Gc: Model-PCB	0.9	1.6	2.4	2.5	dB
Gc: ADS-PCB	3.0	3.5	3.9	4.0	dB
Gc: Model-ADS	2.0	1.8	1.6	1.4	dB

The general shape of the gain curves from the model, ADS simulation and PCB results show reasonable trend agreement. From Table 3, the model predicted peak Gc is within 2.0 dB of circuit simulation results and within 2.5 dB of measured PCB results. From Table 2, the RMSE of the model Gc compared to the measured PCB is similar to that due to full circuit simulation. The remaining error is possibly because, for simplicity, the model does not include all BJT current limiting aspects (which may require use of much more complex transistor models, such as Mextram and thus losing the convenience of the simple GP model). The F_T of the BFP740F is 45 GHz (typical) so the relatively close operational frequency of the mixer and tolerancing of the real device may have also led to some of the differences seen compared to the measured data. An increased sensitivity to LO power on conversion gain, for operation close to F_T , is seen in [53] for a Gilbert Cell architecture and this could also be an issue.

The published works discussed in Section 1.2 typically report a measurement to simulation error of circa 1 dB. However, there are very few published works that provide results of theoretical predictions of conversion gain or linearity as a function of base/gate DC bias and LO power. There are also very few works that have investigated the relationship between LO power and base/gate bias, which was a key motivator for this paper. In [8] the authors report conversion gain for an indium–phosphide (InP) double heterojunction BJT mixer with fixed bias operating in fundamental mode at 140 GHz, with an error in predicted Gc ranging from 0 dB to circa 10 dB over a range of LO powers. Table 2 shows a better prediction accuracy over a range of biases and powers (though at a lower carrier frequency). In [9] the authors show a InP High Electron Mobility Transistor acting as a mixer at 85 GHz and showing a decreasing conversion loss as LO power is increased, for two gate bias voltages. For high LO powers the conversion loss converges, as also seen in this work in Figures 11 & 12. In [9] a 5 dB reduction in Gc is seen as the bias is reduced, a trend also predicted and seen in this paper. The authors of [10] present results for a GaAs (FET) mixer at 7.8 GHz, showing Gc measurements and theoretical predictions agreeing within circa 0.5 dB. This is notably better than the results in this work, but are at a lower frequency and with a FET technology rather than BJT. In [11] an E band SiGe BJT ring mixer is reported, with circuit simulation results showing that bias and LO amplitude can be traded (e.g., 0.3 V LO amplitude & 0.7 V bias give similar Gc to 0.7 V LO & 0.5 V bias)—as also proposed in this work and seen in Figures 11 and 12. However, no theoretical calculation prediction of gain is provided. The authors of [11] report the measured conversion gain differs by circa 3 dB from that simulated. In [21] the g_{m_c} of a FET VHF mixer is seen to increase for increasing bias and increasing LO amplitude—as also seen here with the BJT.

By adjusting the base DC bias V_b , the single-ended mixer LO power was reduced from +10 dBm to +3 dBm, while suffering only a 1 dB drop in the conversion gain and benefitting from a 2 mA drop in DC draw. The accuracy of predicting V_b using Equation (34) was assessed, compared to the V_b required for the test PCB, in the lab for a desired gain and LO power. The error in predicting the required V_b over the range of LO powers was found to be less than 10%.

The measured PCB mixer conversion gain is negative largely owing to losses in the input combiner rat-race and network feeding the transistor base and choice of transistor. However, it should be noted that a negative conversion gain is common in simple single-device mixers operating at frequencies in the tens of gigahertz. Whilst it would be theoretically possible to de-embed the active part of the mixer so that it can be considered in isolation from passive circuits, it would still be necessary to include the effect of these losses when measuring and comparing to the test PCB. Therefore, the measurements reported here are compared to the RF ports of the built PCB and include the effect of all losses, allowing a direct comparison.

Figure 15 shows results from lab measurements of the mixer's G_c across the RF input range 24 GHz–28 GHz with a 3 dBm LO and with various applied V_b (results are normalized to the G_c at 26 GHz). This shows the mixer's measured conversion gain dependency on V_b is not a strong function of frequency—suggesting the single mathematical model can be used over the band.

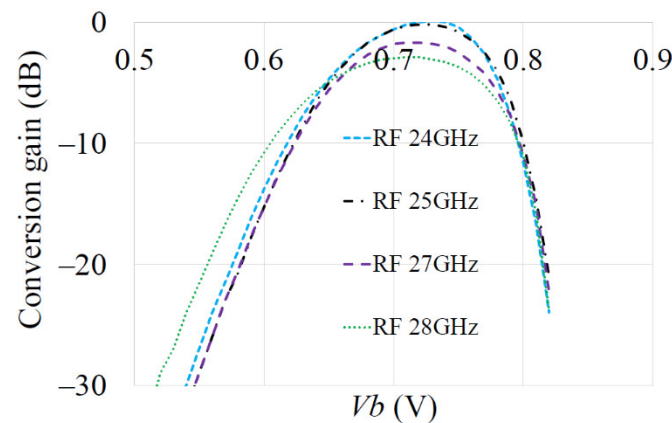


Figure 15. Measured gain (normalized to gain at 26 GHz) across range 24–28 GHz as function of V_b (3 dBm LO drive).

A comparison of IP1dB for the prototype mixer and the model Equation (24) is presented in Figure 16a, showing good agreement between the mathematical model and laboratory measurements for all tested LO powers, with a model error of circa 1 dB. Figure 16b shows the comparison between the measured IIP3, an ADS harmonic balance (HB) simulation and Equation (25). Since the model underestimates the IP1dB, it could be expected to also underestimate the IIP3 by a similar amount. In practice, the model underestimates IIP3 by circa 5 dB. It is interesting to note that whereas the model tends to underestimate the IIP3 by 5 dB (or less) the ADS HB simulation tends to overestimate it by 5 dB. These results point to a general difficulty in modeling mixer nonlinearity, which can be sensitive to DC bias as also seen in [21], or possibly due to memory effects. However, the predicted IIP3 trend is correct and a ~5 dB uncertainty may be acceptable in early-stage designs. The authors of [20] show that IIP2 increases as LO power increases, to a certain point, as also seen in Figure 16b though for IIP3. This improvement in linearity for increasing LO power and sensitivity to V_b is also predicted in Figure 9a,b. Additionally [21] confirms the third order products reduce as LO drive increases, leading to an increased IIP3.

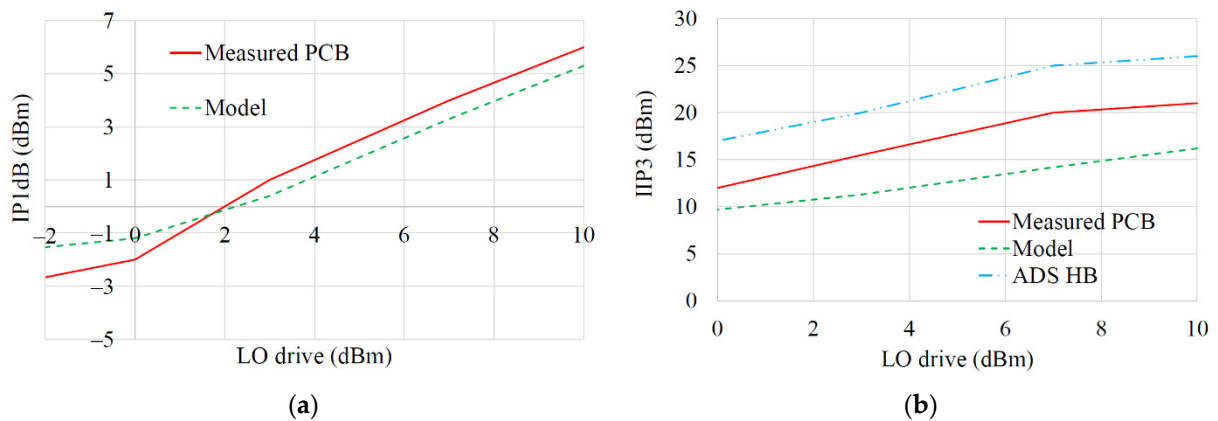


Figure 16. Measured and mathematical model comparison for IP1dB & IIP3 as function of LO drive level (V_b chosen to achieve peak gain for each tested LO drive power): (a) IP1dB; (b) IIP3.

The RF input 3 dB bandwidth of the mixer was measured for an IF at 5 GHz and found to be 1.4 GHz (+10 dBm LO power). The IF 3 dB bandwidth of the mixer was also measured, and found to be 900 MHz, with an LO of 21 GHz and +10 dBm LO power.

5.3. Noise Figure Measurements

Since the mixer has circa 10 dB conversion loss (CL), this will dominate any noise figure (NF) results. This was confirmed by measuring the single sideband (SSB) NF and associated conversion loss on the prototype for 10 dBm and 0 dBm LO powers, as shown in Figure 17. The NF was measured using a noise diode (Keysight 346CK01) and spectrum analyzer with LNA (Keysight PXA N9030B) and evaluating the added noise from the mixer. The SSB NF of the mixer can be seen to be within 1 dB of the conversion loss, as expected. It is also worth noting from Figure 17 that if V_b is carefully selected (based on maximizing G_c), only a 2 dB degradation in NF will be suffered yet the LO power can be reduced by 10 dB.

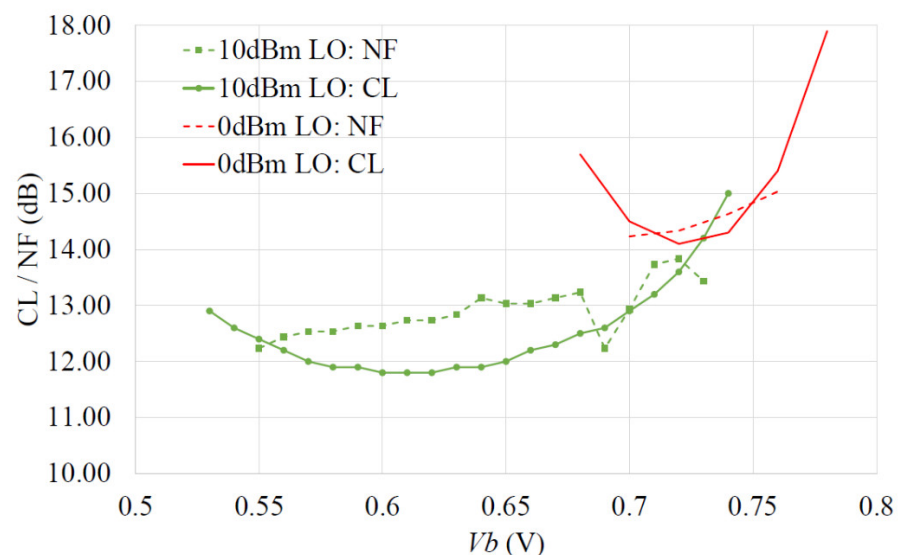


Figure 17. Measured mixer SSB NF and conversion loss (CL) for 10 dBm and 0 dBm LO drive.

6. Conclusions

It is shown that G_c , DC draw, IP1dB and IIP3 that can be achieved from a SiGe bipolar transistor downconverting mixer can be predicted to useful accuracy using the developed, simple mathematical models without recourse to full circuit simulation. Furthermore, an equation to predict the required V_b , for a base LO drive A_L , to achieve a desired conversion transconductance is presented. The transconductance mixer mathematical models were compared to Keysight ADS circuit simulations and prototype hardware.

During tests, the mathematical model predicts peak conversion gain within 2.0 dB of circuit simulation results and within 2.5 dB of measured PCB results. The conversion gain RMSE between the model and circuit simulation is 3 dB worst-case, 1.3 dB best-case. The RMSE between predicted DC current and circuit simulation is below 2 mA. The model predicts IP1dB to 1 dB and IIP3 to circa 5 dB accuracies, with respect to the measured PCB.

Another key finding is that for operation below the peak G_c , the LO drive power can be traded for V_b bias while maintaining a defined conversion gain. An equally important finding is that conversion gain can be optimized by V_b as LO power is reduced and this can be predicted. This is an important finding because LO power is often challenging to generate at mmWave frequencies and impacts battery life of portable products. This also allows system designers using front-end mixers to configure them for a particular operational gain scenario, dynamically degrading gain and linearity where acceptable, to save power.

Although the model agrees well with simulation and measured results, some of the differences between the measured results and the mathematical models are likely due to the use of standard commercial uncharacterized surface-mount packaged transistors. The lab prototype used to validate the models also serves to demonstrate that a practical 26 GHz mixer can be realized using a low cost packaged transistor and conventional PCB design.

In general, mixer use-cases will likely have a primary design criterion based on NF/ G_c or IIP3/P1dBi or obtaining best overall RF performance for a given available LO power. Hence, using the developed mathematical models, the following mixer scenarios can be investigated early in a design before embarking on a full circuit design:

- NF/ G_c : best settings for A_L , V_b can be found and resulting IIP3/P1dBi predicted;
- IIP3/P1dBi: best settings for A_L , V_b can be found and resulting NF/ G_c predicted;
- Fixed LO power: Achievable NF, G_c , IIP3, P1dBi and DC power as function of V_b can be predicted;
- Fixed DC power: Achievable NF, G_c , IIP3, P1dBi as function of LO power can be predicted.

Funding: This research was funded by UKRI, grant number MR/T043164/1. The APC was funded by the UKRI.

Conflicts of Interest: The author declares no conflict of interest.

References

1. Hong, W.; Jiang, Z.H.; Yu, C.; Hou, D.; Wang, H.; Guo, C.; Hu, Y.; Kuai, L.; Yu, Y.; Jiang, Z.; et al. The Role of Millimeter-Wave Technologies in 5G/6G Wireless Communications. *IEEE J. Microw.* **2021**, *1*, 101–122. <https://doi.org/10.1109/jmw.2020.3035541>.
2. Chataut, R.; Akl, R. Massive MIMO Systems for 5G and beyond Networks—Overview, Recent Trends, Challenges, and Future Research Direction. *Sensors* **2020**, *20*, 2753.
3. Yang, T.Y.; Chiou, H.K. A 28 GHz Sub-Harmonic Mixer Using LO Doubler in 0.18-Mm CMOS Technology. In Proceedings of the Digest of Papers—IEEE Radio Frequency Integrated Circuits Symposium, San Francisco, CA, USA, 10–13 June 2006; Volume 2006, pp. 209–212.
4. Chang, Y.T.; Lin, K.Y. A 28-GHz Bidirectional Active Gilbert-Cell Mixer in 90-Nm CMOS. *IEEE Microw. Wirel. Compon. Lett.* **2021**, *31*, 473–476. <https://doi.org/10.1109/LMWC.2021.3061658>.
5. Kumar, S.; Saraiyan, S.; Dubey, S.K.; Pal, S.; Islam, A. A 2.4 GHz Double Balanced Downconversion Mixer with Improved Conversion Gain in 180-Nm Technology. *Microsyst. Technol.* **2020**, *26*, 1721–1731. <https://doi.org/10.1007/s00542-019-04718-3>.

6. Varonen, M.; Kärkkäinen, M.; Kantanen, M.; Halonen, K.A.I. Millimeter-Wave Integrated Circuits in 65-Nm CMOS. *IEEE J. Solid-State Circuits* **2008**, *43*, 1991–2002. <https://doi.org/10.1109/JSSC.2008.2001902>.
7. Ball, E.A. Investigation into the Relationship Between Conversion Gain, Local Oscillator Drive Level and DC bias in a SiGe Transistor Transconductance Modulated Mixer at 24–28 GHz. In Proceedings of the IEEE Texas Symposium on Wireless & Microwave Circuits and Systems, Waco, TX, USA, 18 May 2021. <https://doi.org/10.1109/WMCS52222.2021.9493227>.
8. Yan, Y.; Bao, M.; Gunnarsson, S.E.; Zirath, H. A 110-170-GHz Multi-Mode Transconductance Mixer in 250-nm InP DHBT Technology. *IEEE Trans. Microw. Theory Tech.* **2015**, *63*, 2897–2904. <https://doi.org/10.1109/TMTT.2015.2459676>.
9. Ning, X.; Yao, H.; Wang, X.; Jin, Z. A W-Band Single-Ended Downconversion/Upconversion Gate Mixer in InP HEMT Technology. In Proceedings of the 2013 IEEE International Conference on Microwave Technology and Computational Electromagnetics, Qingdao, China, 25 August 2013. <https://doi.org/10.1109/ICMTCE.2013.6812434>.
10. Pucel, R.A.; Masse, D.; Bera, R. Performance of GaAs MESFET Mixers at X Band. *IEEE Trans. Microw. Theory Tech.* **1976**, *24*, 351–360. <https://doi.org/10.1109/TMTT.1976.1128854>.
11. Del Rio, D.; Gurutzeaga, I.; Rezola, A.; Sevillano, J.F.; Velez, I.; Gunnarsson, S.E.; Tamir, N.; Saavedra, C.E.; Gonzalez-Jimenez, J.L.; Siligaris, A.; et al. A Wideband and High-Linearity E-Band Transmitter Integrated in a 55-nm SiGe Technology for Backhaul Point-to-Point 10-Gb/s Links. *IEEE Trans. Microw. Theory Tech.* **2017**, *65*, 2990–3001. <https://doi.org/10.1109/TMTT.2017.2664833>.
12. Chen, J.D.; Wang, W.J. A K-Band Low-Noise and High-Gain Down-Conversion Active Mixer Using 0.18-Mm CMOS Technology. *Wirel. Pers. Commun.* **2019**, *104*, 407–421. <https://doi.org/10.1007/s11277-018-6027-4>.
13. Beigizadeh, M.; Nabavi, A. Design of a High Gain and Highly Linear Common-Gate UWB Mixer in K-Band. *Analog. Integr. Circuits Signal Process.* **2014**, *78*, 501–509. <https://doi.org/10.1007/s10470-013-0132-9>.
14. Solati, P.; Yavari, M. A Wideband High Linearity and Low-Noise CMOS Active Mixer Using the Derivative Superposition and Noise Cancellation Techniques. *Circuits Syst. Signal Process.* **2019**, *38*, 2910–2930. <https://doi.org/10.1007/s00034-019-01023-2>.
15. Heidari, T.; Nabavi, A. Design and Analysis of a Wideband Compact LNA-Mixer in Millimeter Wave Frequency. *Analog. Integr. Circuits Signal Process.* **2020**, *105*, 371–383. <https://doi.org/10.1007/s10470-020-01737-3>.
16. Gladson S.C.; Bhaskar, M. A Low-Power RF Mixer with Harmonic Cancellation for IEEE 802.15.4 Portable, Wearable Wireless Applications. *AEU-Int. J. Electron. Commun.* **2020**, *124*, 153335. <https://doi.org/10.1016/j.aeue.2020.153335>.
17. Sivonen, P.; Vilander, A.; Pärssinen, A. Cancellation of Second-Order Intermodulation Distortion and Enhancement of IIP2 in Common-Source and Common-Emitter RF Transconductors. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2005**, *52*, 305–317. <https://doi.org/10.1109/TCSI.2004.841571>.
18. Nguyen, T.T.; Fujii, K.; Pham, A.-V. Highly Linear Distributed Mixer in 0.25- μm Enhancement-Mode GaAs pHEMT Technology. *IEEE Microw. Wirel. Compon. Lett.* **2017**, *27*, 1116–1118. <https://doi.org/10.1109/LMWC.2017.2750071>.
19. Nguyen, T.T.; Riddle, A.; Fujii, K.; Pham, A.-V. Development of Wideband and High IIP3 Millimeter-Wave Mixers. *IEEE Trans. Microw. Theory Tech.* **2017**, *65*, 3071–3079. <https://doi.org/10.1109/TMTT.2017.2669042>.
20. Kivekäs, K.; Pärssinen, A.; Halonen, K.A.I. Characterization of IIP2 and DC-Offsets in Transconductance Mixers. *IEEE Trans. Circuits Syst. II Analog. Digit. Signal Process.* **2001**, *48*, 1028–1038. <https://doi.org/10.1109/82.982353>.
21. Surana, D.C.; Gardiner, J.G. Gain and Distortion Properties of FET Mixers and Modulators. *IEEE Trans. Electromagn. Compat.* **1974**, *EMC-16*, 29–38. <https://doi.org/10.1109/TEMC.1974.303320>.
22. Korotkov, A.S. Double-Balanced Mixer Based on MOSFETs. *Russ. Microelectron.* **2011**, *40*, 128–140. <https://doi.org/10.1134/S1063739711020053>.
23. Bae, B.; Han, J. 24-40 GHz Gain-Boosted Wideband CMOS Down-Conversion Mixer Employing Body-Effect Control for 5G NR Applications. *IEEE Trans. Circuits Syst. II Express Briefs* **2022**, *69*, 1034–1038. <https://doi.org/10.1109/TCSII.2021.3119995>.
24. Amirabadizadeh, S.; Bijari, A.; Alizadeh, H.; Mehrshad, N. Performance Improvement of a Down-Conversion Active Mixer Using Negative Admittance. *Circuits Syst. Signal Process.* **2021**, *40*, 22–49. <https://doi.org/10.1007/s00034-020-01477-9>.
25. Bidi, A.A.S.; Karimi, G. Design of High Linearity Inductor-Less Active CMOS Mixer Based on Volterra Series Analysis. *Circuits Syst. Signal Process.* **2020**, *39*, 4810–4828. <https://doi.org/10.1007/s00034-020-01407-9>.
26. García, J.A.; de La Fuente, M.L.; Zamanillo, J.M.; Mediavilla, A.; Tazón, A.; Pedro, J.C.; Carvalho, N.B. Intermodulation Distortion Analysis of FET Mixers under Multitone Excitation. In Proceedings of the 2000 30th European Microwave Conference, EuMC 2000, Paris, France, 2–5 October 2000; pp. 1-4.
27. Xu, H.; Chen, J.; Wu, X.; Peng, C.; Yu, J.; Yuan, B.; Xie, Z. A 32–40 GHz 4-Channel Transceiver with 6-bit Amplitude and Phase Control. *AEU Int. J. Electron. Commun.* **2021**, *139*, 153925. <https://doi.org/10.1016/j.aeue.2021.153925>.
28. Avenier, G.; Diop, M.; Chevalier, P.; Troillard, G.; Loubet, N.; Bouvier, J.; Depoyan, L.; Derrier, N.; Buczko, M.; Leyris, C.; et al. 0.13 μm SiGe BiCMOS Technology Fully Dedicated to Mm-Wave Applications. *IEEE J. Solid-State Circuits* **2009**, *44*, 2312–2321. <https://doi.org/10.1109/JSSC.2009.2024102>.
29. Wietstruck, M.; Marschmeyer, S.; Schulze, S.; Wipf, S.T.; Wipf, C.; Kaynak, M. Recent Developments on SiGe BiCMOS Technologies for Mm-Wave and THz Applications. In Proceedings of the 2019 IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA, 2 June 2019; pp. 1126–1129.
30. Pruvost, S.; Telliez, I.; Danneville, F.; Dambrine, G.; Rolland, N.; Pourchon, F. A 40 GHz Single-Ended Down-Conversion Mixer in 0.13 μm SiGeC BiCMOS HBT. *IEEE Microw. Wirel. Compon. Lett.* **2005**, *15*, 496–498. <https://doi.org/10.1109/LMWC.2005.852773>.

31. Wang, X.; Guo, B.; Wu, J.; Gong, J. A 28 GHz Front-End for Phased Array Receivers Simulated in 180 Nm CMOS. In Proceedings of the 2020 IEEE International Conference on Semiconductor Electronics (ICSE), Kuala Lumpur, Malaysia, 28 July 2020; pp. 1–4.
32. Kivekäs, K.; Pärssinen, A.; Ryyänen, J.; Jussila, J.; Halonen, K. Calibration Techniques of Active BiCMOS Mixers. *IEEE J. Solid-State Circuits* **2002**, *37*, 766–769. <https://doi.org/10.1109/JSSC.2002.1004581>.
33. Fonte, A.; Plutino, F.; Moquillon, L.; Razafimandimby, S.; Pruvost, S. 5G 26 GHz and 28 GHz Bands SiGe:C Receiver with Very High-Linearity and 56 DB Dynamic Range. In Proceedings of the 2018 13th European Microwave Integrated Circuits Conference (EuMIC), Madrid, Spain, 23 September 2018; pp. 57–60.
34. Kivekas, K.; Parssinen, A.; Jussila, J.; Ryyanen, J.; Halonen, K. Design of Low-Voltage Active Mixer for Direct Conversion Receivers. In Proceedings of the ISCAS 2001—2001 IEEE International Symposium on Circuits and Systems, Conference Proceedings, Sydney, NSW, Australia, 6–9 May 2001; Volume 4, pp. 382–385.
35. Reynolds, S.K. A 60-GHz Superheterodyne Downconversion Mixer in Silicon-Germanium Bipolar Technology. *IEEE J. Solid-State Circuits* **2004**, *39*, 2065–2068. <https://doi.org/10.1109/JSSC.2004.835838>.
36. Mazor, N.; Sheinman, B.; Katz, O.; Levinger, R.; Bloch, E.; Carmon, R.; Ben-Yishay, R.; Elad, D. Highly Linear 60-GHz SiGe Downconversion/Upconversion Mixers. *IEEE Microw. Wirel. Compon. Lett.* **2017**, *27*, 401–403. <https://doi.org/10.1109/LMWC.2017.2678426>.
37. Qayyum, J.A.; Albrecht, J.D.; Ulusoy, A.C. A Compact V-Band Upconversion Mixer with -1.4-dBm OP1dB in SiGe HBT Technology. *IEEE Microw. Wirel. Compon. Lett.* **2019**, *29*, 276–278. <https://doi.org/10.1109/LMWC.2019.2901395>.
38. Sweet, A.A. *Designing Bipolar Transistor Radio Frequency Integrated Circuits*, 1st ed.; Artech House: Norwood, MA, USA, 2008; pp. 200–205.
39. Reynolds, S.K.; Powell, J.D. 77 and 94-GHz Downconversion Mixers in SiGe BiCMOS. In Proceedings of the 2006 IEEE Asian Solid-State Circuits Conference, ASSCC 2006, Hangzhou, China, 13–15 November 2006; pp. 191–194.
40. Choi, C.; Son, J.H.; Lee, O.; Nam, I. A +12dBm OIP3 60-GHz RF Downconversion Mixer with an Output-Matching, Noise- and Distortion-Canceling Active Balun for 5G Applications. *IEEE Microw. Wirel. Compon. Lett.* **2017**, *27*, 284–286. <https://doi.org/10.1109/LMWC.2017.2661964>.
41. Testa, P.V.; Szilagyi, L.; Xu, X.; Carta, C.; Ellinger, F. A Low-Power Low-Voltage Down-Conversion Mixer for 5G Applications at 28 GHz in 22-Nm FD-SOI CMOS Technology. In Proceedings of the Asia-Pacific Microwave Conference Proceedings, APMC, Hong Kong, 8–11 December 2020; pp. 911–913.
42. Bhatt, D.; Mukherjee, J.; Redouté, J.M. Low-Power Switched Transconductance Mixer and LNA Design for Wi-Fi and WiMAX Applications in 65 Nm CMOS. *IET Microw. Antennas Propag.* **2018**, *12*, 1736–1744. <https://doi.org/10.1049/iet-map.2017.0798>.
43. Yang, S.; Hu, K.; Fu, H.; Ma, K.; Lu, M. A 24-to-30 GHz Ultra-High-Linearity Down-Conversion Mixer for 5G Applications Using a New Linearization Method. *Sensors* **2022**, *22*, 3802. <https://doi.org/10.3390/s22103802>.
44. Xu, L.; Wang, Z.; Li, Q. Design of a Broadband Millimeter-Wave Monolithic IQ Mixer. *J. Infrared Millim. Terahertz Waves* **2010**, *31*, 593–600. <https://doi.org/10.1007/s10762-010-9615-2>.
45. Lee, D.; Lee, M.; Park, B.; Song, E.; Lee, K.; Lee, J.; Han, J.; Kwon, K. 24–40 GHz MmWave Down-Conversion Mixer with Broadband Capacitor-Tuned Coupled Resonators for 5G New Radio Cellular Applications. *IEEE Access* **2022**, *10*, 16782–16792. <https://doi.org/10.1109/ACCESS.2022.3149311>.
46. Xavier, B.A.; Aitchison, C.S. Simulation and Modelling of a Heterojunction Bipolar Transistor Mixer. In Proceedings of the IEEE MTT-S International Microwave Symposium Digest, Albuquerque, NM, USA, 1–5 June 1992; Volume 1, pp. 333–336.
47. Antognetti, P.; Massobrio, G. *Semiconductor Device Modeling with SPICE*, 2nd ed.; McGraw Hill: New York, NY, USA, 1993.
48. Pozar, D.M. *Microwave Engineering*, 4th ed.; Wiley: Hoboken, NJ, USA, 2012; pp. 637–655.
49. Maas, S.A. *Nonlinear Microwave and RF Circuits*, 2nd ed.; Artech House: Norwood, MA, USA, 2003; pp. 497–514.
50. Robertson, I.D.; Lucyszyn, S. *RFIC and MMIC Design and Technology*, 1st ed.; The IET: London, UK, 2001; pp. 316–321.
51. Kang, S.; Choi, B.; Kim, B. Linearity Analysis of CMOS for RF Applications. *IEEE Trans. Microw. Theory Tech.* **2003**, *51*, 972–977. <https://doi.org/10.1109/TMTT.2003.808709>.
52. Liu, Z.; Dong, J.; Chen, Z.; Jiang, Z.; Liu, P.; Wu, Y.; Zhao, C.; Kang, K. A 62–90 GHz High Linearity and Low Noise CMOS Mixer Using Transformer-Coupling Cascode Topology. *IEEE Access* **2018**, *6*, 19338–19344. <https://doi.org/10.1109/ACCESS.2018.2814062>.
53. Syu, J.S.; Meng, C.; Wang, C.L. 2.4-GHz Low-Noise Direct-Conversion Receiver with Deep N-Well Vertical-NPN BJT Operating near Cutoff Frequency. *IEEE Trans. Microw. Theory Tech.* **2011**, *59*, 3195–3205. <https://doi.org/10.1109/TMTT.2011.2169421>.