Partial Power Processing Multiport DC-DC Converter with Radial Module Connections

Yuwei Liu, Yihua Hu, *Senior Member*, Guipeng Chen, *Member*, *IEEE,* Huiqing Wen, *Senior Member*, *IEEE*

***Abstract*- The partial power processing (PPP) concept has been extensively employed in many two-port converters to achieve high efficiency and high power density by modifying one of the original converter ports to be connected in series between input and output. This is attractive but is confined to two-port applications, and how to extend it to multiport applications is not clear. Hence, this paper aims to explore a generalized PPP multiport scheme by arranging the connection of the module rather than the converter. For a PPP single-input(output)-N-outputs(inputs) converter, one terminal of all N+1 modules is connected together to construct a radial structure, and another terminal is series/parallel connected with the input/output port. Each module only needs to process partial power caused by the voltage or current difference between input and output. Therefore, the required power rating of components is effectively reduced, contributing to low cost as well as low power loss. In this paper, a PPP single-input dual-output converter with active bridge modules is also taken as an example to be introduced in detail, designed and experimented upon, which validates that high efficiency and high power density can be achieved.**

Index Terms- Partial power processing, multiport DC-DC, radial module connection, active bridge.

I. Introduction

The concept of partial power processing (PPP) has been proposed to improve the overall efficiency and power density of DC-DC converters and was firstly applied in photovoltaic (PV) power systems [1]. When transmitting power from the PV array to the battery bank, one port of the utilized two-port DC-DC converter is changed to be connected in series between them. Therefore, only the partial power caused by the voltage difference is processed through the converter, while the other power is transferred directly. Assuming that the efficiencies of the two-port DC-DC converter and the direct transmission are η_1(η_1<100%) and η_2(η_2=100%), respectively, the total efficiency of the conversion must be larger than η_1. Therefore, the global efficiency of PPP is successfully improved when compared with the traditional method of processing the full power through the DC-DC converter. Moreover, because the DC-DC converter in the PPP system only processes a small part of the total power, its current and voltage stresses are correspondingly reduced, contributing to decreased cost and increased power density. Owing to these advantages, PPP two-port structures attract increasing attention, and they are already promoted to applications, such as space power systems [2, 3], wind turbines [4, 5], electric vehicles [6] and so on [7].

Two typical PPP two-port structures produced by changing the connection scheme of traditional isolated two-port DC-DC converters are proposed in [8], including the input-parallel-output-series structure and the input-series-output-parallel structure, which are named structure Type I and structure Type II, respectively [9], as shown in Fig. 1. From Fig. 1(a), node a_1 is connected to node d_1; therefore, port c_1d_1 is in series connection between the input port and output port, and port a_1b_1 is in parallel with input port V_i. Similarly, node b_2 is connected to node c_2 in Fig. 1(b), constructing the ISOP structure. In these structures, only the partial power generated by the voltage difference between V_i and V_o is processed by the DC-DC converter, while the other power is transmitted through the direct power delivery path. Accordingly, the ratio of the partial power P_p to the total power P_t is $(V_o\text{-}V_i)/V_o$ or $(V_o\text{-}V_i)/V_i$. In addition, the voltage and current stresses of the DC-DC converter in the PPP structure are relatively reduced when compared with the full power processing approach. The smaller the difference between port voltages V_i and V_o, the higher the efficiency and the greater the power density. On the other hand, V_i is smaller than V_o in both Fig. 1(a) and Fig. 1(b) if the polarities of ports c_1d_1 and a_2b_2 are positive, while the step-down voltage gain will be obtained if their polarities are reversed [10].

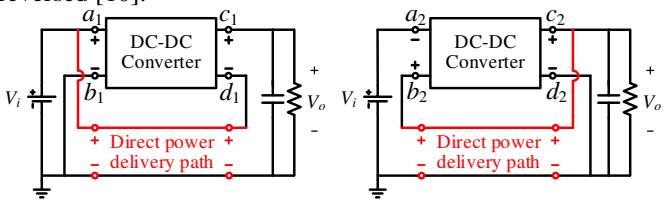

Fig. 1 Typical PPP two-port structures: (a) Type I and (b) Type II [9].

Based on these two structures, a variety of PPP two-port converters have been explored by using different isolated DC-DC converters, such as push-pull converters [11], phase-shifted full/half-bridge converters [12-15], flyback converters [16, 17], LLC converters [18], dual-active bridge (DAB) converter [19], and so on [20]. The topologies in [11-13] are able to realize

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voltage step-down, while voltage step-up is achieved in [14-20]. Nevertheless, because the port voltage polarities of these isolated DC-DC converters are fixed, the derived PPP two-port topologies are unable to realize buck-boost voltage gain. To obtain a more flexible voltage relationship, two methods for realizing buck-boost are proposed in [21-24]. The first one adds additional switches in series with diodes such that both boost mode and buck mode can be obtained [21, 22]. The other one employs an H-bridge to change the output voltage polarity of the full power isolated DC-DC converter [23, 24]. However, the added switches increase the conduction loss as well as the cost.

In addition to two-port applications, two PPP three-port converters have also been proposed in [25, 26]. In [25], an isolated Sepic converter was activated to realize PPP from the supercapacitor to the output when the output load current exceeded the threshold value. In [26], a PPP three-port converter with a reduced number of components was employed to transfer power from the battery and PV modules to the output load. Nevertheless, a specific architecture and converter were used in [25, 26], which makes it difficult to help discover more possible solutions for multiport applications.

From the above, the existing PPP research mainly focuses on two-port applications, and two general structures have been presented. On the other hand, although two PPP three-port converters were proposed, the general architecture of the PPP multiport converter is still lacking. Therefore, this paper proposes a generalized PPP single-input(output)-N-outputs(inputs) DC-DC architecture with radial module connections to expand PPP from two ports to multiple ports. Rather than changing the connection scheme based on the original DC-DC converter, N outputs (inputs) are connected radially via respective series connected modules to a center point, which is also connected with the positive pole of the single input (output). An N+1 module is also parallelly connected with the single input (output). In this radial structure, only the partial power generated by voltage or current differences between input and output will be supplied and transmitted through modules, while the other power is directly delivered. Therefore, the high efficiency is achieved, and the power density is improved with reduced voltage and current stresses of the components. In addition, modules can be replaced by a variety of multiport DC-DC converters to achieve partial power conversion. The possible choices can be a three-port Flyback converter [27], a three-port bidirectional Cuk converter [28], a multi-active bridge converter [29] and other multi-winding transformer-based DC-DC converters [30]. Due to the characteristics above, in addition to the applications mentioned for PPP two-port structures, the proposed PPP multiport structure is also suitable for other high-power multiport applications, such as DC microgrid.

In the rest of the paper, the proposed PPP multiport DC-DC architecture with radial module connections is first introduced in section II. Subsequently, a detailed analysis of an example active bridge module-based PPP single-input dual-output (SIDO) DC-DC converter is conducted in section III. In section IV, the corresponding characteristic analysis and design consideration are illustrated, followed by the experimental results of the prototype circuit in section V. Finally, the conclusions are drawn in section VI.

II. The Proposed PPP Multiport DC-DC Architecture with Radial Module Connections

The proposed PPP multiport DC-DC architecture is shown in Fig. 2, including the single-input multi-output (SIMO) architecture in Fig. 2 (a) and the multi-input single-output (MISO) architecture in Fig. 2(b). N+1 magnetically linked modules are employed for N+1 ports. From Fig. 2, one terminal of all modules M_1~M_{N+1} is connected to a center point, constructing a radial architecture. The other terminals of modules M_1~M_N are connected to the positive pole of outputs(inputs) V_{o1}~V_{oN}(V_{i1}~V_{iN}). In addition, module M_{N+1} is in parallel with the single input(output) V_{i1}(V_{o1}). All input and output share a common ground. In this radial structure, the number of outputs in Fig. 2(a) and inputs in Fig. 2(b) can be flexibly added or reduced, and the types of modules are diverse. Moreover, the output(input) voltage $V_{o(i)k}$ (k=1, 2, …, N) can be designed to be greater or smaller than the single input(output) voltage V_{i1}(V_{o1}) by adjusting the polarity of the module voltage V_k (k=1, 2, …, N). In addition, only a part of the system power is processed through modules, contributing to high efficiency and high power density.

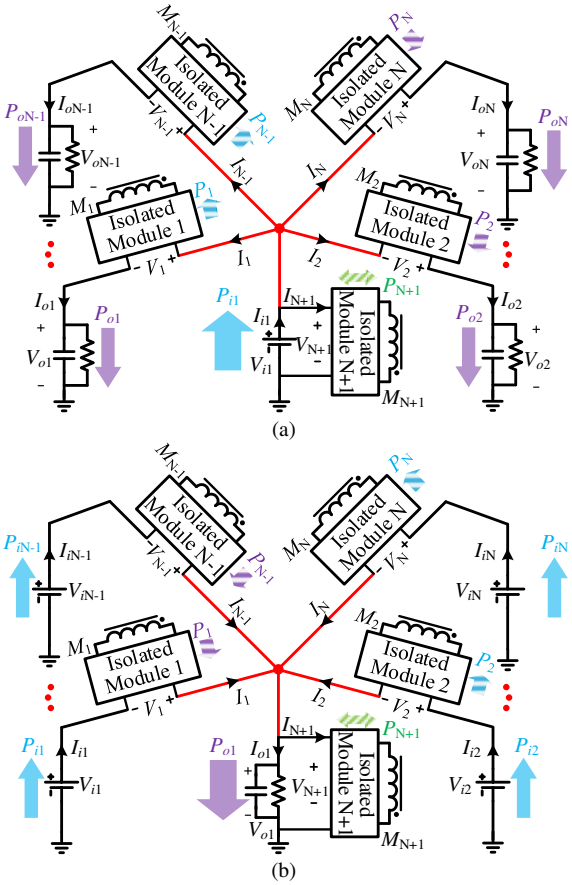

Fig. 2 The proposed PPP DC-DC architecture with radial module connections: (a) SIMO and (b) MISO.

Take Fig. 2 (a) as an example to explain the favorable PPP merit of the proposed architecture. The currents of the modules,

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output ports and input port are defined as I_1~I_{N+1}, I_{o1}~I_{oN} and I_{i1}, respectively. The power processed by module M_k(k=1, 2, …, N) is calculated in (1). When V_{ok}<V_{i1}, P_k flows out of the module. In contrast, P_k flows into the module when V_{ok}>V_{i1}. In addition, P_k is decreased with the output voltage V_{ok} approximating the input voltage V_{i1}. Therefore, if the values of V_{ok} and V_{i1} are similar, the required processing power of module M_k is small, and under this condition, the sum of output currents I_{o1}~I_{oN} is also near the input current I_{i1} according to the power balance principle. Hence, the power processed by module M_{N+1} is also small, as shown in (1). With different load conditions, P_{N+1} is bidirectional. The ratio of the module power P_p to the total system power P_t is calculated in (2) by using absolute values. According to (2), the power ratio P_p/P_t changing with output currents I_{o1} and I_{o2} is demonstrated in Fig. 3, where the per-unit current is set as 2.5A with example system parameters V_{i1}=400V, V_{o1}=320V and V_{o2}=480V. The maximum value 0.25 is achieved for P_p/P_t when I_{o2}=0A, which is much smaller than 1. Moreover, a minimum value of 0.1 is obtained when (V_{i1}-V_{o1})×I_{o1} equals (V_{o2}-V_{i1})×I_{o2}. Therefore, only a small part of the power needs to be processed by modules M_1~M_{N+1}, especially when the difference between the input voltage and output voltage is small. Consequently, the voltage or current stresses of the components in these modules are successfully reduced, contributing to low cost and high power density.

$$\begin{cases} P_k = V_k I_k = (V_{i1} - V_{ok}) I_{ok}, k = 1, 2..., N \\ P_{N+1} = V_{N+1} I_{N+1} = V_{i1} (I_{i1} - \sum_{k=1}^{N} I_{ok}) \end{cases} \tag{1}$$

$$\frac{P_p}{P_t} = \frac{\sum_{k=1}^{N} |P_k| + |P_{N+1}|}{\sum_{k=1}^{N} |P_{ok}| + |P_{i1}|} = \frac{\sum_{k=1}^{N} |V_{i1} - V_{ok}| I_{ok} + V_{i1} \left| I_{i1} - \sum_{k=1}^{N} I_{ok} \right|}{2 V_{i1} I_{i1}} \tag{2}$$

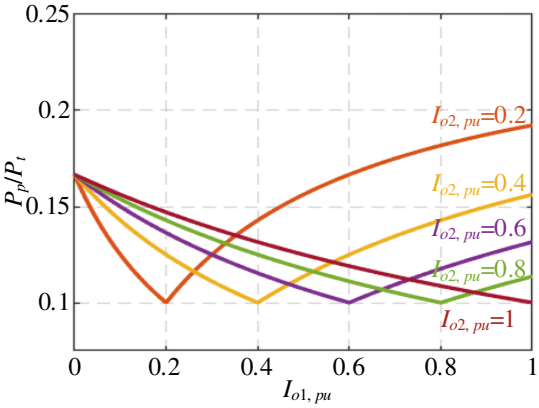

Fig. 3 The relationship among output currents I_{o1}, I_{o2} and the power ratio P_p/P_t.

Due to the PPP ability, the efficiency of the proposed multiport architecture will also be high. Define the power transmission efficiency of the modules and the PPP converter as η_p and η_t, respectively. Because only the partial power is processed by modules, while the other is delivered directly through wire with near 100% efficiency, the total efficiency η_t are calculated in (3). From (3), η_t is always larger than η_p since P_p is smaller than P_t. Moreover, the smaller the ratio P_p to P_t is, the higher the global efficiency η_t that can be attained.

$$\eta_t = \frac{P_p \eta_p + P_t - P_p}{P_t} = \eta_p + \frac{(P_t - P_p)(1 - \eta_p)}{P_t} > \eta_p \tag{3}$$

III. Operational Principle of an Example Active Bridge Module-Based PPP-SIDO DC-DC Converter

To better understand the operation principle of the proposed PPP multiport DC-DC architecture with radial module connections in Fig. 2, a SIDO example with three active bridge modules M_1~M_3 as in Fig. 4 will be introduced in detail. It has an input port V_{i1}, two output ports V_{o1}~V_{o2}, and it is assumed

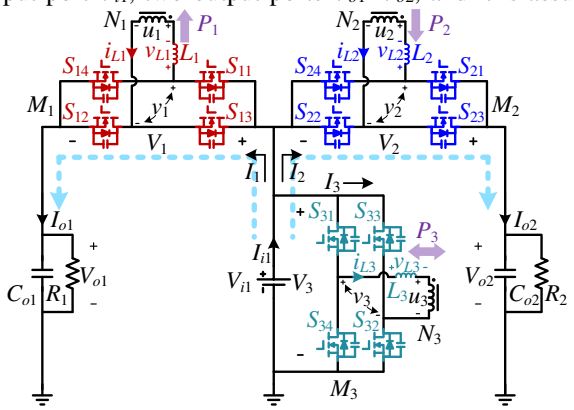

Fig. 4 Circuit diagram of the proposed active bridge module-based PPP-SIDO DC-DC converter.

that V_{o1}<V_{i1}<V_{o2}. Each module M_i(i=1, 2, 3) consists of four switches S_{i1}~S_{i4}(i=1, 2, 3), an inductor L_i(i=1, 2, 3) and a winding of the transformer with turn numbers N_i(i=1, 2, 3). M_1 and M_2 are connected in series, and M_3 is connected in parallel with V_{i1}. In addition, the positive terminal of M_1 and the negative terminal of M_2 are connected to the positive terminal of M_3. Owing to this structure, only a small partial power P_1~P_3 is converted through modules M_1~M_3, while the other large part of the power is delivered directly from V_{i1} to V_{o1} and V_{o2}.

From Fig. 4, the structure of the three-winding transformer with series inductors is depicted in Fig. 5(a). To conveniently calculate the inductor voltage v_{Li}(i=1, 2, 3), the corresponding star-equivalent transformation is given in Fig. 5(b) [31], where v'_2=v_2×N_1/N_2, v'_3=v_3×N_1/N_3, L'_2=L_2×N_1^2/N_2^2 and L'_3=L_3×N_1^2/N_3^2, which represent the primary referred values of voltages v_2 and v_3, and the inductances L_2 and L_3, respectively. Based on Fig. 5(b) and the superposition theorem, the voltages $u_i(t)$(i=1, 2, 3) are calculated in (4), where the voltage $v_i(t)$(i=1, 2, 3) is decided by switch modes, as shown in (5). When switch S_{i1} is turned on, $v_i(t)$=V_i, while $v_i(t)$=-V_i when S_{i1} is turned off. According to (4) and (5), the inductor voltages $v_{Li}(t)$=$v_i(t)$-$u_i(t)$(i=1, 2, 3) are finally calculated in (6).

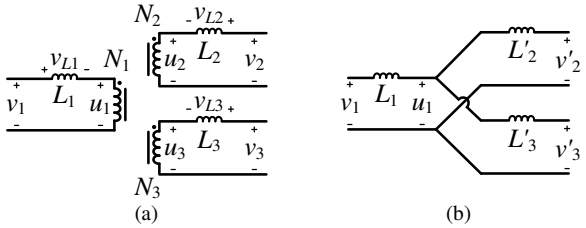

Fig. 5 The structure of a three-winding transformer with series inductors: (a) the re-depicted structure and (b) its star-equivalent model[31].

$$\begin{bmatrix} u_1(t) \\ u_2(t) \\ u_3(t) \end{bmatrix} = \begin{bmatrix} m_1 & m_2N_{12} & m_2N_{13} \\ m_1N_{21} & m_2 & m_3N_{23} \\ m_1N_{31} & m_2N_{32} & m_3 \end{bmatrix} \begin{bmatrix} v_1(t) \\ v_2(t) \\ v_3(t) \end{bmatrix} \tag{4}$$

where $m_1 = \dfrac{L_2'L_3'/(L_2'+L_3')}{L_1+L_2'L_3'/(L_2'+L_3')}$, $m_2 = \dfrac{L_1L_3'/(L_1+L_3')}{L_2+L_1L_3'/(L_1+L_3')}$, $m_3 = \dfrac{L_1L_2'/(L_1+L_2')}{L_3+L_1L_2'/(L_1+L_2')}$ and $N_{xy} = N_x/N_y, (x, y = 1,2,3)$.

$$\begin{cases} v_i(t) = q_i(t) \times V_i, \ i = 1,2,3 \\ q_i(t) = \begin{cases} 1, S_{i1} = on \\ -1, S_{i1} = off \end{cases} \end{cases} \tag{5}$$

$$v_{Li}(t) = q_i(t)V_i - \sum_{k=1}^{3} \frac{N_i}{N_k} m_k q_k(t) V_k, (i = 1,2,3) \tag{6}$$

The key operation waveforms of the active bridge module-based PPP-SIDO DC-DC converter are shown in Fig. 6. The drive signals of switches S_{i1}~S_{i4}(i=1, 2, 3) are v_{gsi1}~v_{gsi4}(i=1, 2, 3), respectively, as shown in Fig. 6. S_{i1} and S_{i2} are switched synchronously, as are S_{i3} and S_{i4}. Moreover, S_{i1} and S_{i3} are activated in complementary fashion with a 0.5 duty cycle. The phase shift angles of v_{gs21} and v_{gs31} with respect to v_{gs11} are defined as φ_{12} and φ_{13}, respectively. The phase shift angles φ_{12} and φ_{13} in radians are employed to regulate the power flows among the three modules M_1~M_3.

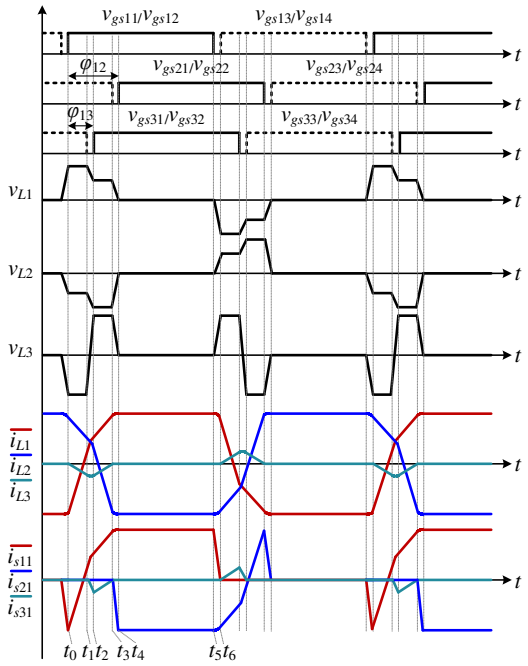

Fig. 6 Key operation waveforms of the proposed active bridge module-based PPP-SIDO DC-DC converter.

From Fig. 6, the half switching period T_s/2 of v_{gs11} can be divided into six states (t_0~t_6) with phase shift relationships $\pi/2>\varphi_{12}>\varphi_{13}>0$. The corresponding values of $q_i(t)$(i=1, 2, 3) in different states are given in TABLE I and the equivalent circuits of six states (t_0~t_6) are also shown in Fig. 7. In addition, assume N_1:N_2:N_3=V_1:V_2:V_3 and N_1^2:N_2^2:N_3^2=L_1:L_2:L_3 so that m_1~m_3 in (6) are all equal to 1/3, which largely simplifies the calculation and analysis.

TABLE I
VALUES OF $q_i(t)$(i=1, 2, 3) IN DIFFERENT STATES

Value	(t_0~t_1)	(t_2~t_3)	(t_4~t_5)
$q_1(t)$	1	1	1
$q_2(t)$	-1	-1	1
$q_3(t)$	-1	1	1

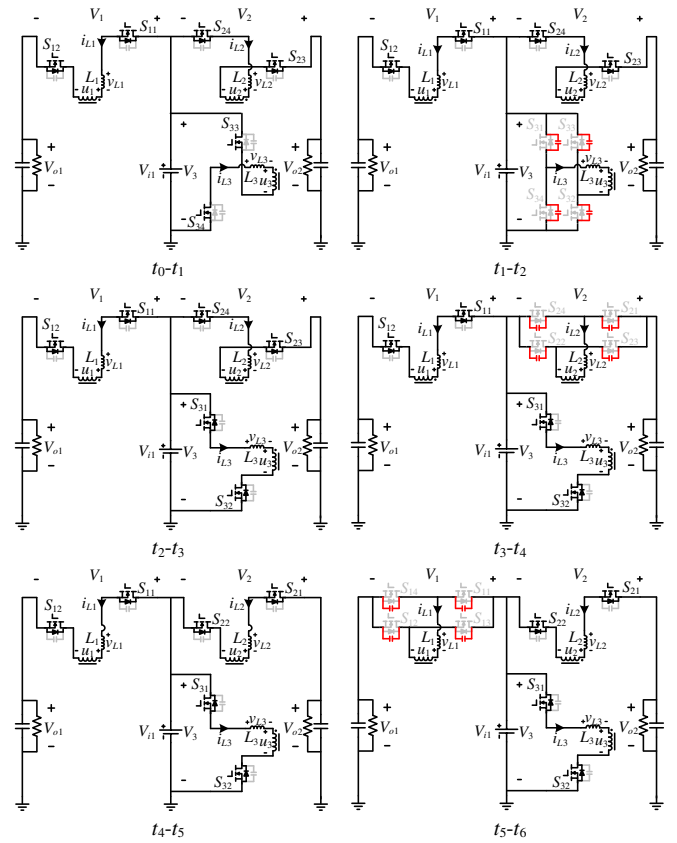

Fig. 7 The equivalent circuits of six states t_0-t_6.

State 1 (t_0~t_1): S_{11} and S_{12} are turned on at t_0. In addition, S_{23}, S_{24}, S_{33} and S_{34} also remain conducting in this state. According to (6) and TABLE I, the three inductor voltages are v_{L1}= 4×V_1/3, v_{L2}=-2×V_2/3 and v_{L3}=-2×V_3/3. Hence, the inductor current i_{L1} increases, while i_{L2} and i_{L3} decrease linearly, as calculated in (7). Accordingly, V_{i1} charges V_{o1}, V_{o2} and L_1 at the same time, while inductors L_2 and L_3 are discharged.

$$\begin{cases} i_{L1}(t) = i_{L1}(t_0) + \dfrac{4}{3} \cdot \dfrac{V_1}{L_1}(t - t_0) \\ i_{L2}(t) = i_{L2}(t_0) - \dfrac{2}{3} \cdot \dfrac{V_2}{L_2}(t - t_0) \\ i_{L3}(t) = i_{L3}(t_0) - \dfrac{2}{3} \cdot \dfrac{V_3}{L_3}(t - t_0) \end{cases} \tag{7}$$

State 2 (t_1~t_2): S_{33} and S_{34} are turned off at t_1. Subsequently, the inductor L_3 starts to resonate with the parasitic capacitors C_{s31}~C_{s34} of switches S_{31}~S_{34}, as illustrated in (8), where the drain-to-source voltages $v_{s31}(t)$ and $v_{s32}(t)$ are decreased.

$$\begin{cases} (C_{s31} + C_{s34}) \dfrac{dv_{s31}(t)}{dt} = (C_{s32} + C_{s33}) \dfrac{dv_{s32}(t)}{dt} = i_{L3}(t) \\ -L_3 \dfrac{di_{L3}(t)}{dt} = v_{s31}(t) + v_{s32}(t) + u_3(t) - V_3 \end{cases} \tag{8}$$

State 3 (t_2~t_3): After discharging of C_{s31} and C_{s32}, the body diodes of switches S_{31} and S_{32} conduct; thereby, their drain-to-source voltages are clamped to zero. Switches S_{31} and S_{32} are turned on at t_2, which indicates that zero-voltage-switching (ZVS) turn-on is achieved. In this state, v_{L1} =2×V_1/3, v_{L2} =-4×V_2/3 and v_{L3} =2×V_3/3. The corresponding inductor currents are given in (9). Therefore, V_{o1}, V_{o2}, L_1 and L_3 are charged by V_{i1}, while L_2 is discharged.

$$\begin{cases} i_{L1}(t)=i_{L1}(t_0)+\dfrac{4}{3}\cdot\dfrac{V_1}{L_1}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s+\dfrac{2}{3}\cdot\dfrac{V_1}{L_1}(t-t_1) \\ i_{L2}(t)=i_{L2}(t_0)-\dfrac{2}{3}\cdot\dfrac{V_2}{L_2}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s-\dfrac{4}{3}\cdot\dfrac{V_2}{L_2}(t-t_1) \\ i_{L3}(t)=i_{L3}(t_0)-\dfrac{2}{3}\cdot\dfrac{V_3}{L_3}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s+\dfrac{2}{3}\cdot\dfrac{V_3}{L_3}(t-t_1) \end{cases} \tag{9}$$

State 4 (t_3~t_4): S_{23} and S_{24} are turned off at t_3, and the resonance among inductor L_2 and parasitic capacitors C_{s21}~C_{s24} begins. The resonance formula is depicted in (10), where C_{s21} and C_{s22} are discharged, while C_{s23} and C_{s24} are charged.

$$\begin{cases} (C_{s21}+C_{s24})\dfrac{dv_{s21}(t)}{dt}=(C_{s22}+C_{s23})\dfrac{dv_{s22}(t)}{dt}=i_{L2}(t) \\ -L_2\dfrac{di_{L2}(t)}{dt}=v_{s21}(t)+v_{s22}(t)+u_2(t)-V_2 \end{cases} \tag{10}$$

State 5 (t_4~t_5): When $v_{s21}(t)$ and $v_{s22}(t)$ drop to zero, the corresponding body diodes conduct; therefore, these two drain-to-source voltages are clamped to zero before t_4. ZVS turn-on of switches S_{21} and S_{22} is realized when they are turned on at t_4. Subsequently, the inductor voltages are all changed to zero such that their inductor currents are constant, as shown in (11). In this state, V_{i1} only charges V_{o1} and V_{o2}.

$$\begin{cases} i_{L1}(t)=i_{L1}(t_0)+\dfrac{4}{3}\cdot\dfrac{V_1}{L_1}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s+\dfrac{2}{3}\cdot\dfrac{V_1}{L_1}\dfrac{(\varphi_{12}-\varphi_{13})}{2\pi}\cdot T_s \\ i_{L2}(t)=i_{L2}(t_0)-\dfrac{2}{3}\cdot\dfrac{V_2}{L_2}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s-\dfrac{4}{3}\cdot\dfrac{V_2}{L_2}\dfrac{(\varphi_{12}-\varphi_{13})}{2\pi}\cdot T_s \\ i_{L3}(t)=i_{L3}(t_0)-\dfrac{2}{3}\cdot\dfrac{V_3}{L_3}\cdot\dfrac{\varphi_{13}}{2\pi}\cdot T_s+\dfrac{2}{3}\cdot\dfrac{V_3}{L_3}\dfrac{(\varphi_{12}-\varphi_{13})}{2\pi}\cdot T_s \end{cases} \tag{11}$$

State 6 (t_5~t_6): S_{11} and S_{12} are turned off at t_5. Parasitic capacitors C_{s11} and C_{s12} are charged during resonance, as calculated in (12). Because C_{s11} and C_{s12} are charged, the drain-to-source voltages $v_{s11}(t)$ and $v_{s12}(t)$ are increased. When v_{gs13} and v_{gs14} turn positive at t_6, the half switching period ends.

$$\begin{cases} (C_{s11}+C_{s14})\dfrac{dv_{s13}(t)}{dt}=(C_{s12}+C_{s13})\dfrac{dv_{s14}(t)}{dt}=-i_{L1}(t) \\ L_1\dfrac{di_{L1}(t)}{dt}=v_{s13}(t)+v_{s14}(t)-u_1(t)-V_1 \end{cases} \tag{12}$$

IV. Characteristic Analysis and Design Consideration

Based on the operational principle of the proposed active bridge module-based PPP-SIDO DC-DC converter, the characteristics analysis and design considerations are introduced in this section with the system parameters in TABLE II. *Part A* calculates the active and non-active power flows based on three active bridge modules. *Part B* concentrates on partial power flow analysis of the proposed structure. Subsequently, hardware design considerations will be given in *Part C* based on voltage and current stresses, working areas, and ZVS operation. In addition, small signal modeling and control design are depicted in *Part D*. Finally, the comparison is made in *Part E* among the typical triple active bridge (TAB) converter [31, 32], an existing three-port PPP converter based on TAB [33] and the proposed example active bridge module-based PPP-SIDO converter. The characteristics of the proposed converter are also summarized.

TABLE II
SYSTEM PARAMETERS

Parameter	Value	Parameter	Value
Input Voltage V_{i1}	400V	Output Current $I_{o1,max}$	2.5A
Output Voltage V_{o1}	320V	Output Current $I_{o2,max}$	2.5A
Output Voltage V_{o2}	480V	Turns Ratio N_1:N_2:N_3	1:1:5
Switching Period T_s	10μs	Series Inductance Ratio L_1:L_2:L_3	1:1:25

A. Active and Non-active Power Flow Calculation

The three active bridge modules in the proposed example PPP-SIDO converter construct a TAB converter. From [31, 32], active power flows P_1, P_2 and P_3 of the three modules are calculated in (13), where P_{12}, P_{13} and P_{23} are virtual power flows according to the triangle-equivalent model, as shown in Fig. 8. Based on (13), (14) and the system parameters in TABLE II, phase shift angles ϕ_{12} and ϕ_{13} under different I_{o1} and I_{o2} are illustrated in Fig. 9, where ϕ_{12} and ϕ_{13} are the angles corresponding to radians φ_{12} and φ_{13}. Therefore, the power flows of the proposed active bridge module-based PPP-SIDO DC-DC converter can be effectively controlled by phase shift angles φ_{12} and φ_{13}.

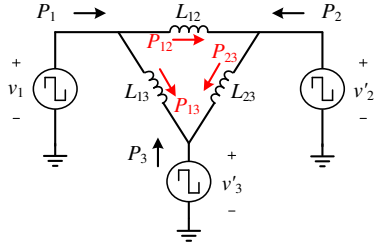

Fig. 8 Triangle-equivalent model[31] of the three-winding transformer with series inductors in Fig. 5.

$$\begin{cases} P_1=P_{12}+P_{13}=I_{o1}(V_{i1}-V_{o1}) \\ P_2=P_{21}+P_{23}=I_{o2}(V_{i1}-V_{o2}) \\ P_3=P_{31}+P_{32}=-P_1-P_2 \end{cases} \tag{13}$$

$$\begin{cases} P_{12}=-P_{21}=\dfrac{V_1V_2N_1}{N_2\omega L_{12}}\varphi_{12}\left(1-\dfrac{|\varphi_{12}|}{\pi}\right) \\ P_{13}=-P_{31}=\dfrac{V_1V_3N_1}{N_3\omega L_{13}}\varphi_{13}\left(1-\dfrac{|\varphi_{13}|}{\pi}\right) \\ P_{23}=-P_{32}=\dfrac{V_2V_3N_1^2}{N_2N_3\omega L_{23}}(\varphi_{13}-\varphi_{12})\left(1-\dfrac{|\varphi_{13}-\varphi_{12}|}{\pi}\right) \end{cases} \tag{14}$$

where $\omega_s=2\pi/T_s$ and $\begin{cases} L_{12}=L_1+L_2'+L_1L_2'/L_3' \\ L_{13}=L_1+L_3'+L_1L_3'/L_2' \\ L_{23}=L_2'+L_3'+L_2'L_3'/L_1 \end{cases}$.

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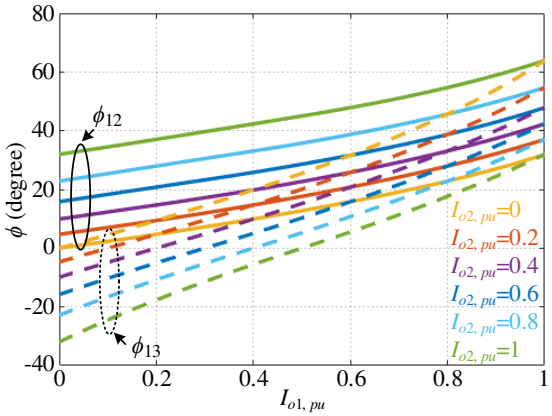

Fig. 9 Graph showing the change of phase shift angles ϕ_{12}, ϕ_{13} with loads I_{o1}, I_{o2}.

In addition to the active power P_1~P_3 calculated in (13), the non-active power is also considered. Owing to the square waveforms of $v_1(t)$, $v'_2(t)$ and $v'_3(t)$ in Fig. 8, they can be transformed universally based on a Fourier series [34], as shown in (15). Subsequently, we can obtain the equivalent inductor currents $i_{L12}(t)$, $i_{L13}(t)$ and $i_{L23}(t)$ in (16). Considering the symmetry of TAB in one switching cycle, the average current of the inductors over one switching period should be zero in the steady state, and we have formula (17). According to (15), (16) and (17), the Fourier series expression of the inductor currents is derived in (18). The expressions of the port currents $i_1(t)$, $i'_2(t)$ and $i'_3(t)$ are given in (19). Afterward, the average power, i.e., the active power $P_i(i=1,2,3)$ of three

$$\begin{cases} v_1(t)=\sum\limits_{n=1,3,5...}\dfrac{4V_1}{n\pi}\cdot\sin(n\omega_s t) \\ v'_2(t)=\sum\limits_{n=1,3,5...}\dfrac{4V'_2}{n\pi}\cdot\sin\left(n(\omega_s t-\varphi_{12})\right) \\ v'_3(t)=\sum\limits_{n=1,3,5...}\dfrac{4V'_3}{n\pi}\cdot\sin\left(n(\omega_s t-\varphi_{13})\right) \end{cases} \tag{15}$$

$$\begin{cases} i_{L12}(t)-i_{L12}(0)=\int_0^t\dfrac{v_1(t)-v'_2(t)}{L_{12}}dt \\ i_{L13}(t)-i_{L13}(0)=\int_0^t\dfrac{v_1(t)-v'_3(t)}{L_{13}}dt \\ i_{L23}(t)-i_{L23}(0)=\int_0^t\dfrac{v'_2(t)-v'_3(t)}{L_{23}}dt \end{cases} \tag{16}$$

$$i_{Lxy}\left(\frac{\pi}{\omega_s}\right)=-i_{Lxy}(0),(x,y=1,2,3) \tag{17}$$

modules M_1~M_3 during one switching period is described in (20). Taking P_3 as an example, its expression is shown in (21). In addition, the product of the two sinusoids is shown in (22). According to the orthogonality of the trigonometric function, the second integral expression in (21) is equal to zero because m≠n. The expression of the active power P_3 is derived in (23). Similarly, from (15), (19) and (20), the active powers $P_i(i=1,2,3)$ are finally derived in (24).

$$\begin{cases} i_{L12}(t)=\sum\limits_{n=1,3,5...}\dfrac{4}{n^2\pi\omega_s L_{12}}\cdot\left[-V_1\cos(n\omega_s t)+V'_2\cos(n\varphi_{12})\cos(n\omega_s t)+V'_2\sin(n\varphi_{12})\sin(n\omega_s t)\right] \\ i_{L13}(t)=\sum\limits_{n=1,3,5...}\dfrac{4}{n^2\pi\omega_s L_{13}}\cdot\left[-V_1\cos(n\omega_s t)+V'_3\cos(n\varphi_{13})\cos(n\omega_s t)+V'_3\sin(n\varphi_{13})\sin(n\omega_s t)\right] \\ i_{L23}(t)=\sum\limits_{n=1,3,5...}\dfrac{4V'_2}{n^2\pi\omega_s L_{23}}\cdot\left[-\cos(n\varphi_{12})\cos(n\omega_s t)-\sin(n\varphi_{12})\sin(n\omega_s t)-2\cos(n\varphi_{12})\right] \\ \qquad +\sum\limits_{n=1,3,5...}\dfrac{4V'_3}{n^2\pi\omega_s L_{23}}\left[\cos(n\varphi_{13})\cos(n\omega_s t)+\sin(n\varphi_{13})\sin(n\omega_s t)+2\cos(n\varphi_{13})\right] \end{cases} \tag{18}$$

$$\begin{cases} i_1(t)=i_{L12}(t)+i_{L13}(t)=\sum\limits_{n=1,3,5...}\dfrac{4}{n^2\pi\omega_s}\cdot\sqrt{A_1^2+B_1^2}\sin\left(n\omega_s t+\arctan\dfrac{A_1}{B_1}\right) \\ i'_2(t)=-i_{L12}(t)+i_{L23}(t)=\sum\limits_{n=1,3,5...}\dfrac{4}{n^2\pi\omega_s}\cdot\left(\sqrt{A_2^2+B_2^2}\sin\left(n\omega_s t+\arctan\dfrac{A_2}{B_2}\right)+C\right) \\ i'_3(t)=-i_{L13}(t)-i_{L23}(t)=\sum\limits_{n=1,3,5...}\dfrac{4}{n^2\pi\omega_s}\cdot\left(\sqrt{A_3^2+B_3^2}\sin\left(n\omega_s t+\arctan\dfrac{A_3}{B_3}\right)-C\right) \end{cases} \tag{19}$$

where

$C=\dfrac{-2V'_2\cos(n\varphi_{12})+2V'_3\cos(n\varphi_{13})}{L_{23}}$	$A_1=\dfrac{-V_1+V'_2\cos(n\varphi_{12})}{L_{12}}+\dfrac{-V_1+V'_3\cos(n\varphi_{13})}{L_{13}}$	$B_1=\dfrac{V'_2\sin(n\varphi_{12})}{L_{12}}+\dfrac{V'_3\sin(n\varphi_{13})}{L_{13}}$
$A_2=\dfrac{-V'_2\cos(n\varphi_{12})+V'_3\cos(n\varphi_{13})}{L_{23}}+\dfrac{V_1-V'_2\cos(n\varphi_{12})}{L_{12}}$		$B_2=\dfrac{-V'_2\sin(n\varphi_{12})+V'_3\sin(n\varphi_{13})}{L_{23}}+\dfrac{-V'_2\sin(n\varphi_{12})}{L_{12}}$
$A_3=\dfrac{V_1-V'_3\cos(n\varphi_{13})}{L_{13}}+\dfrac{V'_2\cos(n\varphi_{12})-V'_3\cos(n\varphi_{13})}{L_{23}}$		$B_3=\dfrac{-V'_3\sin(n\varphi_{13})}{L_{13}}+\dfrac{V'_2\sin(n\varphi_{12})-V'_3\sin(n\varphi_{13})}{L_{23}}$

$$P_i=\frac{1}{T_s}\int_0^{T_s}\left(\sum_{n=1,3,5...} v_i(nt)i_i(nt)+\sum_{m\neq n} v_i(mt)i_i(nt)\right)dt \quad (20)$$

$$P_3=\frac{1}{T_s}\int_0^{T_s}\left(\sum_{n=1,3,5...}\frac{16V_3'}{n^3\pi^2\omega_s}X_3(t)+\sum_{m\neq n}\frac{16V_3'}{mn^2\pi^2\omega_s}X_3(t)\right)dt \quad (21)$$

where

$$X_3=\sin\left(m\omega_s t-m\varphi_{13}\right)\cdot\left(\sqrt{A_3^2+B_3^2}\cdot\sin\left(n\omega_s t+\arctan\frac{A_3}{B_3}\right)-C\right).$$

$$\sin(a)\cdot\sin(b)=\frac{1}{2}\left(\cos(a-b)-\cos(a+b)\right) \quad (22)$$

$$P_3=\sum_{n=1,3,5...}\frac{8V_3'\sqrt{A_3^2+B_3^2}}{n^3\pi^2\omega_s}\cdot\cos\left(\arctan\frac{A_3}{B_3}+n\varphi_{13}\right) \quad (23)$$

$$\begin{cases} P_{1,m=n}=\sum_{n=1,3,5...}\frac{8V_1\sqrt{A_1^2+B_1^2}}{n^3\pi^2\omega_s}\cdot\cos\left(\arctan\frac{A_1}{B_1}\right) \\ P_{2,m=n}=\sum_{n=1,3,5...}\frac{8V_2'\sqrt{A_2^2+B_2^2}}{n^3\pi^2\omega_s}\cdot\cos\left(\arctan\frac{A_2}{B_2}+n\varphi_{12}\right) \\ P_{3,m=n}=\sum_{n=1,3,5...}\frac{8V_3'\sqrt{A_3^2+B_3^2}}{n^3\pi^2\omega_s}\cdot\cos\left(\arctan\frac{A_3}{B_3}+n\varphi_{13}\right) \end{cases} \quad (24)$$

If the active power for TAB is expressed by (25), then the power factor λ=cos(ϕ) is used to indicate the phase differences between the voltage and current. The power factor λ=cos(ϕ) can be divided into two situations: a) For the current and voltage with the same order harmonic component, the power factor λ=cos(ϕ) is followed by (24). b) For the voltage and current with different order harmonic components, the active power is equal to 0 due to the orthogonality of the trigonometric function, which is cos(ϕ)=0.

$$\begin{cases} P=\sum_{n=1,3,5...}V(n)I(n)\cos(\phi)+\sum_{m\neq n}V(m)I(n)\cdot 0 \\ Q=\sum_{n=1,3,5...}V(n)I(n)\sin(\phi)+\sum_{m\neq n}V(m)I(n)\cdot 1 \end{cases} \quad (25)$$

Similarly, the reactive power can also be classified into two categories: 1) the reactive power caused by the voltage and current components with the same frequency, and 2) the reactive power caused by the voltage and current components with different frequencies. Based on (24) and (25), the first category of the reactive power is derived as (26). When m≠n, cos(ϕ)=0, while sin(ϕ)=1. The second category of the reactive power is shown in (27). Finally, the apparent power S_i(i=1,2,3) of each active bridge module M_i(i=1,2,3) is calculated in (28).

$$\begin{cases} Q_{1,m=n}=\sum_{n=1,3,5...}\frac{8V_1\sqrt{A_1^2+B_1^2}}{n^3\pi^2\omega_s}\cdot\sin\left(\arctan\frac{A_1}{B_1}\right) \\ Q_{2,m=n}=\sum_{n=1,3,5...}\frac{8V_2'\sqrt{A_2^2+B_2^2}}{n^3\pi^2\omega_s}\cdot\sin\left(\arctan\frac{A_2}{B_2}+n\varphi_{12}\right) \\ Q_{3,m=n}=\sum_{n=1,3,5...}\frac{8V_3'\sqrt{A_3^2+B_1^2}}{n^3\pi^2\omega_s}\cdot\sin\left(\arctan\frac{A_3}{B_3}+n\varphi_{13}\right) \end{cases} \quad (26)$$

$$\begin{cases} Q_{1,m\neq n}=\sum_{m\neq n}\frac{8V_1\sqrt{A_1^2+B_1^2}}{mn^2\pi^2\omega_s} \\ Q_{2,m\neq n}=\sum_{m\neq n}\frac{8V_2'\sqrt{A_2^2+B_2^2}}{mn^2\pi^2\omega_s} \\ Q_{3,m\neq n}=\sum_{m\neq n}\frac{8V_3'\sqrt{A_3^2+B_3^2}}{mn^2\pi^2\omega_s} \end{cases} \quad (27)$$

$$S_i=\sqrt{\sum_{m=n=1,3,5...}P_{i,m=n}^2+\sum_{m=n=1,3,5...}Q_{i,m=n}^2+\sum_{m\neq n=1,3,5...}Q_{i,m\neq n}^2} \quad (28)$$

B. PPP-based Power Flow Analysis

According to (1) and the system parameters in TABLE II, the relationships among output currents I_{o1} and I_{o2} and module powers P_1~P_3, i.e., partial powers, are presented in Fig. 10(a), where the per-unit current and power are respectively 2.5A and 2000W. From Fig. 10(a), P_1 is always positive, P_2 is negative, and P_3 is bidirectional, which is decided by load conditions. Their maximum absolute values are 200W, which is much smaller than the maximum output power P_{o1}=800W, P_{o2}=1200W and the maximum input power P_{i1}=2000W. In addition, Fig. 10(b) also demonstrates the partial power P_p and the total power P_t under different output currents I_{o1} and I_{o2} based on (2). Note that the partial power P_p processed by modules is effectively reduced in comparison with the total power P_t for any load condition.

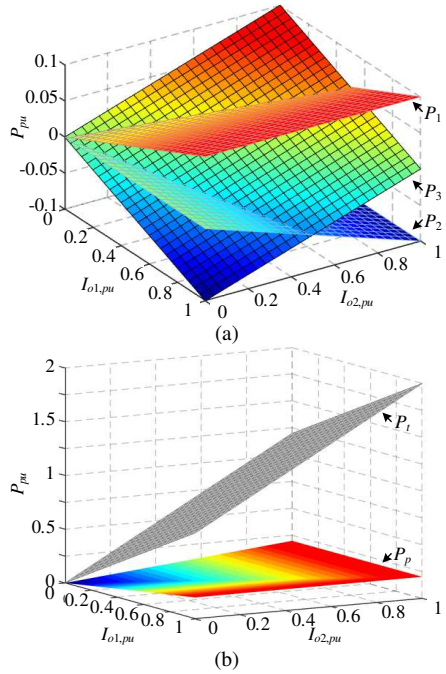

Fig. 10 Relationships among I_{o1}, I_{o2} and different power flows: (a) P_1~P_3 processed by modules M_1~M_3, and (b) partial power P_p and total power P_t.

In addition, according to (24), (26) and (28), both the sum of the partial active-power P_p=P_1+P_2+P_3 and partial apparent power S_p=S_1+S_2+S_3 processed by three isolated modules M_1~M_3 can be calculated after letting m and n take the values 1, 3, and 5, respectively. Subsequently, the curves of the partial power ratios P_p/P_t and S_p/P_t changing with the load currents I_{o1} and I_{o2}

are shown as in Fig. 11. To verify the theoretical analysis above, simulation results from PSIM are also presented in Fig. 11, showing that the theoretical results are in good agreement with the simulated results. In addition, the results calculated by Fourier series in Fig. 11(a) also match Fig. 3. Comparing Fig. 11(a) and Fig. 11(b), the changing trends of the active-power ratio P_p/P_t and apparent-power ratio S_p/P_t are similar. Therefore, the design consideration is similar.

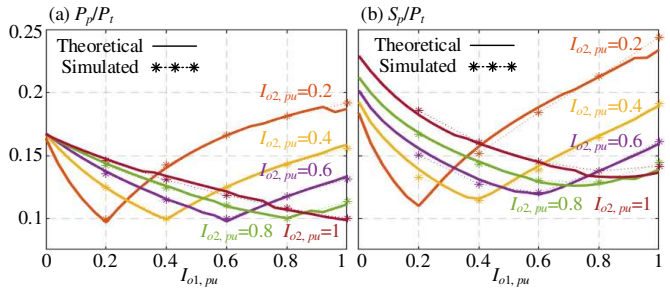

Fig. 11 Theoretical and simulated results of the power ratios changing with the load currents I_{o1} and I_{o2}: (a) P_p/P_t and (b) S_p/P_t.

C. Hardware Design Considerations

First, the current and voltage stresses are calculated. Due to symmetry, the absolute values of inductor currents $i_{Li}(t)$ and $i_{Li}(t+T_s/2)$ are equal, i.e., $i_{Li}(t_0)$=-$i_{Li}(t_6)$ in Fig. 6. According to (11), the inductor currents at t_0 are calculated in (29). Based on (29) and (7), the RMS currents $I_{si1,\mathrm{rms}}$ of switches S_{i1}(i=1, 2, 3) are calculated in (30). In addition, the corresponding voltage stresses are depicted in (31). In each active bridge module M_i(i=1, 2, 3), the current and voltage stresses of the four switches are equal. Accordingly, MOSFET IPW60R180P7 is chosen for switches S_{i1}~S_{i4} in the prototype circuit.

$$\begin{cases} i_{L1}(t_0)=\left(-\dfrac{1}{3}\varphi_{12}-\dfrac{1}{3}\varphi_{13}\right)\cdot\dfrac{V_1T_s}{2\pi L_1} \\ i_{L2}(t_0)=\left(\dfrac{2}{3}\varphi_{12}-\dfrac{1}{3}\varphi_{13}\right)\cdot\dfrac{V_2T_s}{2\pi L_2} \\ i_{L3}(t_0)=\left(-\dfrac{1}{3}\varphi_{12}+\dfrac{2}{3}\varphi_{13}\right)\cdot\dfrac{V_3T_s}{2\pi L_3} \end{cases} \tag{29}$$

$$I_{si1,rms}=\sqrt{\frac{3\pi-2\varphi_{12}}{6\pi}i_{Li}^2(t_0)+\frac{\varphi_{12}}{6\pi}i_{Li}^2(t_1)+\frac{2\varphi_{13}-\varphi_{12}}{6\pi}i_{Li}(t_0)i_{Li}(t_1)} \tag{30}$$

$$\begin{cases} V_{s11}=V_{i1}-V_{o1} \\ V_{s21}=V_{o2}-V_{i1} \\ V_{s31}=V_{i1} \end{cases} \tag{31}$$

The working areas and peak current are also considered. According to (13), (14) and the system parameters in TABLE II, the available ranges of power flows (P_1, P_2) in terms of the series inductance L_1 are generated in Fig. 12, where P_1 is always positive, while P_2 is negative. From Fig. 12, the smaller the inductance L_1 is, the larger the power range. On the other hand, the maximum absolute inductor currents $i_{L1,\max}$~$i_{L3,\max}$ in terms of series inductance L_1 are also depicted in Fig. 13 according to (32) and (35). They are decreased with the decrement of L_1, which adversely affects the realization of the ZVS operation of switches. Therefore, the series inductance L_1 is finally designated as 20μH after a comprehensive consideration of both the power range and ZVS operation.

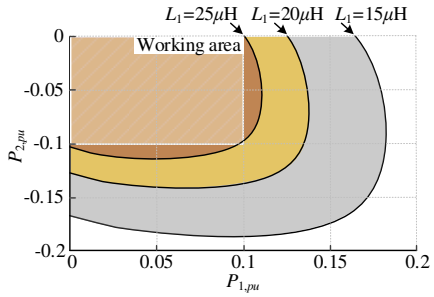

Fig. 12 The available range of power flow (P_1, P_2) in terms of inductance L_1.

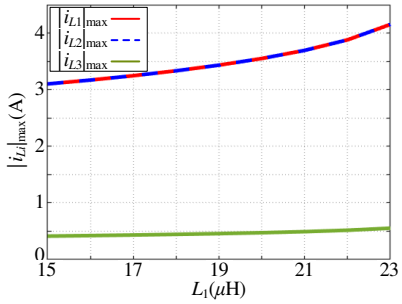

Fig. 13 The maximum absolute inductor currents $i_{L1,\max}$~$i_{L3,\max}$ in terms of series inductance L_1.

Finally, ZVS operation is designed. From the analysis in section III, switches S_{11}, S_{12}, S_{23}, S_{24}, S_{33} and S_{34} are turned on before t_1. The inductor current $i_{L3}(t_1)$ is calculated in (32) based on (7) and (29), which is negative. When S_{33} and S_{34} are turned off at t_1, the inductor L_3 will resonate with the parasitic capacitors C_{s31}~C_{s34}, as shown in Fig. 14. The capacitors C_{s31}~C_{s32} are discharged, while C_{s33}~C_{s34} are charged. From Fig. 14, the expression of $u_3(t)$ during t_1 to t_2 is calculated in (33) based on (4). Combining with (8), the drain-to-source voltage $v_{s31}(t)$ is calculated in (34).

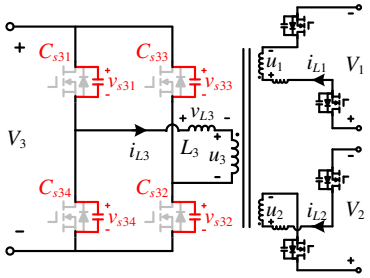

Fig. 14 Resonance process during t_1~t_2.

$$i_{L3}(t_1)=-\frac{1}{3}\varphi_{12}\cdot\frac{V_3T_s}{2\pi L_3}<0 \tag{32}$$

$$u_3(t)=\frac{N_3}{3}\left(V_1-\frac{V_2}{N_2}+\frac{-v_{s31}(t)+V_3-v_{s32}(t)}{N_3}\right) \tag{33}$$

$$v_{s31}(t)=A_{13}\cos\left(\omega_3(t-t_1)\right)+A_{23}\sin\left(\omega_3(t-t_1)\right)+A_{33} \tag{34}$$

where $A_{13}=\dfrac{V_3/3+N_3V_1/3}{C_sL_3\omega_3^2}$, $A_{23}=\dfrac{i_{L3}(t_1)}{\omega_3C_s}$, $A_{33}=V_3-A_{13}$, $\omega_3=\sqrt{4/(3C_sL_3)}$.

Similarly, the inductor currents $i_{L2}(t_3)$ and $i_{L1}(t_5)$ are calculated in (35) so that they are negative and positive, respectively. Therefore, resonances also occur in modules M_2 and M_1 during t_3~t_4 and t_5~t_6, respectively. During resonances,

the parasitic capacitors C_{s21} and C_{s13} are discharged, and the corresponding drain-to-source voltages $v_{s21}(t)$ and $v_{s13}(t)$ are also calculated in (36).

$$\begin{cases} i_{L2}(t_3)=\left(-\frac{2}{3}\varphi_{12}+\frac{1}{3}\varphi_{13}\right)\cdot\frac{V_2T_s}{2\pi L_2}<0 \\ i_{L1}(t_5)=\left(\frac{1}{3}\varphi_{12}+\frac{1}{3}\varphi_{13}\right)\cdot\frac{V_1T_s}{2\pi L_1}>0 \end{cases} \tag{35}$$

$$\begin{cases} v_{s21}(t)=A_{12}\cos\left(\omega_2(t-t_3)\right)+A_{22}\sin\left(\omega_2(t-t_3)\right)+A_{32} \\ v_{s13}(t)=A_{11}\cos\left(\omega_1(t-t_5)\right)+A_{21}\sin\left(\omega_1(t-t_5)\right)+A_{31} \end{cases} \tag{36}$$

where $A_{12}=\frac{V_2/3+N_2V_1}{C_sL_2\omega_2^2}$, $A_{22}=\frac{i_{L2}(t_3)}{\omega_2C_s}$, $A_{32}=V_2-A_{12}$, $A_{11}=0$, $A_{21}=\frac{-i_{L1}(t_5)}{\omega_1C_s}$, $A_{31}=V_1$, $\omega_2=\sqrt{\frac{4}{3C_sL_2}}$, $\omega_1=\sqrt{\frac{4}{3C_sL_1}}$.

According to (34), (36) and the system parameters in TABLE II, the drain-to-source voltages $v_{s13}(t)$, $v_{s21}(t)$ and $v_{s31}(t)$ are shown in Fig. 15. From Fig. 15, both $v_{s13}(t)$ and $v_{s21}(t)$ can drop to zero quickly. After they drop to zero, their body diodes will conduct; therefore, the ZVS turn-on of switches S_{13} and S_{21} is realized if their drive signals turn positive. Nevertheless, $v_{s31}(t)$ decreases slowly and requires a large amount of time to reach zero, which is much larger than the practical dead time. To improve this, an inductor L_4 is added to connect with the drain terminals of switches S_{32} and S_{34}. Accordingly, the resonance expression of $v_{s31}(t)$ is changed from (34) to (37), where $i_{L4}(t_1)<0$. Because $B_1>A_{13}$, while $B_2<A_{23}$, $v_{s31}(t)$ drops faster after adding the parallel inductor L_4, which is also shown in Fig. 15. The ZVS turn-on of switch S_{31} can also be obtained. With the decrease in L_4, the resonance time will be reduced, but the extra conduction losses will increase. Therefore, the inductance L_4 is finally designed as 300μH after establishing a trade-off between the ZVS realization and conduction loss.

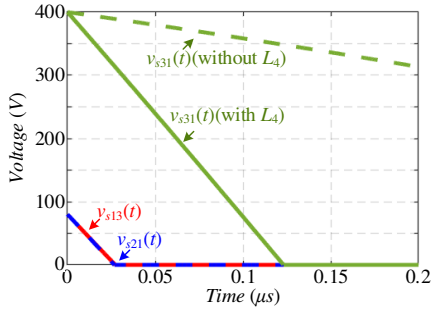

Fig. 15 Resonance waveforms of drain-to-source voltages v_{s13}, v_{s21} and v_{s31}.

$$v_{s31}(t)=B_1\cos\left(\omega_3(t-t_1)\right)+B_2\sin\left(\omega_3(t-t_1)\right)+B_3 \tag{37}$$

where $B_1=\left(N_3V_1/3+(1/3+L_3/L_4)V_3\right)/\left(L_3C_3\omega_3^2\right)$, $B_3=V_3-B_1$, $B_2=\left(i_{L3}(t_1)+i_{L4}(t_1)\right)/(\omega_3C_s)$, $i_{L4}(t_1)=-V_3T_s/(4L_4)$.

The deadtime is set to 0.167μs, and the ZVS operation fails if $v_{s13}(t)$, $v_{s21}(t)$ and $v_{s31}(t)$ cannot drop to zero before the deadtime end. Based on (36), (37) and the system parameters, the ZVS ranges within load conditions I_{o1}=0~2.5A and I_{o2}=0~2.5A are presented in Fig. 16, where the per-unit current is set as 2.5A. From Fig. 16, switches in modules M_1 and M_2 will lose the ZVS operation under light loads. Switches in M_3 can always realize ZVS operation throughout the load ranges.

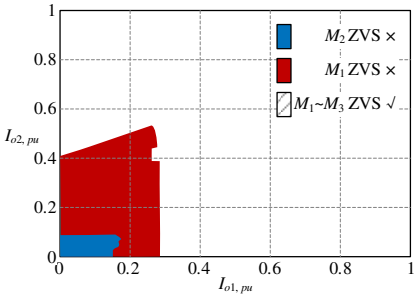

Fig. 16 ZVS ranges of switches in isolated modules M_1~M_3.

D. Small Signal Modeling and Control Design

In addition to steady-state analysis, the dynamic characteristic of the proposed example active bridge module-based PPP-SIDO DC-DC converter is also explained by small signal modeling in this section. Subsequently, the control scheme is designed.

According to the operational principle, the average state space equation of the proposed PPP-SIDO converter is given in (38). The average values $\langle i_1(t)\rangle_{T_s}$ and $\langle i_2(t)\rangle_{T_s}$ need to be represented by other variables without substantial ripples, as shown in (39). These are derived from (13) and (14) by dividing power flows by voltages. Subsequently, average values equal to the corresponding quiescent values plus small AC variations are assumed, which are $\langle v_{o1}(t)\rangle_{T_s}=V_{o1}+\hat{v}_{o1}(t)$, $\langle v_{o2}(t)\rangle_{T_s}=V_{o2}+\hat{v}_{o2}(t)$, $\langle\phi_{12}(t)\rangle_{T_s}=\Phi_{12}+\hat{\phi}_{12}(t)$ and $\langle\phi_{13}(t)\rangle_{T_s}=\Phi_{13}+\hat{\phi}_{13}(t)$. Replacing these equations and (39) into (38), and neglecting both DC terms and higher-order nonlinear terms, we can obtain the small-signal model linearized equation in (40). In addition, after converting the expression from the time domain to the s domain, we output expressions related to the phase shift angles in (41) and the corresponding transfer functions in (42).

$$\begin{cases} C_{o1}\frac{d\langle v_{o1}(t)\rangle_{T_s}}{dt}=\langle i_1(t)\rangle_{T_s}-\frac{\langle v_{o1}(t)\rangle_{T_s}}{R_1} \\ C_{o2}\frac{d\langle v_{o2}(t)\rangle_{T_s}}{dt}=-\langle i_2(t)\rangle_{T_s}-\frac{\langle v_{o2}(t)\rangle_{T_s}}{R_2} \end{cases} \tag{38}$$

$$\begin{cases} \langle i_1(t)\rangle_{T_s}=f_1(v_{o2},v_{i1},\phi_{12},\phi_{13})=\frac{\langle v_{o2}(t)-v_{i1}(t)\rangle_{T_s}}{N_2\omega_sL_{12}}\cdot\frac{\phi_{12}(t)\pi}{180^\circ}\cdot\left(1-\frac{\phi_{12}(t)}{180^\circ}\right)+\frac{\langle v_{i1}(t)\rangle_{T_s}}{N_3\omega_sL_{13}}\cdot\frac{\phi_{13}(t)\pi}{180^\circ}\cdot\left(1-\frac{\phi_{13}(t)}{180^\circ}\right) \\ \langle i_2(t)\rangle_{T_s}=f_2(v_{o1},v_{i1},\phi_{12},\phi_{13})=-\frac{\langle v_{i1}(t)-v_{o1}(t)\rangle_{T_s}}{N_2\omega_sL_{12}}\cdot\frac{\phi_{12}(t)\pi}{180^\circ}\cdot\left(1-\frac{\phi_{12}(t)}{180^\circ}\right)+\frac{\langle v_{i1}(t)\rangle_{T_s}\pi}{N_2N_3\omega_sL_{23}}\cdot\left|\frac{\phi_{13}(t)}{180^\circ}-\frac{\phi_{12}(t)}{180^\circ}\right|\cdot\left(1-\left|\frac{\phi_{13}(t)}{180^\circ}-\frac{\phi_{12}(t)}{180^\circ}\right|\right) \end{cases} \tag{39}$$

$$\begin{cases} C_{o1}\dfrac{d\hat{v}_{o1}(t)}{dt}+\dfrac{\hat{v}_{o1}(t)}{R_1}=k_1\hat{v}_{o2}(t)+k_2\hat{\phi}_{12}(t)+k_3\hat{\phi}_{13}(t) \\ C_{o2}\dfrac{d\hat{v}_{o2}(t)}{dt}+\dfrac{\hat{v}_{o2}(t)}{R_2}=-m_1\hat{v}_{o1}(t)-m_2\hat{\phi}_{12}(t)-m_3\hat{\phi}_{13}(t) \end{cases} \tag{40}$$

where
$$\begin{cases} k_1=\dfrac{df_1}{dv_{o2}}\Big|_{v_{o2}=V_{o2}}=\dfrac{\pi}{N_2\omega_s L_{12}}\cdot\left(\dfrac{\Phi_{12}}{180^\circ}-\dfrac{\Phi_{12}^2}{180^{\circ 2}}\right)=m_1 \\ k_2=\dfrac{df_1}{d\phi_{12}}\Big|_{\phi_{12}=\Phi_{12}}=\dfrac{(V_{o2}-V_{i1})\pi}{N_2\omega_s L_{12}}\cdot\left(\dfrac{1}{180^\circ}-\dfrac{2\Phi_{12}}{180^{\circ 2}}\right) \\ k_3=\dfrac{df_1}{d\phi_{13}}\Big|_{\phi_{13}=\Phi_{13}}=\dfrac{V_{i1}\pi}{N_3\omega_s L_{13}}\cdot\left(\dfrac{1}{180^\circ}-\dfrac{2\Phi_{13}}{180^{\circ 2}}\right) \\ m_2=\dfrac{df_2}{d\phi_{12}}\Big|_{\phi_{12}=\Phi_{12}}=\dfrac{(V_{o1}-V_{i1})\pi}{N_2\omega_s L_{12}}\cdot\left(\dfrac{1}{180^\circ}-\dfrac{2\Phi_{12}}{180^{\circ 2}}\right)+m_3 \\ m_3=\dfrac{df_2}{d\phi_{13}}\Big|_{\phi_{13}=\Phi_{13}}=\dfrac{V_{i1}\pi}{N_2N_3\omega_s L_{23}}\cdot\left(\dfrac{1}{180^\circ}-\dfrac{2(\Phi_{13}-\Phi_{12})}{180^{\circ 2}}\right) \end{cases}.$$

$$\begin{cases} \hat{v}_{o1}(s)=G_{vd12}\hat{\phi}_{12}(s)+G_{vd13}\hat{\phi}_{13}(s) \\ \hat{v}_{o2}(s)=G_{vd22}\hat{\phi}_{12}(s)+G_{vd23}\hat{\phi}_{13}(s) \end{cases} \tag{41}$$

$$\begin{cases} G_{vd12}=\hat{v}_{o1}(s)/\hat{\phi}_{12}(s)=\dfrac{A_1B_2+A_2B_0}{A_0B_0-A_1B_1} \\ G_{vd13}=\hat{v}_{o1}(s)/\hat{\phi}_{13}(s)=\dfrac{A_1B_3+A_3B_0}{A_0B_0-A_1B_1} \\ G_{vd22}=\hat{v}_{o2}(s)/\hat{\phi}_{12}(s)=\dfrac{A_2B_1+A_0B_2}{A_0B_0-A_1B_1} \\ G_{vd23}=\hat{v}_{o2}(s)/\hat{\phi}_{13}(s)=\dfrac{A_3B_1+A_0B_3}{A_0B_0-A_1B_1} \end{cases} \tag{42}$$

where $A_0=sC_{o1}+1/R_1$, $A_i=k_i(i=1,2,3)$, $B_0=sC_{o1}+1/R_1$, $B_i=-m_i(i=1,2,3)$.

The Bode plots of the control-to-output transfer functions are shown in Fig. 17(a) based on (42) and the system parameters in TABLE II. In addition, Fig. 17(b) also illustrates the Bode plots of the transfer functions from simulation software PSIM, which is basically consistent with the one obtained by the theoretical analysis in Fig. 17(a).

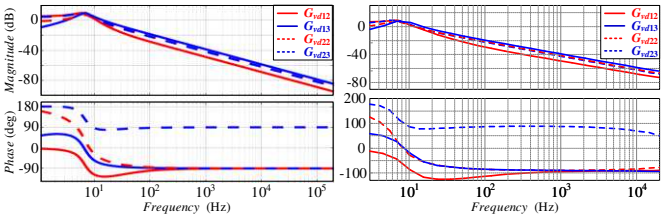

Fig. 17 Bode plots of the control-to-output transfer functions G_{vd12}, G_{vd13}, G_{vd22} and G_{vd23} obtained by (a) the theoretical analysis and (b) the simulation.

Subsequently, the control scheme is designed in Fig. 18, where constant voltage controls of V_{o1} and V_{o2} depend on ϕ_{12} and ϕ_{13}, respectively, with separate compensators. Note that the phase of G_{vd23} is larger than 0° from Fig. 17; therefore, the voltage error of the control system of output V_{o2} is designed as v_{o2}-V_{ref2} rather than V_{ref2}-v_{o2} to realize negative feedback closed loop control. According to the control-to-output transfer functions in Fig. 17 and the control scheme in Fig. 18, the compensators G_{c1} and G_{c2} are designed in (43). The open-loop G_{op1}= G_{vd12}×G_{c1} and -G_{op2}=-G_{vd23}×G_{c2} are presented in Fig. 19. From Fig. 19, both the magnitude values of G_{op1} and G_{op2} at 0 Hz are large due to their -20 dB/dec slopes. This indicates the errors between the real and reference output voltages can be eliminated. Moreover, the phase margins of G_{op1} and G_{op2} are approximately 90°, ensuring the stability of the closed-loop system. In addition, their crossover frequencies are approximately 300Hz, which contributes to quick responses. In other words, the closed-loop system obtains both good steady-state accuracy and dynamic performance after adding the compensators.

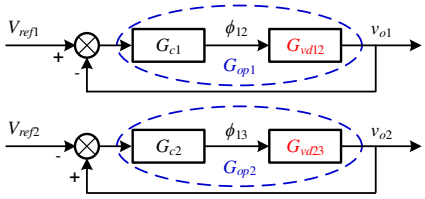

Fig. 18 The closed-loop control system with separate compensators.

$$\begin{cases} G_{c1}=\dfrac{120s+16000}{s} \\ G_{c2}=\dfrac{60s+6000}{s} \end{cases} \tag{43}$$

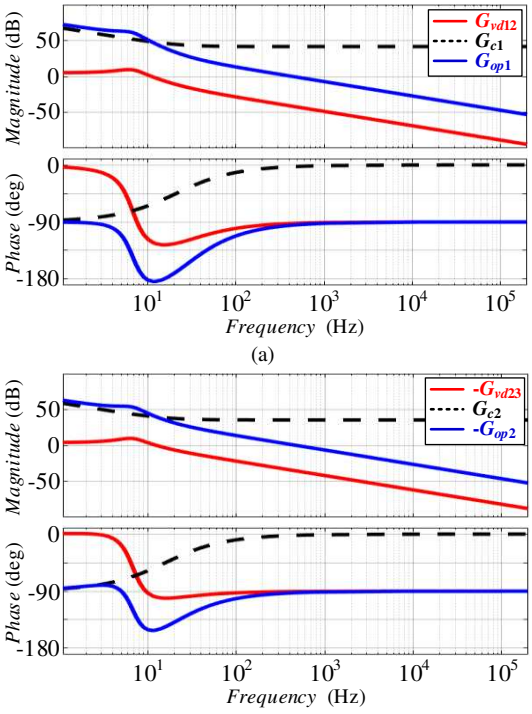

Fig. 19 Bode plots: (a) G_{vd12}, G_{c1}, G_{op1} and (b) -G_{vd23}, G_{c2}, -G_{op2}.

E. Comparison and Summary

A comparison is made among the typical TAB DC-DC converter [31, 32], the existing PPP three-port DC-DC converter based on TAB [33] and the proposed example active bridge module-based PPP-SIDO DC-DC converter. Their topologies are depicted in Fig. 20. In a conventional TAB converter, as shown in Fig. 20(a), this active bridge modules

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need to process the full power of the respective ports. The active bridge modules in the proposed PPP-SIDO converter only need to convert the partial power caused by voltage or current differences, which is depicted in (1). This is because these modules are series/parallel connected with output/input ports in the proposed topology, as depicted in Fig. 20(c). Taking the parameters in TABLE II as an example, the power processed by each module in two topologies can be calculated in TABLE III. It is obvious that the voltage/current stresses of both the semiconductors and magnetic components in the three modules of the proposed topology (c) are successfully reduced, and the small power rating components can be chosen so that the volume and costs can be reduced. Moreover, the conduction losses are reduced, which contributes to a high efficiency. In addition, the proposed structure can be further expanded to multiport while maintaining PPP according to Fig. 2. In contrast, topology (a) must process full power, and topology (b) can only realize PPP between two ports. Finally, the overall comparison among the three topologies is summarized in TABLE IV.

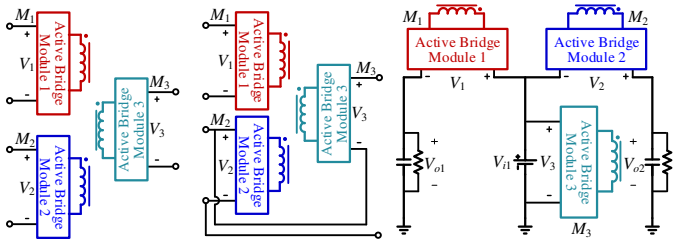

Fig. 20 Active bridge module-based topologies: (a) typical TAB[31, 32], (b) the existing PPP three-port DC-DC converter based on TAB[33], and (c) the proposed example active bridge module-based PPP-SIDO DC-DC converter.

TABLE III
STRESS COMPARISON OF THE THREE MODULES BETWEEN TOPOLOGIES (A) AND (C) IN FIG. 20

Module Stresses	Topology (a)	Topology (c)
Power (W)	P_1=800 P_2=1200 P_3=2000	P_1=200 P_2=200 P_3=0
Voltages(V)	V_1=320 V_2=480 V_3=400	V_1=80 V_2=80 V_3=400
Current (A)	I_1=2.5 I_2=2.5 I_3=5	I_1=2.5 I_2=2.5 I_3=0

TABLE IV
COMPARISON OF ACTIVE BRIDGE MODULE-BASED TOPOLOGIES IN FIG. 20

Topology	Ability to Realize PPP	Module Stress	Costs	Power Density
(a)	No	Large	Large	Low
(b)	Only two-port	Medium	Medium	Medium
(c)	Multiport	Small	Small	High

V. EXPERIMENTAL VERIFICATION

Based on the system parameters and design in section IV, a prototype circuit is set up, as shown in Fig. 21. The experimental waveforms of port voltages V_{i1}, V_{o1}, V_{o2}, and module voltages V_1~V_3 of M_1~M_3 are depicted in Fig. 22. From Fig. 22, the output voltages V_{o1} and V_{o2} are regulated to 320V and 480V, respectively. The module voltage V_3 of M_3 is equal

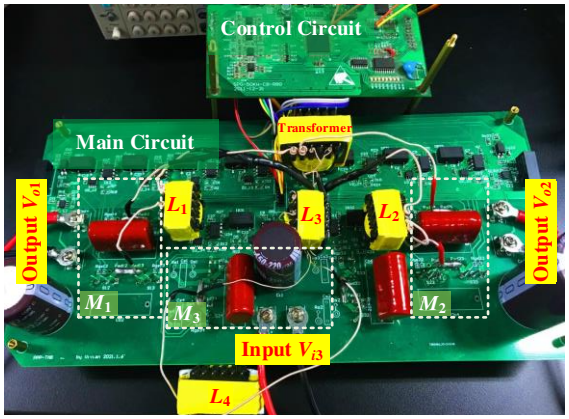

Fig. 21 Photograph of the prototype circuit.

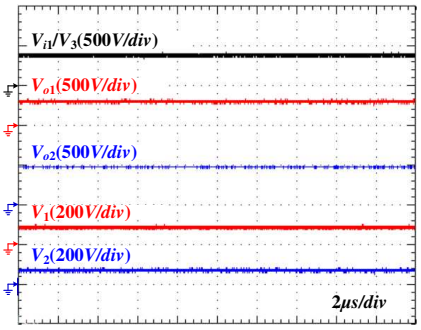

Fig. 22 Experimental waveforms of port voltages V_{i1}, V_{o1}, V_{o2}, and module voltages V_1~V_3.

to the input voltage V_{i1}=400V. The module voltages $V_{1,2}$ of $M_{1,2}$ are 80V, which is the difference between the input and output voltages. Therefore, the voltage stresses of modules $M_{1,2}$ are effectively reduced in the proposed converter.

In addition, Fig. 23~Fig. 25 demonstrate key experimental waveforms and ZVS realization under three conditions of (I_{o1}, I_{o2}), which are (2.5A, 2.5A), (2.5A, 0.5A) and (0.5A, 2.5A), respectively. According to Fig. 23(a)~Fig. 25(a), the phase shifts ϕ_{12} and ϕ_{13} are (63.9°, 31.95°), (37°, 54.7°) and (37°, -17.6°), respectively, which coincide well with Fig. 9. Moreover, with the measured values of I_{i1}, I_{o1}, and I_{o2}, the average current I_3 of module M_3, which is equal to I_{i1}-I_{o1}-I_{o2}, is 0A, -0.4A and 0.4A under three load conditions. Therefore, the current stress of module M_3 is also reduced in the proposed converter when compared with the conventional TAB converter.

Moreover, from Fig. 23(b), the inductor current i_{L1} is negative before switch S_{11} is turned on. Hence, the parasitic capacitor of switch S_{11} will be discharged, and its drain-to-source voltage v_{s11} will be decreased after S_{13} is turned off. When v_{s11} decreases to zero, the inductor current i_{L1} will flow through the source terminal to the drain terminal of switch S_{11}. Afterward, the ZVS operation of S_{11} is achieved with its drive signal becoming positive. Similarly, from Fig. 23(c)~ Fig. 23(d), Fig. 24(b)~Fig. 24(d) and Fig. 25(b)~Fig. 25(d), all the switches can successfully achieve ZVS operation under these three load conditions. Comparing Fig. 23~Fig. 25, the maximum absolute value of the inductor currents i_{L1} is increased with the rising load currents I_{o1}; therefore, the ZVS operation of switches in module M_1 is correspondingly easier. Module M_2 obtains a similar trend when I_{o2} increases. On the other hand, the ZVS

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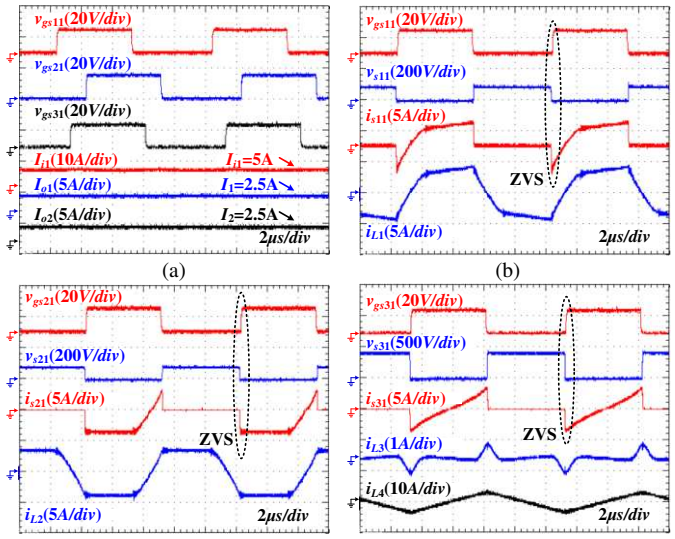

Fig. 23 Key experimental waveforms under load conditions I_{o1}=2.5A, I_{o2}=2.5A.

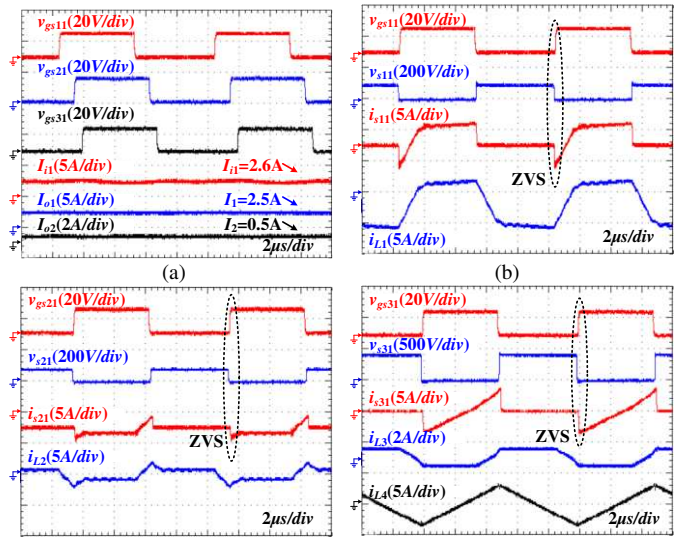

Fig. 24 Key experimental waveforms under load conditions I_{o1}=2.5A, I_{o2}=0.5A.

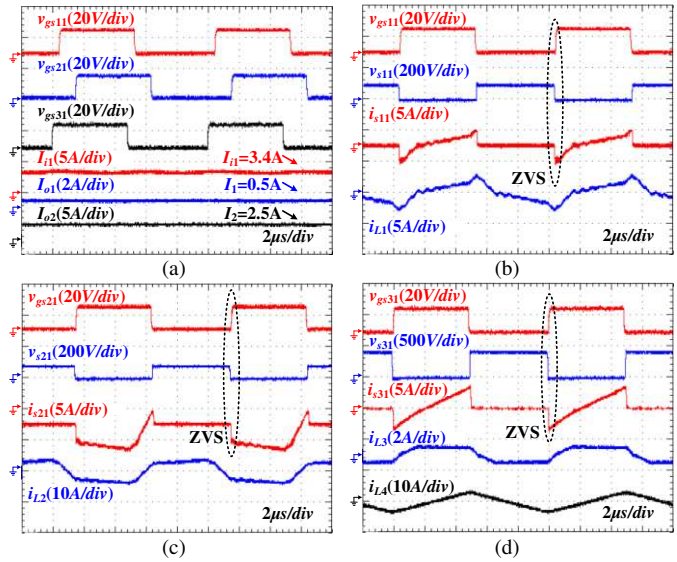

Fig. 25 Key experimental waveforms under load conditions I_{o1}=0.5A, I_{o2}=2.5A.

operation of switches in module M_3 is almost unaffected by load conditions because it is mainly influenced by the additional inductor current i_{L4} rather than i_{L3}.

In addition, the dynamic response under the output resistance variation is presented in Fig. 26. From Fig. 26, as the output resistances change, the output voltages fluctuate at first and they will return to the rated values quickly.

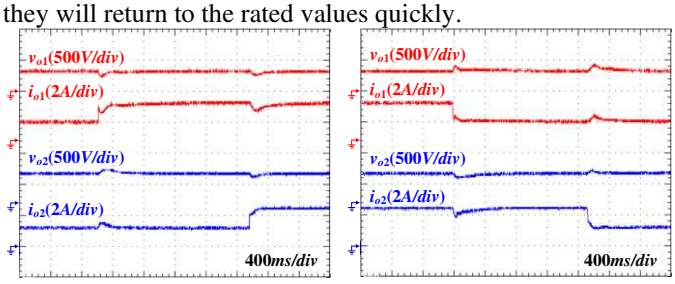

Fig. 26 Dynamic response when output resistance R_1 is changed between 256Ω and 128Ω, and R_2 is changed between 384Ω and 192Ω, respectively.

According to the measured module voltages $V_{1\sim3}$ and average module current $I_{1\sim3}$, the corresponding powers (P_1, P_2, P_3) being processed by three modules M_1~M_3 are equal to (200W, -200W, 0W), (200W, -40W, -160W) and (40W, -200W, 160W), respectively, under three load conditions (2.5A, 2.5A), (2.5A, 0.5A) and (0.5A, 2.5A). They only account for 10%, 19.23% and 14.7% of the practical power of the input and output ports, and the remaining power is transferred from input to output directly. Therefore, their corresponding efficiencies are high at 98.87%, 98.40% and 98.86%, respectively. In the prototype circuit, the power loss is mainly caused by conduction losses of both semiconductors and magnetic components, while switching loss and magnetic core loss can almost be ignored entirely due to the realization of ZVS and small magnetizing current. To justify the efficiencies, the detailed loss analysis of three load conditions (I_{o1}, I_{o2})=(2.5A, 2.5A)/(2.5A, 0.5A)/(0.5A, 2.5A) is conducted as follows:

According to Fig. 6, (30) and the system parameters in TABLE II, we can obtain the root mean square (RMS) current values of switches $I_{si1,\mathrm{rms}}$ (i=1, 2, 3) under three load conditions in (44). The RMS values of the series and parallel connected inductor currents $I_{Li,\mathrm{rms}}$ (i=1, 2, 3) and $I_{L4,\mathrm{rms}}$ can also be obtained in (45) and (46), respectively.

$$\begin{cases} I_{s11,rms} = 2.21A/2.17A/0.62A \\ I_{s21,rms} = 2.21A/0.62A/2.17A \\ I_{s31,rms} = 0.12A/0.34A/0.34A \end{cases} \tag{44}$$

$$I_{Li,rms} = \sqrt{2}\cdot I_{si1,rms} \tag{45}$$

$$I_{L4,rms} = \frac{1}{\sqrt{3}}\cdot\frac{V_3 T_s}{4L_4} = 1.92A \tag{46}$$

Based on the datasheet of MOSFET IPW60R180P7, the drain-to-source on-state resistance is R_{ds}=0.18Ω. Therefore, the conduction losses of switches under three load conditions are calculated in (47). In addition, because the three windings of the transformer are in series with inductors L_1~L_3, their sums of

resistances are R_{m1}=0.33Ω, R_{m2}=0.31Ω, and R_{m3}=6.98Ω, respectively. The resistance of the parallel connected inductor L_4 is R_{L4}=0.74Ω. The conduction losses of the magnetic components under three load conditions are obtained in (48). According to (47) and (48), the sum of the conduction losses is $P_{c,loss}$=17.81W/13.42W/13.25W. We can thus obtain estimated efficiencies of 99.11%/98.71%/99.03%. Compared with the measured efficiencies of 98.87%/ 98.40%/98.86%, the estimated efficiencies are basically consistent with the measured efficiencies. Their small differences are caused by other losses and measurement errors.

$$P_{s,loss} = 4 \cdot R_{ds} \cdot \left[I_{s1,rms}^2 + I_{s2,rms}^2 + \left(I_{s3,rms} + \frac{1}{\sqrt{2}} I_{L4,rms} \right)^2 \right] \quad (47)$$
$$= 8.62W / 5.74W / 5.74W$$

$$P_{L,loss} = \sum_{i=1}^{3} R_{mi} I_{Li,rms}^2 + R_{L4} I_{L4,rms}^2 \quad (48)$$
$$= 9.19W / 7.68W / 7.51W$$

In addition, the efficiencies over the full-load range are measured and presented in Fig. 27. Owing to the realization of partial power processing, power ratings over the whole load range are small; therefore, the losses are relatively small. As a result, the measured efficiencies are high over the whole load range, and the minimum efficiency reaches 98.13%.

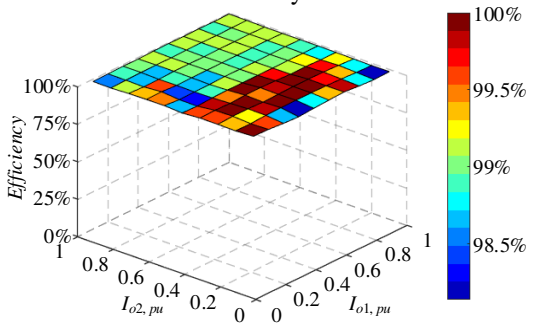

Fig. 27 Measured efficiencies of the proposed example active bridge module-based PPP-SIDO DC-DC converter over the whole load range.

VI. Conclusion

In this paper, a generalized PPP multiport DC-DC architecture with radial module connections is proposed for SIMO and MISO applications. This successfully expands PPP from two ports to multiple ports. In the proposed architecture, only the partial power generated by voltage or current differences between input and output will be processed by modules, while the other power will be transmitted directly. Therefore, a high power density and high global efficiency are obtained. Moreover, the magnetically linked modules can be implemented by using many various isolated converters. An example PPP-SIDO DC-DC converter with three active bridge modules M_1~M_3 is analyzed in detail in the paper, to gain a better understanding. The voltage stresses are effectively reduced in modules M_1~M_2, while the current stress is reduced in M_3. Therefore, a small power rating and high efficiency are obtained, which is effectively verified by the experimental results.

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