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Modular design of a three-level SiC MOSFET power module for more-electric aircraft applications

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Abstract

In this article, a three-level neutral point clamped inverter design for more-electric aircraft applications is presented. The power losses were calculated by building an accurate electrical model and comparing the efficiency and power density of the inverter when connected with different numbers of MOSFETs in parallel per switch. The steady-state and transient thermal models were established by means of the Finite Element Method (FEM) for thermal analysis. The thermal effects when different numbers of MOSFETs in parallel under different air mass flow rate conditions are also obtained.

1 Introduction

With more countries committed to achieving carbon neutrality by the middle of the century, a significant increase in electrification is considered essential to achieving increased efficiency and reduced environmental in the aviation industry. Most of the power electronics converters in aircraft currently use DC power supplies of 270V, and power levels usually not exceeding the tens of kWs. Due to the simple structure and easy control of the two-level converters, they are widely used in the power electronics drive systems in aircraft actuation, pumps, and compressors. As the trend toward the "more-electric aircraft" continues with significantly higher power levels in the future, it is expected that the voltage level will exceed the current 270V and reach $\pm$540/1080V, and that the power range will increase from kW to MW. The electric propulsion drives of MEA require lightweight and highly efficient power converters. Power electronics must minimise losses and maximise efficiency while minimising size and weight to achieve the high-power output required. Therefore, higher power density and reliability performances increase the demands on the electrical design and thermal management of power modules, a more precise design, and optimisation are needed [1]. Multi-level converters have several notable advantages in terms of output power quality, lower electromagnetic interference emissions, the ability to handle higher DC-link voltages with devices having lower voltage rating than a two-level converter, and the ability to produce output voltages with lower harmonic content when operated with the same switching frequency of a two-level converter. Better harmonic distortion with the same switching frequency also allows further benefits such as the reduction in size and cost of passive filtering components. A design of an active rectifier for a starter/generator with 400-A peak output current, 1.2-kV dc-link peak, was presented in [2]. A comparative analysis of two-level converters and three-level neutral point clamped (NPC) converters using off-the-shelf Si IGBTs, demonstrates that the three-level converter/rectifier produces lower losses. Coupled with lower harmonic distortion and EMI, the higher efficiency would make a three-level converter the optimal choice in this aircraft application. In the last decade, continuous advances to device properties have made Silicon carbide (SiC) MOSFETs the devices of choice for high-performance converters, thanks to the lower switching losses, faster switching speeds, and higher temperature operation compared to Si IGBTs [3]-[4].

Silicon Carbide (SiC) is a compound semiconductor material which is very stable thermally, chemically, and mechanically. The main advantages of SiC devices over Si devices are reduced energy losses during switching, easier miniaturisation, and greater resistance to high temperatures and voltages.

The switching losses of an all-SiC power module are much lower than those of an equivalent Si-IGBT module and the higher the switching frequency, the greater the difference in losses with the Si-IGBT module, which means that an all-SiC power module can not only reduce losses significantly but also achieve high switching speeds and therefore a reduction in the size of peripheral components. The lower resistance makes it easier to miniaturise; SiC MOSFETs have lower on-state resistance and can reduce the chip area by up to 1/10 the size of Si, which can reduce the size of modules.

Analyses presented in [5] for in a three-phase active rectifier application of a three-level converter with Vdc<1000V and switching frequency 15kHz, that the best efficiency is obtained when SiC MOSFETs are used. Although a converter can potentially be built with discrete devices, it is well known that the parasitic inductances that are inevitable in such a solution will significantly limit efficiency and degrade EMI emission. A converter based on integrated modules is therefore required in any high-performance application. At present, some hybrid modules with SiC diodes and Si IGBTs or a combination of Si IGBT and SiC diodes are available on the market. However, no three- or multi-level module based exclusively on SiC MOSFET is commercially available. This paper presents the design, efficiency, and thermal analysis for a 400A three-level

neutral point clamped (NPC) all SiC power module [6]. The suitable topology for an NPC converter is shown in Fig. 1.

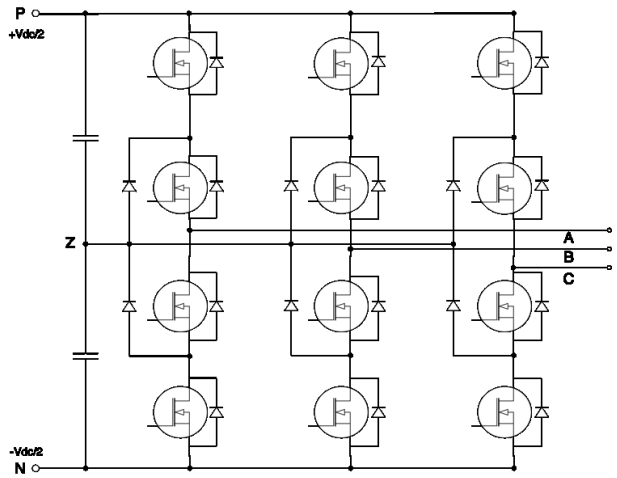

Fig. 1: Schematic of a three-level NPC inverter

The main electrical specifications of the designed power module are listed in Table 1 below.

Table 1 Main electrical specifications (per phase)

Parameter	Symbol	Value
DC-link voltage	V_{DC}	1080V
Devices switching frequency	f_{sw}	10kHz
Power factor	$\cos\varphi$	0-1
Load frequency	f_{load}	Max 2kHz
Amplitude modulation ratio	m	0-1
Output power	P_{out}	100kW
Output phase current	I_{load}	280A(rms)

A module layout has been designed with five MOSFETs dies and six diodes dies (per sub-module). However, the module design is modular to accommodate different power levels by increasing or decreasing the number of dies.

The modules have been manufactured, together with bespoke gate drives and assembled in a three-phase converter as shown in Fig 2. Details of the modules construction, layout, converter design and operation will be presented in a separate publication. This paper summarises the design decisions based on thermal and efficiency analyses.

This article is organised as follows: In section 2, the power loss values of each power device in the three-level NPC inverter are obtained by analysing the electrical model. On this basis, the efficiency and power density are calculated. In section 3, the steady-state and transient thermal responses are analysed by means of the finite element (FE) thermal model, and the thermal effects are compared under different conditions using the equivalent heat transfer coefficients obtained from the analytical model. Section 4 is a summary of this paper.

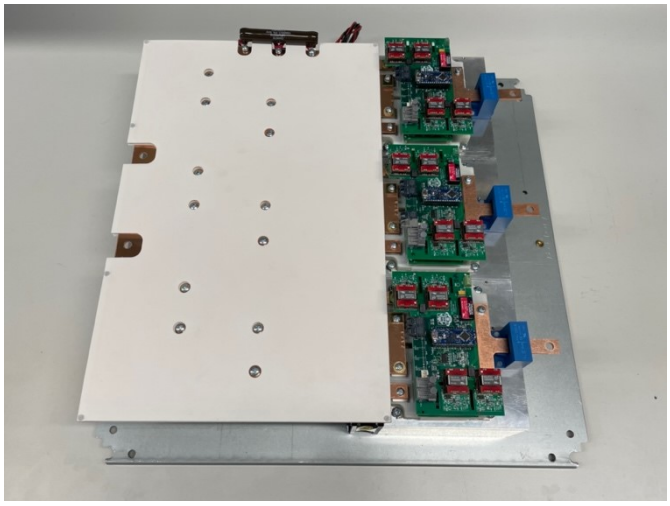

Fig. 2: Three-phase three-level converter built using the SiC modules described in the paper

2. Electrical loss model and simulation results

Detailed electrical simulations have been performed in MATLAB/Simulink to evaluate the performance of the converter and support the design of the module, e.g., identify the number of dies for the MOSFETs and diodes to parallel. Each MOSFET and diode is modelled using an accurate electrical model based on three-dimensional look-up tables representing the output characteristic drain-source current $I_{DS}(V_{DS}, V_{GS}, T.)$ as a function of drain-source V_{DS} and gate-source V_{GS} voltages and temperature T [7], device characteristics are obtained from datasheets: for the MOSFET Wolfspeed CPM3-1200-0013A, 13mΩ, 1200V device, and for the diodes CPW5-1200-Z050B 1200V, 50A. Power losses during conduction are computed by multiplying the voltage and the current in on-state. Therefore, the instantaneous value of the MOSFET conduction losses is:

$$p_{cond}(t) = u_{ds}(t) \cdot i_d(t) = R_{DSon}(i_{ds}) \cdot i_{ds}^2(t) \qquad (1)$$

Integration of the instantaneous power losses over the switching cycle gives an average value of the MOSFET conduction losses:

$$P_{cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_{cond}(t)dt$$
$$= \frac{1}{T_{sw}} \int_0^{T_{sw}} R_{DSon}(i) \cdot i_{ds}^2(t)\, dt = R_{DSon} \cdot I_{Drms}^2 \qquad (2)$$

As the current is distributed to each branch when different numbers of MOSFETs are connected in parallel, the total conduction losses are related to the drain current, the on-resistance, and the number of paralleled dies. Due to the dependence of conduction losses on power factor and modulation index, the conduction losses are compared at the same modulation index (m=1) and power factor 1 (unity) and 0 (lagging).

Switching losses are also independent of the inverter modulation index M and the load power factor (PF) [8] but

increase linearly with switching frequency. Conduction losses are not affected by f_{sw} but depend on the modulation index M and PF. Estimating the switching losses could be obtained by the approximation of the MOSFET and diode switching characteristics. A simpler way of calculating the switching losses is to utilize the switching energy-current (E-I) characteristic for on and off times. The switching losses can be calculated for the turn-on and turn-off energy in MOS and diodes as:

$$P_{sw} = P_{on+off} = \frac{1}{\pi} \cdot f_s \cdot [E_{on}(i) + E_{off}(i)] \qquad (3)$$

Where E_{on} is the on energy and E_{off} is the off energy, which is a function of the current, the total losses of MOSFETs are expressed as the sum of conduction and switching losses [9]. According to the electrical simulation results, Fig. 3 shows the relationship between the different losses and the number of paralleled SiC MOSFETs.

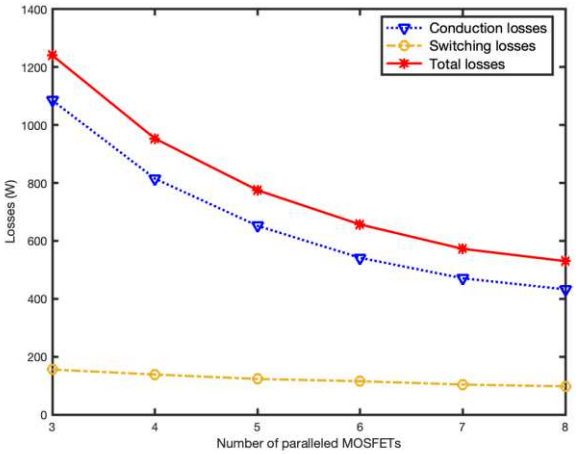

Fig. 3: Simscape model of a three-level NPC inverter

Table 2 shows the total losses in one phase/leg, including top/bottom MOSFETs, the middle MOSFETs, and the NPC diodes, for various numbers of MOSFETs and diodes dies in parallel per switch. The power density per chip calculated by using losses divided by volume is shown in Table 3.

To achieve sufficient efficiency, at least 5 MOSFETs in parallel per switch should be chosen. However, in the case of using six MOSFETs in parallel per switch, there is no significant relative increase in efficiency. A trade-off between efficiency and volume of power module needs to be considered.

Table 2 Losses for different numbers of MOSFETs in parallel (Device characteristics at T_j=125℃)

Losses per phase (W)	Total losses	Efficiency
3 MOSFETs per switch	1241.02	98.74%
4 MOSFETs per switch	991.52	98.98%
5 MOSFETs per switch	775.09	99.21%
6 MOSFETs per switch	656.64	99.33%
7 MOSFETs per switch	572.42	99.42%
8 MOSFETs per switch	530.08	99.46%

Table 3 Power density for different numbers of MOSFETs in parallel (Device characteristics at T_j=125℃)

Power density per chip ($W/m^3 \times 10^9$)	Top/Bottom MOSFETs	Middle MOSFETs	Diodes
3 MOSFETs per switch	14.45	19.95	2.707
4 MOSFETs per switch	8.750	11.48	2.696
5 MOSFETs per switch	5.529	7.412	2.844
6 MOSFETs per switch	3.963	5.164	2.800
7 MOSFETs per switch	3.030	3.997	2.789
8 MOSFETs per switch	2.477	3.241	2.724

3. Thermal model and simulation results

3.1 Thermal model

Establishing an accurate thermal model is critical to the electro-thermal design of the power module. For example, if a semiconductor device exceeds its maximum allowable junction temperature, it may result in functional failure [10]. This article presents an analytical simulation of the thermal model of a power module under different conditions by using the FEM. The finite element numerical analysis method can simulate the relationship between the thermal responses and the heat sources by means of many finite elements. Simulations are conducted using the FE tool ANSYS mechanical, and the boundary conditions are assumed iso-thermal at 80℃ on the heatsink top surface. A thermal interface material (TIM) Kerafol KERATHERM Thermal Pad 6.5W/mK is assumed between the module's baseplate and the heatsink since it can fill the gap between the module and the heatsink to ensure good heat transfer.

The vertical cross-section of the module and the material used are shown in Fig. 4 and Table 4, respectively. The losses calculated before are fed into a thermal finite element simulation using ANSYS. As the devices characteristics depend on temperature, an iterative process is necessary to evaluate the correct operating point. Some results are shown in Figs. 5-6, assuming an ambient temperature of 80℃. When using the losses calculated with the 125℃ devices characteristics, the maximum temperature is around 110℃ on top/bottom MOSFET, 121℃ on middle MOSFET, and 123℃ on the clamping diode. For reliability reasons, it would be desirable to restrict the maximum devices temperature to below 125℃.

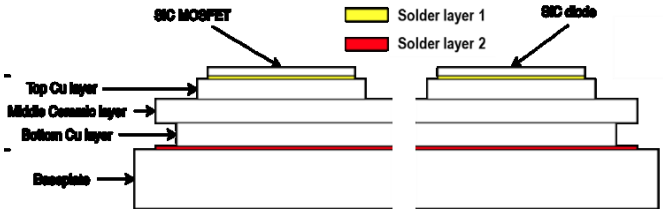

Fig. 4: Vertical cross-section of the module

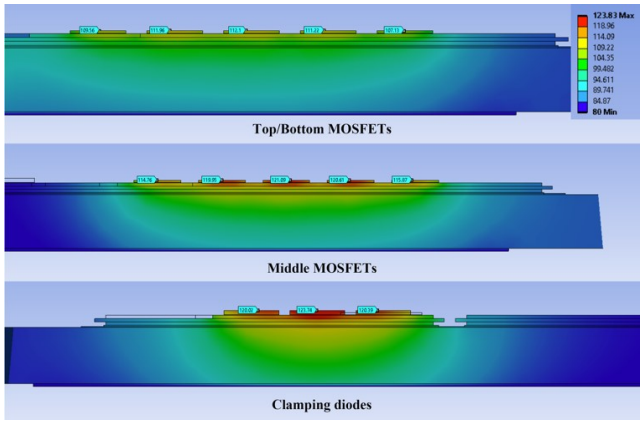

Fig. 5: Vertical temperature distribution of different devices

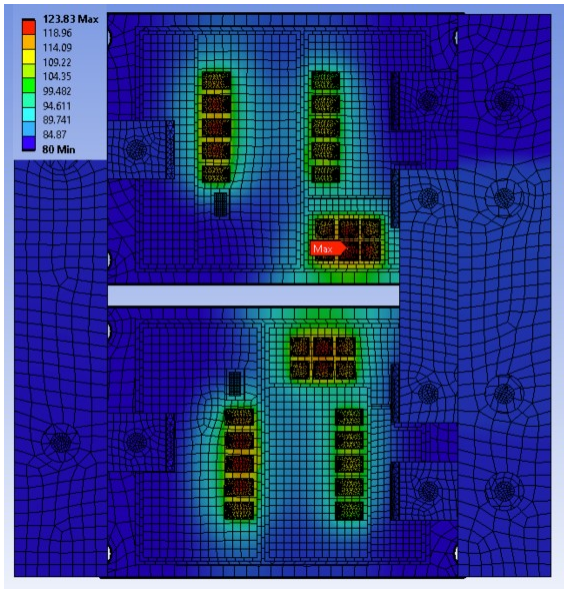

Fig. 6: Steady-state temperature distribution

The FE method allows to observe the transient response of the thermal model and thus extracts the parameters of the RC thermal network model for further thermal design, thermal management, life prediction, etc. [11]. Transient thermal simulations have been conducted to calculate the thermal impedance in a single-pulse case. Results are shown in Fig. 7 for the SiC MOSFETs.

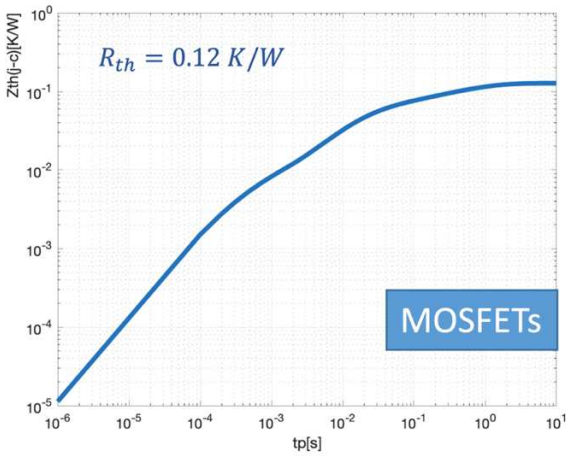

Fig. 7: Transient thermal responses for SiC MOSFET

3.2 Achievable power with forced air cooling

As liquid cooling is not generally allowed in aircraft applications of power electronics to reduce the weight and reliability of liquid cooling systems, power density achievable with the air cooling is evaluated in this section. Forced air convection in a parallel-plate finned heatsink, which is common in power electronics applications, is considered here. Fig. 8 shows the forced air-cooled system of the power module used in this study. Applying the analytical model in [12], it is possible to establish a functional relationship between heat transfer coefficients and the axial distance for the heatsink as a function of the air mass flow rate, which varies from 4g/s to 7g/s. The ANSYS mechanical simulation results are obtained by setting the heat transfer coefficients to the top surface of the heatsink as boundary conditions. Tables 5-7 summarise the temperatures of different devices at different air mass flow rates for different numbers of MOSFET paralleled.

From these tables, when only 3 or 4 MOSFETs are connected in parallel per switch, some of the devices generate high temperatures and are not suitable for use in practice. It is concluded that five MOSFETs in parallel would be required to meet this requirement with a sufficient safety margin. Table 8 shows the maximum power (one phase/leg) that can be achieved under different conditions at a fixed maximum permissible temperature of 125°C. Fig. 9 shows that the more devices are connected in parallel and the faster the air mass flow rate, the higher the power can be achieved.

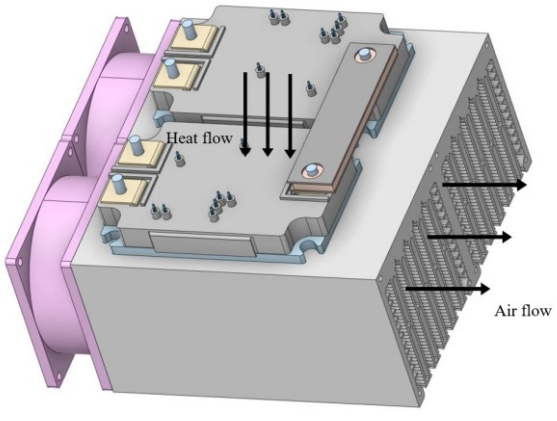

Fig. 8: 3D view of forced Air-cooled system

Table 5 Three MOSFETs per switch

Temperature (°C)	4g/s	5g/s	7g/s
Top MOSFETs	197.4	188.9	177.9
Bottom MOSFETs	175.4	166.8	155.5
Middle MOSFETs	223.5	213.1	201.3
Clamping diodes	150.3	141.9	131.0

Table 6 Four MOSFETs per switch

Temperature (°C)	4g/s	5g/s	7g/s
Top MOSFETs	152.7	146.1	136.9
Bottom MOSFETs	139.5	132.5	123.6
Middle MOSFETs	166.0	158.8	149.5
Clamping diodes	142.4	135.1	125.4

Table 7 Five MOSFETs per switch

Temperature (°C)	4g/s	5g/s	7g/s
Top MOSFETs	124.4	118.4	110.6
Bottom MOSFETs	115.9	110.0	101.9
Middle MOSFETs	133.0	126.8	118.9
Clamping diodes	133.4	127.2	118.7

Table 8 Maximum power at different conditions (per phase)

Achievable power (kW)	4g/s	5g/s	7g/s
3 MOSFETs per switch	79.98	84.40	90.05
4 MOSFETs per switch	112.59	118.65	127.51
5 MOSFETs per switch	146.45	155.34	169.07

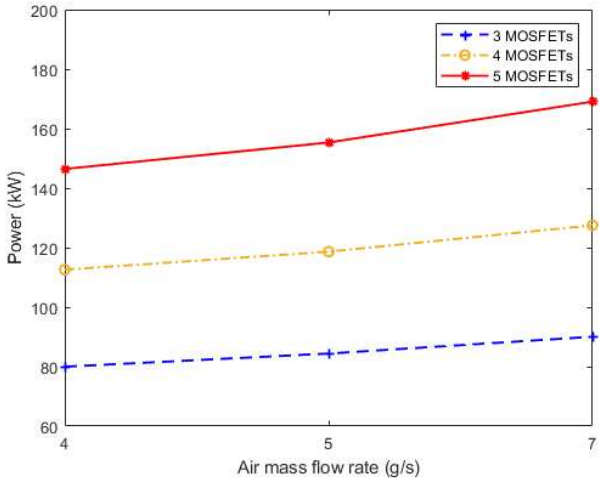

Fig. 9: Achievable power at different conditions (per phase)

3.3 CFD simulation of cooling systems

In section 3.2, the temperature is obtained from the given heat transfer coefficient in the analytical model by using the FE method. In this section, the temperature of the devices at different air speeds will be simulated using the computational fluid dynamics (CFD) method.

In this work the fan model is Ebmpapst 8314H and the heatsink is LA 10/150 24V from FISCHER ELEKTRONIK. The heat sink was tested to get the temperature distribution in the axial direction of the heatsink when the inlet air speed ranged from 1 to 5 m/s. The result is shown in Figure 10, which shows that when the air speed is above 3m/s, the temperature distribution is more concentrated in the axial direction, and the temperature difference is less than 5 °C. It can therefore be assumed that the cooling system meets the requirements well.

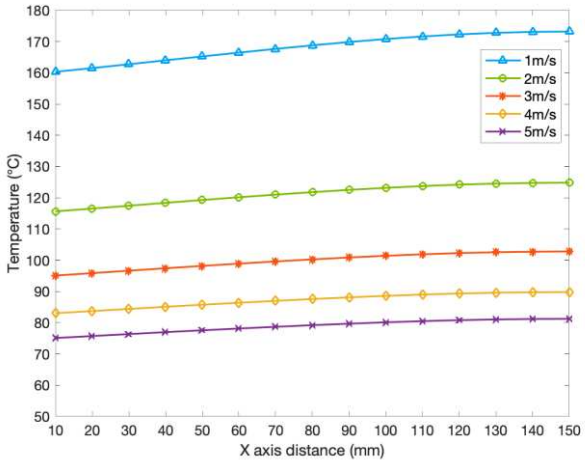

Fig. 10: Temperature distribution along the axial direction

According to the fan's air volume-static pressure characteristic diagram (P-Q curve), the maximum flow rate will appear when the pressure drop across the fan is zero. This only happens if there are no obstacles in front of or behind the fan, allowing air to flow freely into and out of the fan. Once the fan is blocked, such as a heatsink being placed in front of the fan, then there will be some pressure drop across the fan. The air speed at the centre of the heatsink is 3.4m/s, measured by an anemometer when the fan is at rated power. Multiplying the air speed by the effective area of the heatsink gives a mass flow rate of $44.8 m^3/h$ for a single fan, which is the operating point of the cooling system.

The subsequent measurements were taken at air speeds of 1, 3, 3.4 and 5m/s, respectively, when the power modules were connected in parallel using 5 MOSFETs and the power generated using the values from section 2, resulting in the temperatures on the different devices shown in Figure 11. It shows that the temperature generated by the devices does not exceed the maximum device junction temperature when the wind speed is above 3m/s.

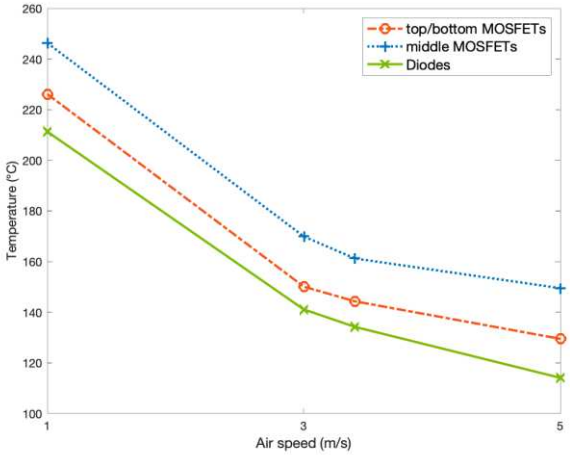

Fig. 11: Device temperature at different air speeds

4 Conclusion

This paper presents the design of a modular SiC MOSFET three-level NPC power module suitable for more-electric aircraft applications. Detailed coupled electro-thermal simulations are presented to support the design process.

In both the electrical and thermal convection models, the use of 3 or 4 MOSFETs in parallel does not meet the design requirements very well. It may even lead to device failure, and given the cost and size of the power module, a design of using 5 MOSFETs in parallel per switch was chosen.

Furthermore, CFD simulations of the cooling system show that it produces a more concentrated temperature distribution on the heatsink when the air speed is above 3m/s, which meets the cooling requirements and keeps the device temperature within the allowable maximum.

It is demonstrated that the module can achieve a peak power of 169 kW per phase when 5 MOSFETs per switch are used. The modules have been manufactured and a three-phase converter, including bespoke gate drives, has been designed, assembled and tested. Results will be presented in a forthcoming publication.

Acknowledgment

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