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1 **Current Limiter Circuit to Avoid Photovoltaic Mismatch Conditions** 2 **including Hot-Spots and Shading**

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5 **Abstract:**

6 Photovoltaic (PV) hot-spots are considered as one of the main reliability issues for PV modules.
7 Although PV modules are capable to tolerate over-temperature, the hot-spots can lead to
8 accelerated aging and, sometimes, to sudden failure with possible risk to fire. The common-
9 practise for mitigating this phenomenon is the adoption of the conventional bypass diode
10 circuit, yet, this method does not guarantee a decrease in the temperature of hot-spotted solar
11 cell. Therefore, in this paper, we present the development of a new current limiter circuit that
12 is capable of mitigating the current flow of PV modules affected by mismatch conditions
13 including partial shading and hot-spotting phenomenon. The foundation of the proposed circuit
14 is fundamentally based on an input buffer which allows high impedance input voltages, and an
15 operational amplifier circuit which controls the current flow of an integrated MOSFETs.
16 Hence, to allow the control of the amount of current passing though mismatched PV sub-
17 strings, and therefore, increase the output power generation. Detailed circuit simulations and
18 multiple experiments are presented to evidence the capability of the circuit. In contrast, the
19 average dissipated power of the circuit is limited to 0.53 W.
20

21 **Keywords: Hot-spots; bypass diode; Reliability Analysis; Photovoltaics.**

22 **1. Introduction**

23 **1.1 Overview of PV Mismatch Conditions**

24 In the last years the Photovoltaic (PV) technology experienced a huge increase of the total
25 installed capacity. As a worldwide point of view, the attainment of the fuel parity pushed large
26 investments in the construction of new photovoltaic systems. By taking in mind that the return
27 of investment (ROI), is not only reliant on the expected lifetime of the PV systems, but also on
28 the continuity of the energy generation, it is clear that PV systems shut down for maintenance
29 purposes should be avoided or, at least, minimized. It is quite understandable that the finest
30 strategy to prevent production losses, and consequent maintenance demands, is to advance the
31 technological solutions for reliability of photovoltaics modules.

32 Nowadays, PV reliability analysis became an important factor to utilize the main cause of PV
33 degradation, failure and mismatch conditions. PV installations frequently suffers from partial
34 shading conditions arise during cloud movements [1], permanent shade (i.e. tree coverage) [2],
35 and dust particles [3]. Practically speaking, these issues are a considered as the major
36 significant factors in decreasing the performance of the output power generation of PV
37 modules, as well as creating an uneven increase in the cells temperature, causing a phenomenon
38 named “PV hot-spots” [4]-[5].

39 It should be remarked that not only the impact of partial shading, mismatch conditions and
40 aging would result hot-spotting phenomenon. But also, PV modules are affected by micro-
41 cracks, snail trail contamination and internal corrosion and delamination, hence, these factors
42 would also increase the probability of the existence of hot-spots. The rising in temperature due
43 to hot-spots is caused by the reversed biasing of the output PV current, thus the affected solar
44 cells will be dissipating power and getting hot [6]. In order to limit the determined reverse
45 voltage and current bias, usually the PV modules are equipped with bypass diodes, as well
46 explained early in 1986 [7]. Unfortunately, various studies including [8]-[10] confirm that
47 bypass diodes cannot overcome the hot-spots events.

48 M. Dhimish *et al.* [8], shows that the mitigation of hot-spots is possible using the integration
49 of MOSFETs parallelised with the PV modules, but, certainly it was observed that the
50 conventional bypass diode fails to overcome the hot-spotting phenomenon. In addition, I.
51 Geisemeyer *et al.* [9] argues that the integration of conventional bypass diodes in hot-spotted
52 PV modules typically would increase the risk of increasing the surface-temperature of the
53 affected PV modules, resulting an increase in the output power loss.

54 According to the survey conducted by P. Manganiello *et al.* [10], it was observed that
55 mismatching conditions and aging of PV modules lead to the occurrence of PV hot-spotting
56 phenomenon. It was recommend that the conventional procedure to overcome PV hot-spots
57 cannot be though using the conventional bypass diodes circuits, but, a more complex power
58 electronics system designs are required.

59 The ability to sustain hot-spots, it has been commercially certified by the international standard
60 IEC 61215 that the integration of bypass diodes have to be the standard practise in PV
61 manufacturing, however, future correspondence of PV hot-spots has to be further investigated.
62 On the other hand, largest up-to-date study have investigated the impact and output power loss
63 of 2580 PV modules distributed across the UK [11]. It was found that the power dissipation of

64 hot-spotted PV modules is varying from -2.7% to -19%. Ultimately, this power loss would
65 increase the fault probability in PV installations due to the presence of the hot-spots.

66 **1.2 Existing Hot-Spots Mitigating Techniques**

67 In this section a comprehensive review of existing hot-spotting mitigating techniques will be
68 discussed. A summary of available hot-spotting mitigation methods are presented in **Table 1**.
69 K. Kim & P. Krein [12] proposed one of the first hot-spotting mitigation techniques which is
70 based on the reconfiguration of the PV module bypass diodes. This technique moderately
71 improves the hot-spotted solar cells temperature. On the other hand, S. Daliento *et al.* [13],
72 presented a modified bypass diode configuration with the present of MOSFETs to state ON-
73 OFF the PV module during hot-spotting scenarios, while the system output power improvement
74 was not discussed.

75 Other methods, such as [14]-[17] use the relay-state controllable MOSFETs within the hot-
76 spotted PV modules. There is a considerable increase in the output power during partial shading
77 scenarios, as well as decrease in the hot-spotted cells temperature. However, these methods
78 contains micro-controller based circuits, eventually, needs further modification and complex
79 programming algorithms, as well as additional power supply for the equipped circuit.

80 In 2019, two novel algorithms based on two different mitigation process have been suggested
81 to improve the performance of PV modules affected by hot-spots. P. Guerriero *et al.* [18]
82 proposed a modified bypass diode circuit that is capable of decreasing the temperature of the
83 hot-spots up to 50 °C; while during partial shading scenarios the circuit is only capable of
84 enhancing the output power by at most 8%. In addition, M. Dhimish. [19], proposed suitable
85 method improves the output power of hot-spotted PV module at least by 70%. The method uses
86 a modified maximum power point tracking (MPPT) algorithm which is skilled of determining
87 the amount of current and voltage loss for hot-spotted PV modules, subsequently, increasing
88 the output power production. While the main drawback of this algorithm that it is not capable
89 of decreasing the temperature of the hot-spots.

90 By contrast with above limitations, in this article, we propose a novel PV hot-spotting
91 mitigation technique using the concept of a current limiter circuit. The proposed circuit is based
92 on an input buffer which allows high impedance input voltages that occurs during mismatch
93 conditions (i.e. partial shading), and an operational amplifier circuit which controls the current
94 flow of an integrated MOSFETs. Hence, to allow the control of the amount of current passing
95 though mismatched PV sub-strings, and therefore, increase the output power generation.

96 Differently from previous hot-spotting mitigation solutions, the new current limiter circuit is
 97 able to completely suppress the current flow into the reverse biased solar cell(s), therefore no
 98 leakage/reversed current is present in the affected PV module. It has also a significant lower
 99 forward voltage drop than conventional bypass diodes circuits such as Schottky diodes.
 100 Practically speaking, a drop of less than 0.24 V at 2 A of current is required to function the
 101 circuit which translates into a typical maximum power dissipation of 0.5 W.

102 Additional advantage of the proposed circuit that it can eliminate the increase of the hot-spotted
 103 solar cells temperature, resulting a maximum increase in the output current of 16.7% if the PV
 104 module is affected by multiple hot-spotted solar cells.

Table 1 Summary of existing PV hot-spotting mitigation techniques

Ref.	Year	Proposed Mitigation Technique	Hot-spots Temperature Improvement	% of Output Power Increase
[12]	2015	Reexamination of bypass diodes integration with PV module as well as improving the structure of the bypass diode equipped with hot-spotted PV modules	Moderately improvement in the cells temperature	Not discussed
[13]	2016	Modified bypass diode circuit integration with respect to ON/OFF MOSFETs process	Cooled down to 24 °C	Not discussed
[14]	2017	DC impedance of PV array current, while a two-state relay is used to open circuited the hot-spotted PV module	Not discussed	Up to 2.3%
[15]	2018	Current and voltage mitigation using MOSFET-based circuit	Cooled down to 13 °C	Up to 1.7%
[16]	2018	Mitigating of PV hot-spots using distributed power electronics and bypass diodes integration	Cooled down to ambient temperate	Up to 15.8%
[17]	2018	16F877A micro-controller based system to prevent hot-spotting using open circuited PV module operation	Cooled down to 17 °C	Up to 3.8%
[18]	2019	A bypass circuit using TLC555 digital oscillator and two N-Channel MOSFET	Cooled down to 50 °C	Up to 8%
[19]	2019	Enhanced Maximum Power point Tracking (MPPT) algorithm to control the decrease of the current for hot-spotted PV modules	Not applicable “PV remains hot-spotted”	Up to 70%

2. Current-Limiter Circuit Implementation – Proposed Method

In order to avoid the decrease of the current caused by PV hot-spots, we have used the principle of current limit circuit, hence to avoid possible decrease/increase in the current of the affected PV module.

The standard current limit operation [20] consists of a current sensor, control circuit and a pass transistor. As shown in **Fig. 1**, R_{sense} is a low-value resistor mainly used to sense the current. As long as the voltage across R_{sense} is less than 0.6 V, the transistor ($T1$) will operate at the conduction state. Whenever the load current (I_L) reaches a value such that when R_{sense} voltage ($R_{sense} \text{ voltage} = I_L \times R_{sense}$) exceeds 0.6 V, the second transistor ($T2$) will start to conduct. The base current of $T1$ is driven by $T2$ and, as consequence the emitter current of $T1$ drops.

The main limitation of this circuit that there is a large voltage drop in the operation of the current limiter, hence, the PV module voltage at output of the limiter would be affected and less power would be produced. This voltage drop is associated with the first transistor $T1$ that requires almost 1 V to function, and across the R_{sense} of about 0.6 V. Therefore, the total drop is equivalent of 1.6 V (i.e. if the PV module is operating at 20 V at maximum power, the net output voltage at the load would be equal to 18.4 V).

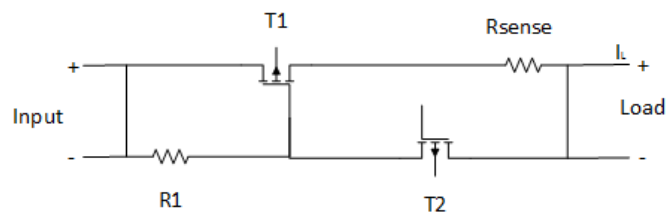


Fig. 1 Widely used current limiter circuit

In contrast with above limitation, we have implemented a novel current limiter circuit which is capable of mitigating the current of the hot-spotted or shaded PV modules with a limited output voltage loss of 0.08 V using 2 A dc load. The developed circuit is shown in **Fig. 2(a)**.

Twenty series connected solar cells which corresponds to a PV sub-string are connected in parallel with a bypass diode. In case, there is greater loss in the current, due to the impact of hot-spotting or high percentage of partial shading, the output current will be derived using the current limiter circuit. The circuit operates for a minimum supply voltage of 5 V, to higher values up to 40 V. The voltage across the R_{sense} resistor is amplified by a subtractor amplifier (LT1636) in a differential mode.

130 According to **Fig. 2(b)**, the differential amplifier (in other words called subtractor), acquires
 131 the output voltage (V_{out}) by the difference of $V1$ and $V2$ multiplied by the ratio of $R3$ and $R1$;
 132 where $R3$ is equal to $R2+R4$, and $R1$ is equal to $R2$. Therefore, V_{out} is calculated as follows:

133
$$V_+ = V1 \frac{R3}{R3+R1} \quad (1)$$

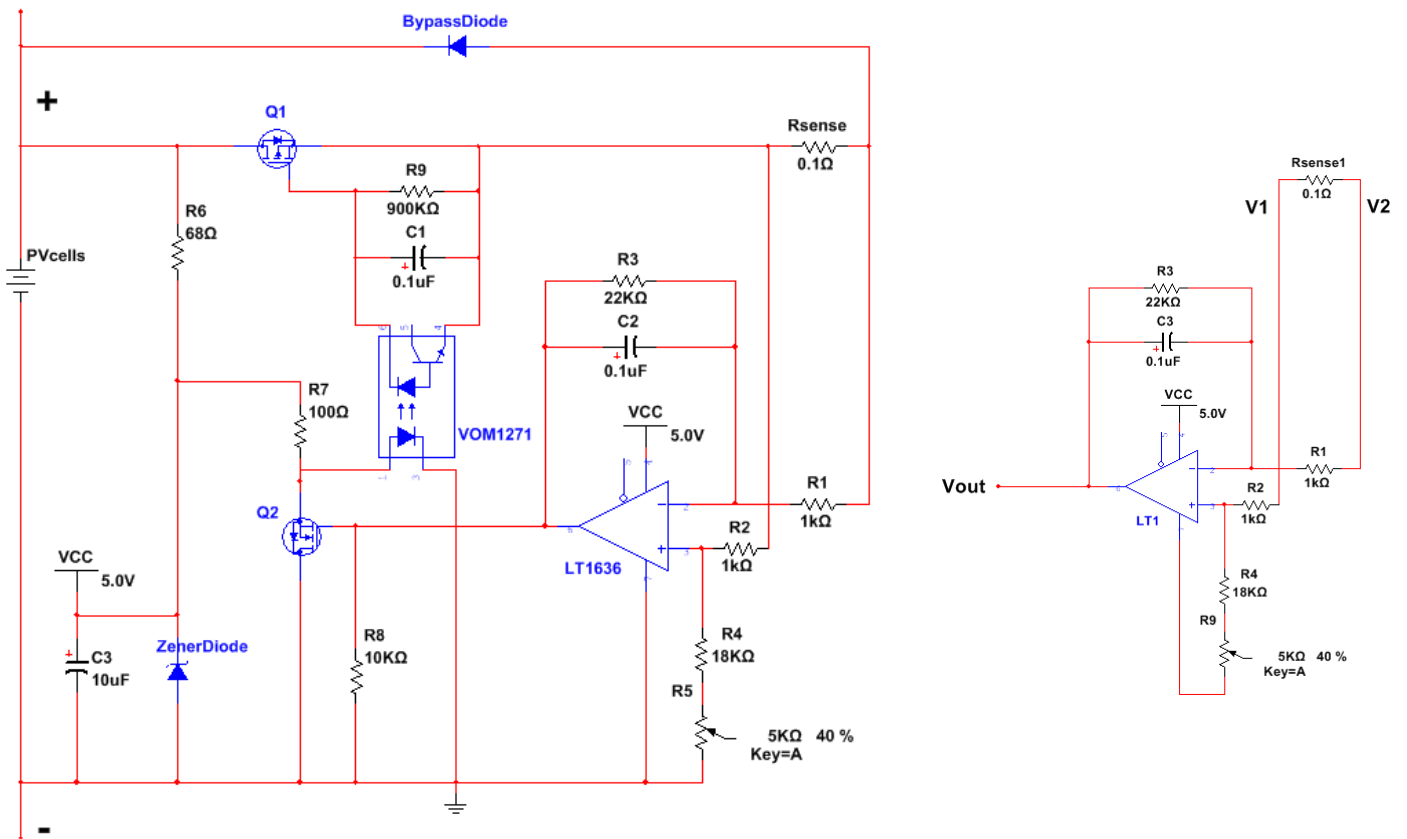
134
$$V_- = V2 + (V_{out} - V2) \frac{R1}{R3+R1} \quad (2)$$

135 Rearranging V_+ and V_- , the output voltage will be equal to:

136
$$V1R3 = V2(R1 + R3) + R1(V_{out} - V2) \quad (3)$$

137
$$V_{out} = (V1 - V2) \frac{R3}{R1} \quad (4)$$

129



143

(a)

(b)

Fig. 2 (a) Proposed current limiter circuit for preventing PV hot-spots/shading, **(b)** Differential Amplifier where the V_{out} is the differential input voltage ($V1 - V2$) multiplied by the ratio of $R3$ and $R1$ ($R1 = R2$)

144 To make the circuit generic, we have added a potentiometer $R9$, which adjusts the gain of the
 145 amplifier. Therefore, if the solar cells have greater current at maximum power point (I_{mpp}), the
 146 circuit will be attuned to gets its nominal output current. As shown in **Fig. 2(a)**, in order to
 147 control the drain-source resistance (R_{DS}), the amplifier output voltage is connected to Q2
 148 MOSFET. On the other hand, the drain current of the Q2 MOSFET controls the LED current
 149 of VOM1271, a photovoltaic MOSFET driver.

150 When the load current is low, R_{sense} voltage is also low. As a result, the amplifier output voltage
 151 remains below the threshold of Q2 MOSFET. The consequential higher LED current of the
 152 MOSFET driver yields an output voltage which is high enough to drive Q1 MOSFET. Next,
 153 when the load current reaches a value that drives Q2 MOSFET into a conduction mode, the
 154 gate-source voltage V_{GS} of Q1 MOSFET goes low, subsequently forces the load current to go
 155 low. In case of PV hot-spotting or partial shading scenarios, the conduction mode of the Q2
 156 MOSFET will no longer exists, since lower current will be driven by the circuit. Therefore, the
 157 V_{GS} of Q1 MOSFET goes high and forces the load to drive higher current. Consequently,
 158 improving the current flow of the hot-spotted or shaded solar cells, and resulting higher output
 159 power generation of the PV module.

160 The presented solution fully prevents the rising in the temperature of the hot-spotted solar cells
 161 through the control of the current driven by the circuit. Furthermore, different from other
 162 prevention methods such as [15]-[17], the proposed method does not exploit microprocessor
 163 or any other logic-based apparatuses, and it consume a very limited power during the mitigation
 164 events, since the MOSFET Q1 and LED current deriver are internally operated using the
 165 amplifier circuit, whereas the voltage drop across the MOSFET Q1 and R_{sense} is very limited.

166 Previous circuit shown in **Fig. 2(a)** has a differential amplifier with low-impedance
 167 capabilities, and since the purpose of the developed current limiter circuit has to work with
 168 mismatch conditions associated with PV modules, therefore, high impedance would be
 169 expected. Hence, the design of the amplifier circuit has been improved to overcome this issue.
 170 High input impedance instrumentation amplifier is used to allow high impedance measurement
 171 of the PV modules. According to **Fig. 3**, the two non-inverting amplifiers ($LT2$ and $LT3$) are
 172 acting as a buffer amplifiers with a gain expressed by (5). The main advantage of this
 173 modification that the gain of the existing circuit could be adjusted only by changing the input
 174 gain resistance (R_{Gain}).

$$175 \quad \text{Input buffers gain} = 1 + \frac{2R_{buffer}}{R_{Gain}} ; \text{where } R_{buffer1} = R_{buffer2} \quad (5)$$

176 As the differential amplifier take no current, the difference in the voltage of R_{Gain} is equal to
 177 the difference in the voltage across R_{sense} . Therefore, the yielded output voltage of the
 178 differential amplifier is expressed as follows:

179
$$V_{out} = (V1 - V2) \left(1 + \frac{2R_{buffer}}{R_{Gain}} \right) \frac{R3}{R1}; \text{ where } R1 = R2 \quad (6)$$

180 The values of the $R3$ and $R1$ is fixed at $1k\Omega$, R_{buffer} is equal to $10k\Omega$, $V1$ and $V2$ are the positive
 181 and negative input of the differential amplifier, respectively. R_{Gain} is the input gain resistance
 182 adjusted to increase/decrease the gain of the differential amplifier in contrast with high
 183 impedance voltage levels measured at R_{sense} terminals. Hereafter, the modified circuit accepts
 184 high impedance input for mismatching conditions as well as has the capability to regulate the
 185 circuit gain based on a potentiometer allocated in the input buffer circuit.

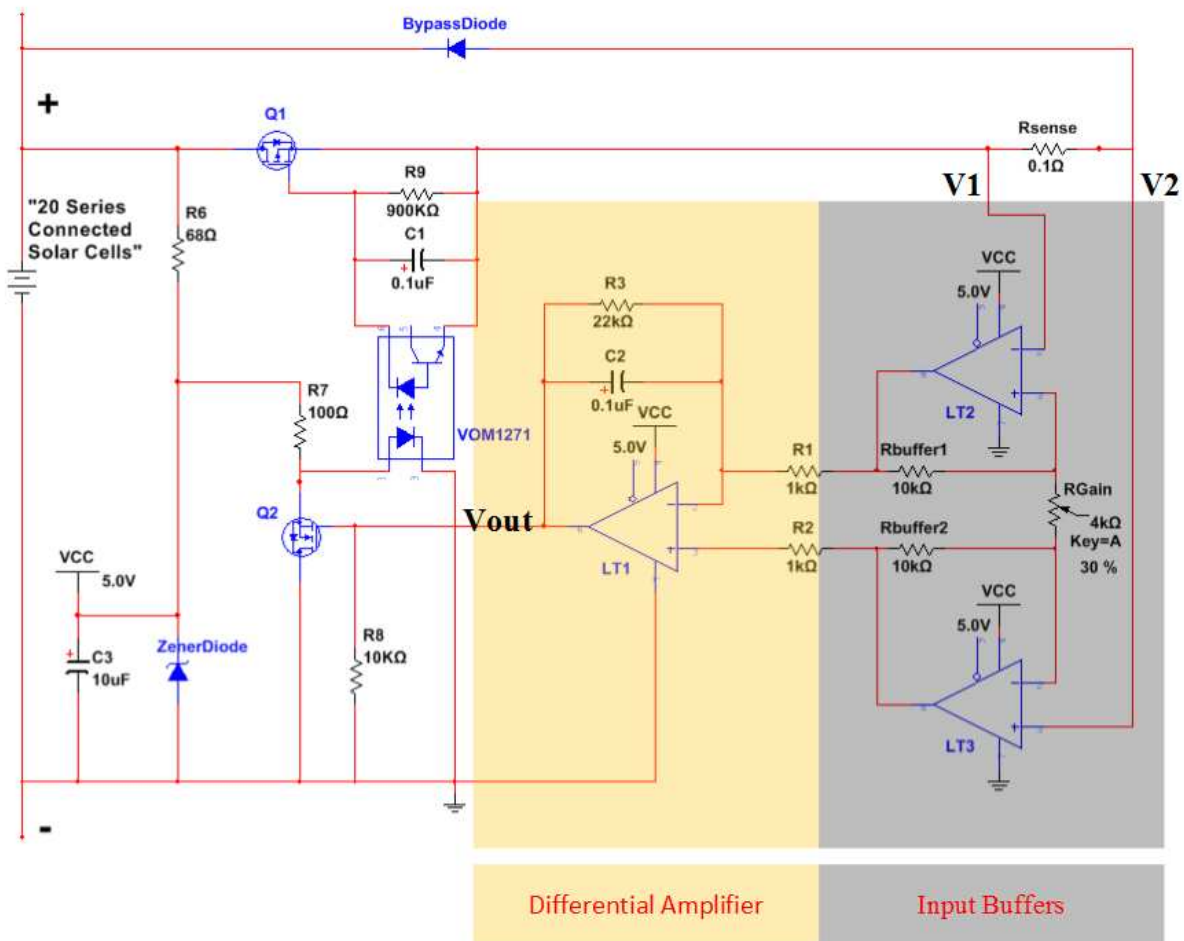


Fig. 3 Improved current limiter circuit with high input impedance characteristics

186 In order to observe the total voltage drop of the proposed current limiter circuit, we have tested
 187 the circuit using a high power resistive load. The resistive load was slowly reduced by factor
 188 of 0.5 A, and the voltage drop across $Q1$ and $Q1+R_{sense}$ are measured; the only loss in the
 189 voltage is across these components since Q2 MOSFET is derived internally by the differential
 190 amplifier as well as the LED current driver. According to **Fig. 4**, the maximum current limiter
 191 circuit voltage drop at 10 A dc load is equal to 0.09 V and 0.12 V across $Q1$ and R_{sense} ,
 192 respectively. Simply, this quantifies that the total loss of the voltage is equal to 0.21 V.

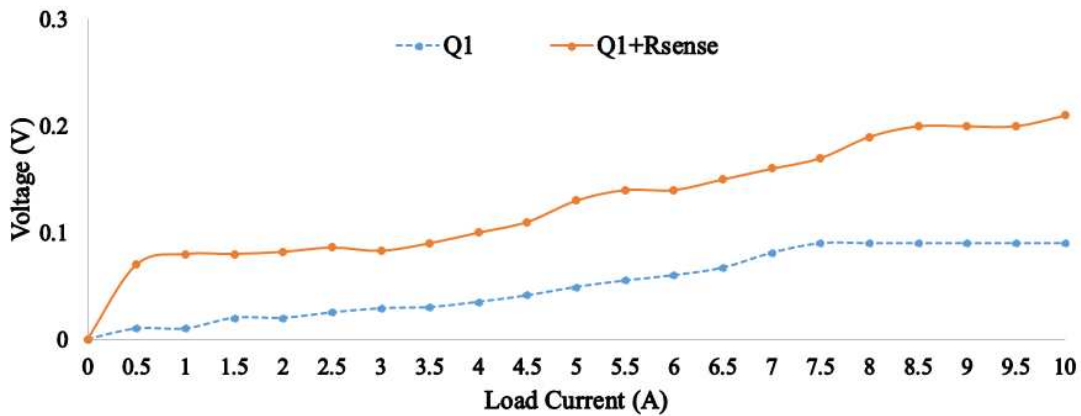


Fig. 4 Voltage drop of $Q1$ and $Q1+R_{sense}$

193 A complete connection of the circuit across three series-connected PV sub-strings are shown
 194 in **Fig. 5**. It is worth noting that the present circuit is designed for monocrystalline and
 195 polycrystalline solar modules, which are made by multiple sub-strings as shown in **Fig. 5**.
 196 While, other PV technologies such as thin films are based on multijunction solar cells that are
 197 manufactured in such a way that each solar cell is provided with its own bypass diode, where
 198 hot-spotting is not a concern.

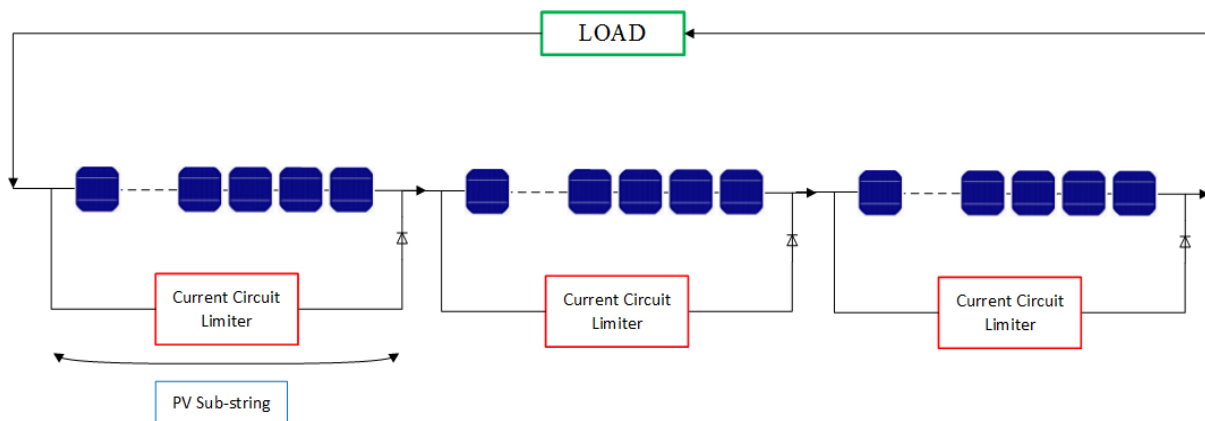


Fig. 5 Detailed connection of three series-connected PV sub-strings with the implemented current circuit limiter

199 **3. Simulation Results**

200 Three different simulation case studies were carried out by analyzing the performance of the
 201 current limiter circuit. The simulation was carried out using MTLAB/Simulink software, the
 202 simulation layout is shown in **Fig. 6**. A single PV sub-string comprising 20 series-connected
 203 solar cells was simulated, while the main electrical parameters at standard test conditions (STC)
 204 are shown in **Table 2**. We have also included a simple perturb and observe (P&O) maximum
 205 power point tracking algorithm to trace the output power-curve (P-V) in each simulated
 206 scenario, a further explanation on the implementation of typical P&O is discussed in previous
 207 articles such as [21]-[23]. The solar irradiance and temperature of each solar cell are taken from
 208 a MATLAB c-code. Therefore, any shading condition could be applied on every solar cell by
 209 changing the solar irradiance. As an example, if a first solar cell is affected by 30% shading,
 210 hence, the solar irradiance would be equal to 700 W/m^2 , instead of 1000 W/m^2 at STC.

Table 2 PV sub-strings (20 series-connected solar cells) main electrical Parameter at STC

Electrical Parameter	Value
Maximum Power Point (P_{mpp})	73.32 W
Current at maximum power point (I_{mpp})	7.67 A
Voltage at maximum power point (V_{mpp})	9.56 V
Short circuit current (I_{sc})	8.18 A
Open circuit voltage (V_{oc})	12.25 V

211 In the first case (case #1), four solar cells are affected by 30% partial shading condition, while
 212 in the second case (case #2) three solar cells are affected by 30% shading condition and other
 213 three are under 75% shading. In the last case (case #3), the implemented current circuit limiter
 214 was examined while 15 solar cells are under 70% shading. Obtained results were compared
 215 with conventional bypass diode circuit [24].

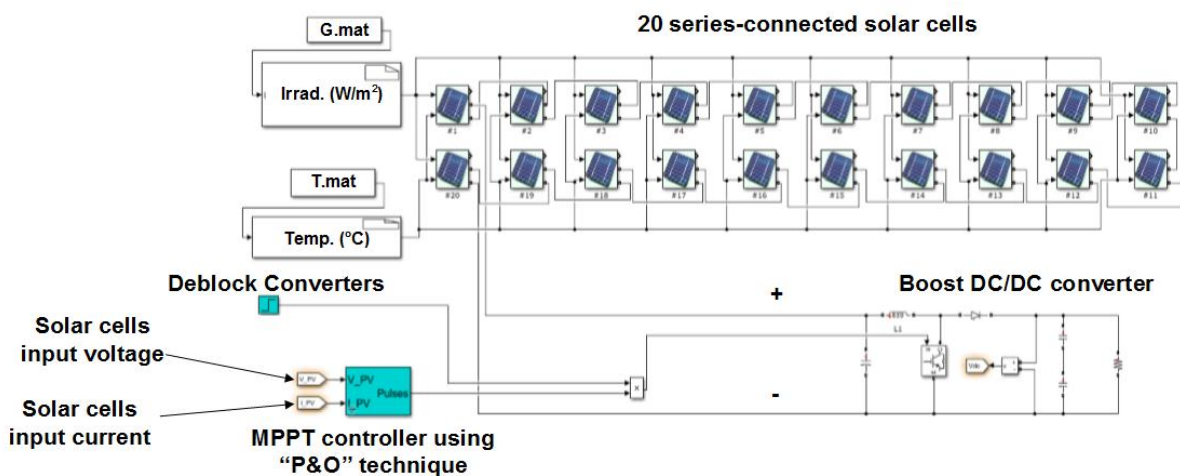


Fig. 6 Simulation layout using MATLAB/Simulink software

216 In the first case (case #1) four solar cells are affected by 30% shading condition, the simulation
 217 results of the P-V curves are shown in **Fig. 7(a)**. Without using the current limiter circuit, the
 218 maximum output power is equal to 64.87W; while there is an increase of 29.2% in the output
 219 power after using the proposed mitigation method. Likewise, results of the second case are
 220 shown in **Fig. 7(b)**. Evidently, the proposed current limiter circuit increases the output power
 221 by 34.2%. According to the results of the last case, shown in **Fig. 7(c)**. The P-V curves show
 222 that without using the current limiter circuit the maximum power is equal to 20.34W; while the
 223 output power is increase by 25% (up to 25.43W) after using the current limiter circuit.

224 As a result, simulation results show that the proposed method is capable of increasing the
 225 output power of the shaded solar cells, typically in a range of 25% to 34%.

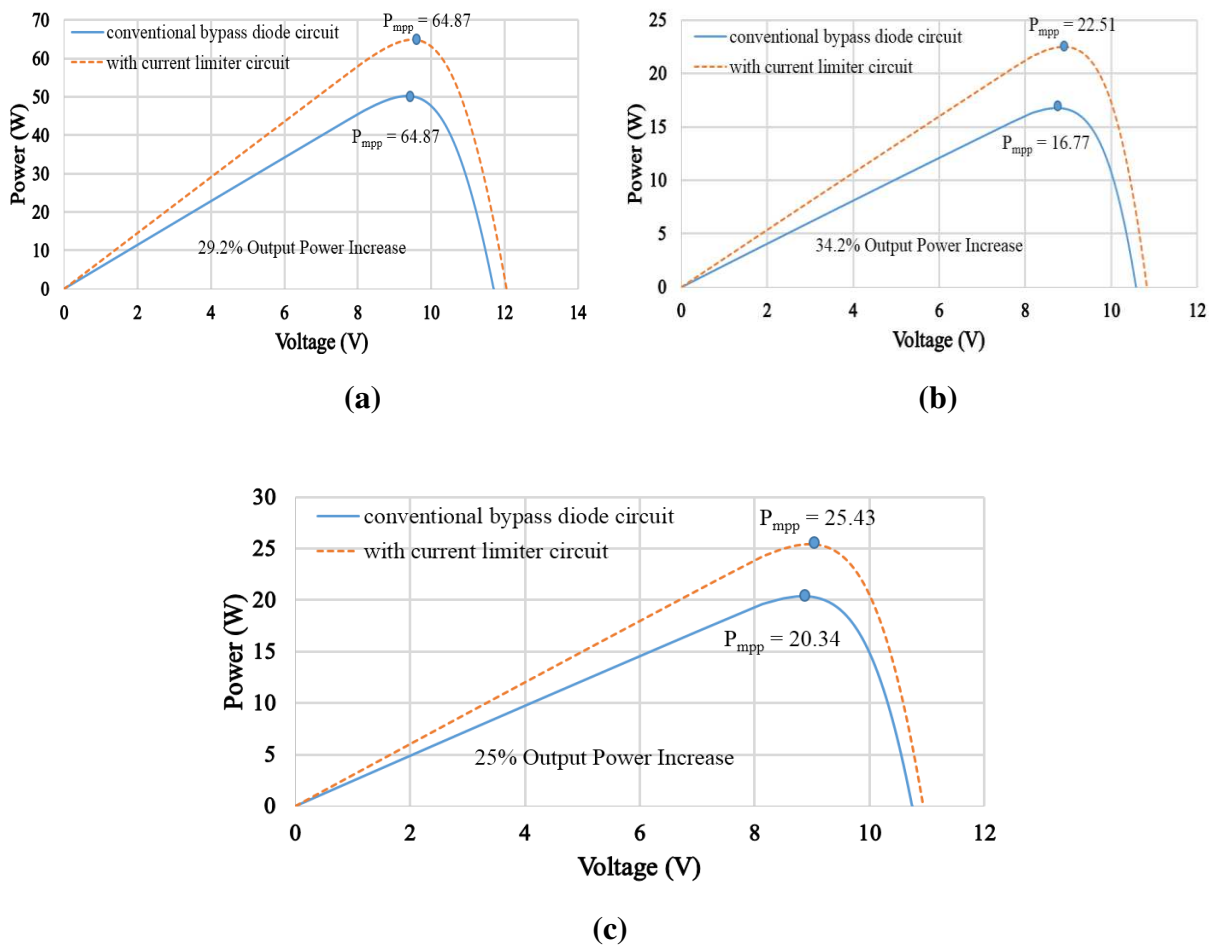


Fig. 7 Simulation results of the Power-Voltage curves for different case studies shown earlier in Fig. 6. (a) Case #1, (b) Case #2, (c) Case #3

226 Despite the improvement in the output power using the current limiter circuit, it is worth
 227 declaring that the proposed circuit on average would dissipated around 0.46W during
 228 conduction mode; where a PV module is affected by a mismatch condition (i.e. shading or hot-
 229 spotting affecting a PV module). **Fig. 8** shows the simulation results of the dissipated output
 230 power of the current limiter circuit while mitigating the current level using the third simulation
 231 case study (Case #3); simulation results captured over a period of one minute; while the
 232 minimum and maximum dissipated power are equal to 0.44 W and 0.47 W, respectively.

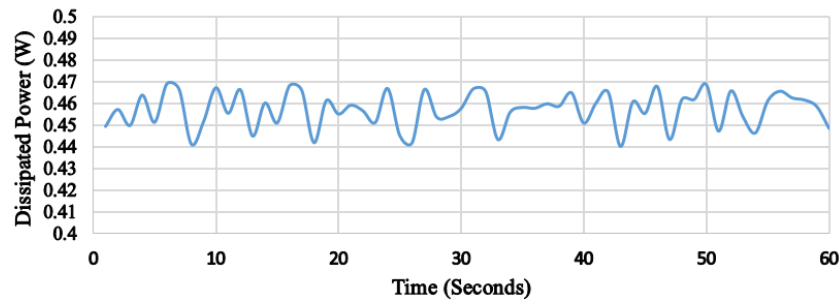


Fig. 8 Power dissipation of the developed current limiter circuit; the simulation is taken from the third case study (Case #3)

233 4. Experimental Results

234 In order to experimentally observe the performance of the new proposed current limiter circuit,
 235 the circuit was integrated with a PV module that will be examined under different scenarios.
 236 The PV module adopted for the experiments is shown in **Fig. 9**. For comparison purposes, the
 237 output measured data for an adjacent PV module configured with a conventional bypass diode
 238 circuit has been considered. The examined PV modules consists of 60 solar cells manufactured
 239 as in three sub-strings, their main electrical parameters are as follows: P_{mpp} : 220.2 W; V_{mpp} :
 240 28.7 V, V_{oc} : 36.7 V, I_{mpp} : 7.67 A, and I_{sc} : 8.18 A.

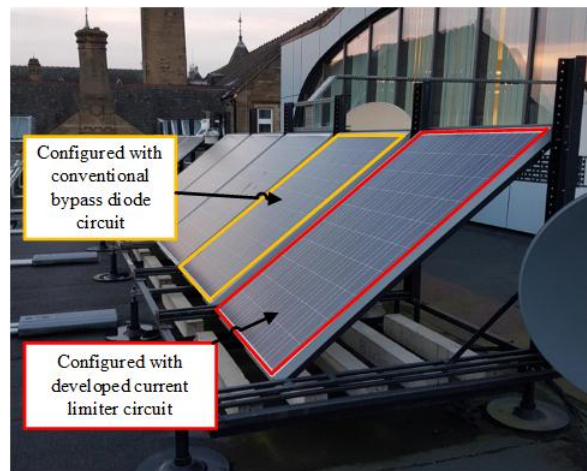


Fig. 9 Examined PV modules

241 The circuit implementation of the new junction-box is shown in **Fig. 10**. Typically for high
 242 power PV modules, there are three to four sub-strings. However, low power PV modules
 243 normally contain 2 sub-string. Therefore, the develop circuit (junction-box) can accept up to
 244 four different sub-strings connection, while the measurements of each sub-string voltage,
 245 current can be monitored. On the other hand, the total voltage loss in the current limiter circuit
 246 can be obtained using the measurement of the voltage drop in across Q1 MOSFET and R_{sense} .

247 It is worth noting that the current is measured using AD8218 a high voltage, high resolution
 248 current shunt sensor [25]. The AD8218 performs bidirectional current measurements across a
 249 shunt resistor with a range of ± 15 A. The sensor is capable of breakthrough performance
 250 throughout the -40 °C to $+125$ °C temperature range, with a maximum measurement error of
 251 0.35%. According to the voltage transducer, the circuit is implant with B25 voltage sensor [26]
 252 that can measure maximum sub-string voltage of 25 V, typically with a maximum measurement
 253 error of 0.1% in a temperature range between -30 °C to $+175$ °C.

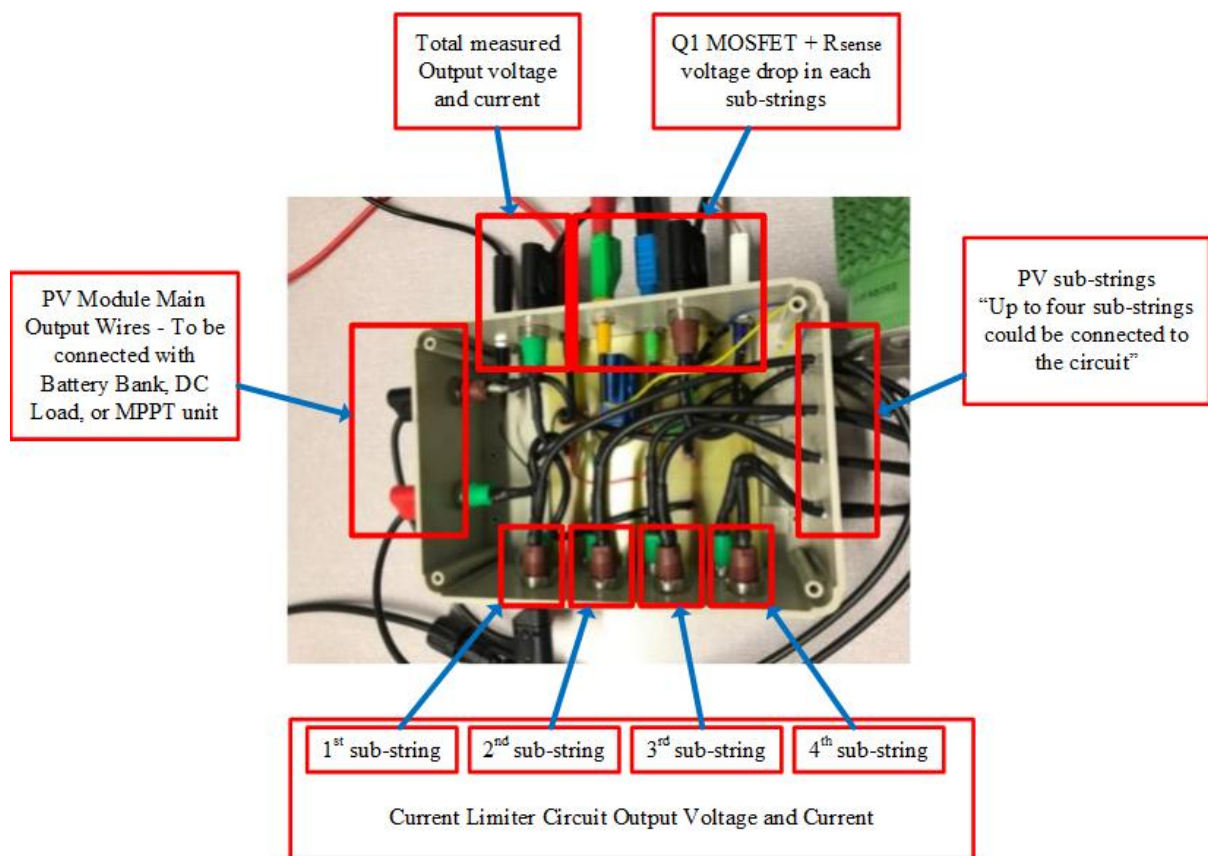


Fig. 10 Developed PV module junction box

254 **4.1 Partial Shading Scenarios**

255 This section presents the evaluation of the current limiter circuit vs. the conventional bypass
256 diode circuit throughout various partial shading scenarios. The examination of each shading
257 scenario lasts for 1-day. In order to observe the effectiveness of the proposed circuit, tested PV
258 modules output voltage, current and power have been recorded.

259 The first partial shading scenario is shown in **Fig. 11(a)**. Two solar cells are covered by opaque
260 object. In contrast, one PV sub-string is affected by a shade (1st sub-string). Same experiment
261 is applied for the 2nd PV module equipped with the conventional bypass diode circuit. Solar
262 irradiance over the day is shown in **Fig. 11(c)**; the solar irradiance and ambient temperature are
263 measured using a ground-based weather station shown in **Fig. 11(b)**, sited adjacent to the
264 examined PV modules, while the average temperature over the day is equal to 12.3 °C.

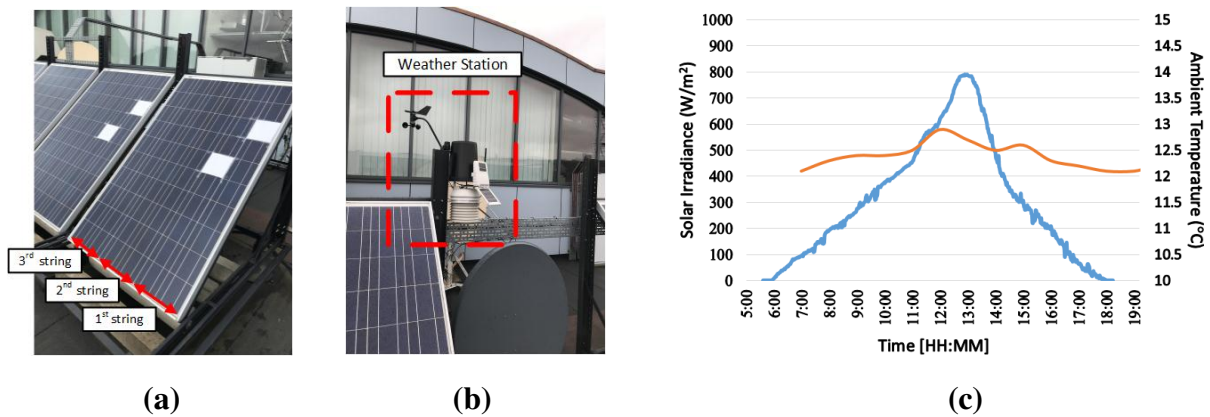


Fig. 11 (a) Shading scenario #1; two solar cells at the same sub-string are covered by opaque object, **(b)** Weather station, **(c)** Measured solar irradiance and ambient temperature during the experiment

265 As shown in **Fig. 12(a)**, the PV sub-strings output voltage are almost identical, with a very
266 limited decrease in the output measured voltage over the shaded PV sub-string (PV string #1).
267 However, the output current shown in **Fig. 12(b)** has a drop in the first PV string of the PV
268 module equipped with the bypass diode circuit, whereas this drop in the output current is no
269 longer exists for the PV module equipped with the proposed current limiter circuit.
270 Subsequently, it is expected to have a drop in the output power generated from the 1st PV sub-
271 string as shown in **Fig. 12(c)**, whistle there is a limited output power loss measured in the PV
272 module equipped with the proposed circuit.

273 According to **Fig. 12(d)**, the yielded output power has an average increase of 5.68% using the
274 proposed circuit. In fact, this increase in the amount of power is allied to the increase in the
275 first PV sub-string output current; whistle, the voltage drop has no significance impact over
276 this particular shading scenario.

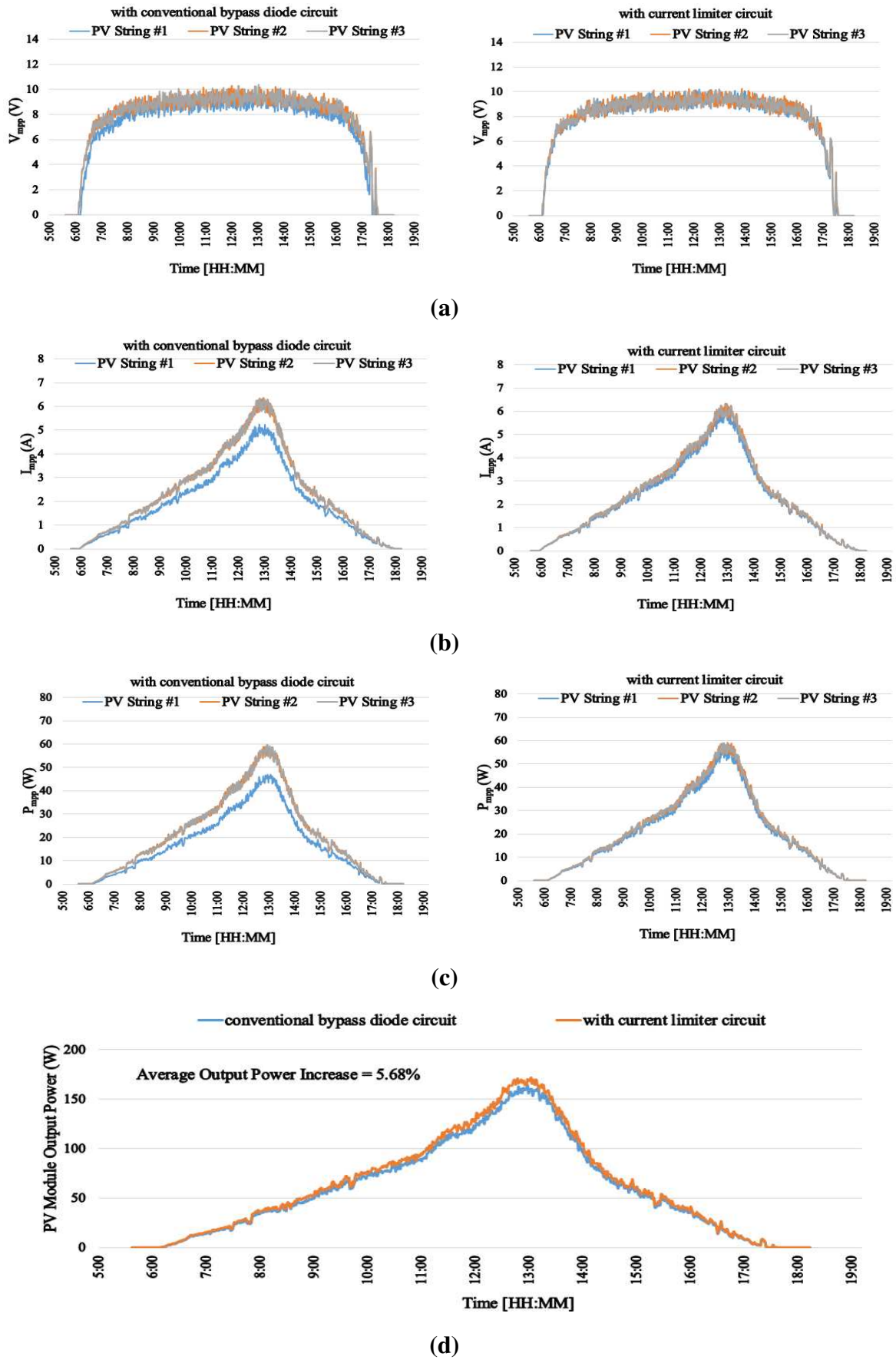


Fig. 12 (a) Measured V_{mpp} , (b) Measured I_{mpp} , (c) Measured P_{mpp} , (d) PV modules measured output power

277 In order to test the Feasibility of the proposed method to overcome the hot-spotting
278 phenomenon during partial shading conditions, we have examined the PV module shown in
279 **Fig. 11(a)**. The thermal image of the PV module before using the current limiter circuit is
280 shown in **Fig. 13(a)**. Since two solar cells are shaded by opaque object, hence, the shaded PV
281 cells electrically operate as load, and the electrical power is transformed into heat causing an
282 increase of the cells temperature from 19.1 to 19.6 °C. However, adjacent solar cells, non-
283 shaded cells, have a temperature of 13.2 °C.

284 At this point, we have manually connected the PV module to the current limiter circuit in order
285 to test its impact on the hot-spots temperature. As shown in **Fig. 13(b)**, the PV module no
286 longer have the hot-spotted solar cells, in fact, this is due to the limitation of the current
287 controlled by the proposed technique. As a result, the PV module solar cells have a temperature
288 of 12.9 °C.

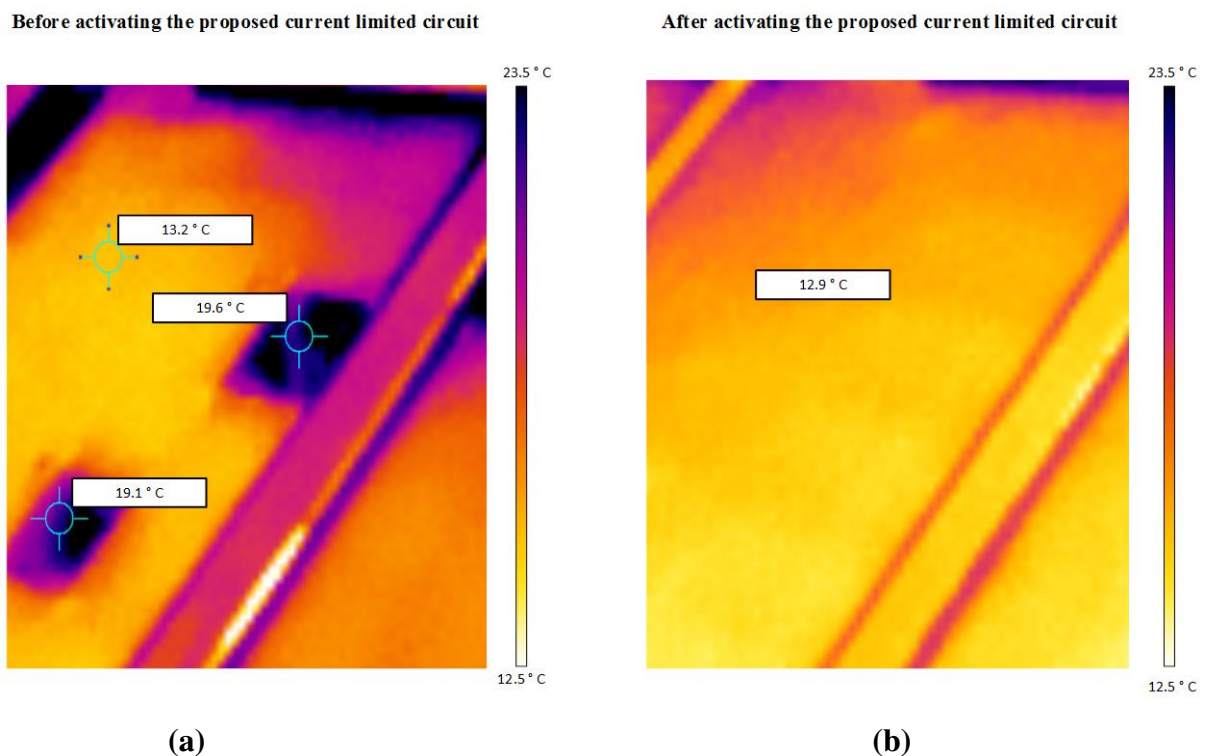


Fig. 13 Impact of using the proposed current limiter circuit on the hot-spots of the PV module present due to the existence of partial shading. (a) Thermal image of the PV module before using the current limiter circuit, (b) Thermal image of the PV module after using the current limiter circuit

289 The second partial shading scenario is shown in **Fig. 14(a)**. Two and four solar cells are shaded
 290 in the first and second PV sub-strings, respectively. Same experiment is applied for the 2nd PV
 291 module equipped with the conventional bypass diode circuit. The Solar Irradiance and ambient
 292 temperature over the day is measured and presented in **Fig. 14(b)**.

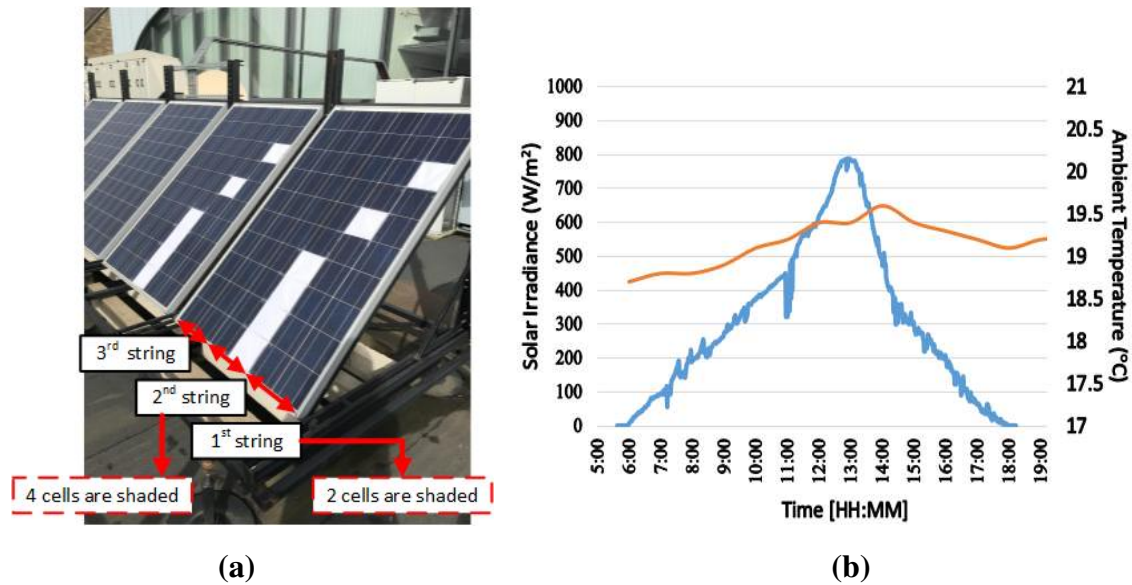
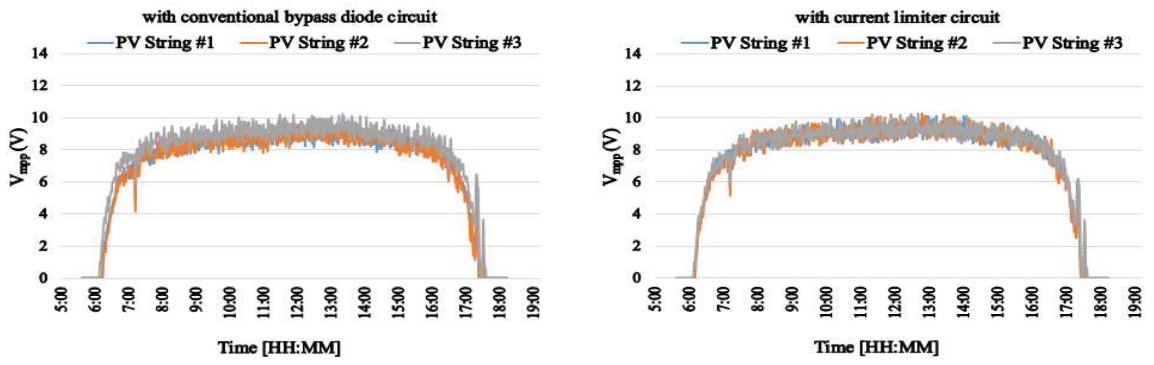


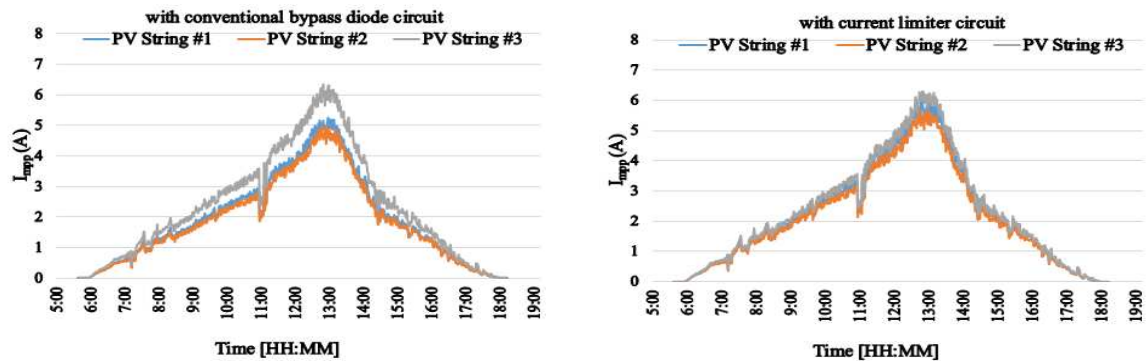
Fig. 14 (a) Shading scenario #2; two and four solar cells are shaded in the first and second PV sub-strings, subsequently, **(b)** Measured solar irradiance and ambient temperature during the experiment

293 As shown in **Fig. 15(a)**, the PV sub-strings output voltage is almost identical, with a very
 294 limited decrease in the V_{mpp} over the shaded PV sub-strings (#1 and #2). However, the output
 295 current shown in **Fig. 15(b)** has a drop in the first and second PV strings of the PV module
 296 equipped with the bypass diode circuit, while this drop in the output current is no longer exists
 297 for the PV module equipped with the proposed current limiter circuit. Consequently, it is
 298 expected to have a drop in the output power generated from the 1st and 2nd PV sub-strings as
 299 presented in **Fig. 15(c)**. The yielded output power has an average increase of 12.3% using the
 300 proposed circuit as presented in **Fig. 15(d)**. Indeed, this increase in the amount of power allied
 301 with the increase in the first and second PV sub-strings output current.

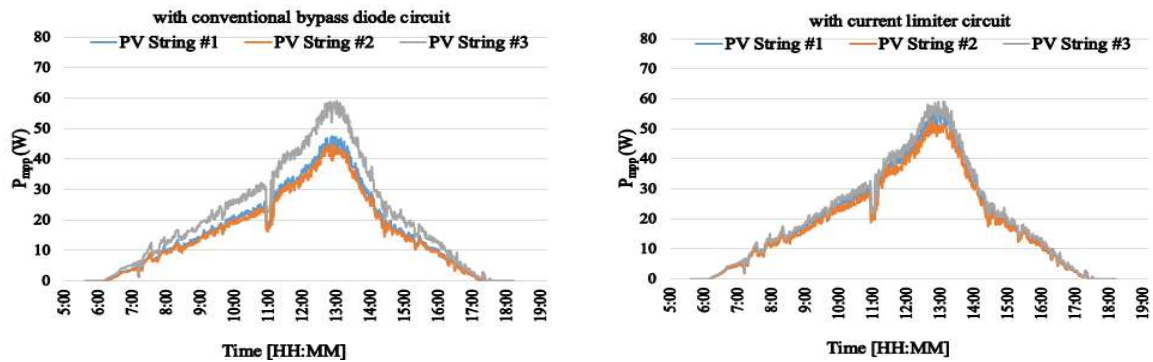
302 As a result, the output power enhancement in both shading scenarios #1 and #2 confirm the
 303 ability of the proposed current limiter circuit to increase the yielded power generation of the
 304 PV modules by mitigating the amount of the current distributed by the mismatched PV sub-
 305 string(s).



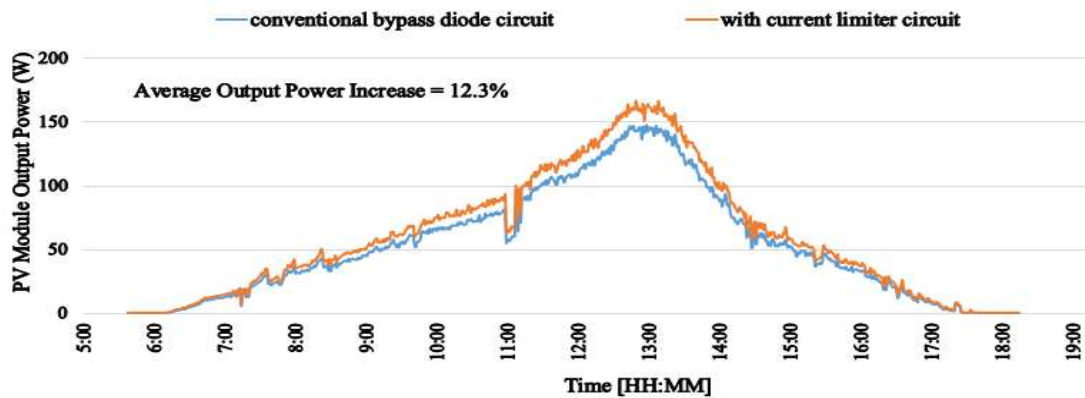
(a)



(b)



(c)



(d)

Fig. 15 (a) Measured V_{mpp} , (b) Measured I_{mpp} , (c) Measured P_{mpp} , (d) PV modules measured output power

4.2 PV Modules Affected by Hot-Spots

In this section, the current limiter circuit will be evaluated using two different PV modules affected by dissimilar hot-spotting type; namely one hot-spotted solar cell, and two hot-spotted solar cells.

The first examined PV module is affected by one hot-spotted solar cell. The thermal image of the hot-spot is shown in **Fig. 16(a)**. As noticed, the hot-spotted solar cell has a temperature of 21.3 °C, compared to adjacent healthy/non-hot-spotted solar cells of 16.2 °C. The proposed current limiter circuit were equipped in the PV module and as presented by the second thermal image, the hot-spot has been completely eliminated; the temperature of the PV module is equal to 15.3 °C. It is worth noting that the used thermal camera (FLIR i5) has a resolution of ± 0.3 °C. By contrast with the results shown in Fig. 16(a), it is evident that the proposed circuit decreases the hot-spot temperature to equivalent with adjacent healthy solar cells. The removal of the hot-spots was guaranteed since the current limiter circuit mitigates the mismatched current flowing through the PV sub-strings, subsequently, warrant an equivalent amount of current flowing into all solar cells.

At first stage the PV module was connected to the conventional bypass diode circuit. Manually, we have reconnected the PV module sub-strings to the current limiter circuit. The solar irradiance during the experiment was fixed at 670 W/m^2 . Here, we have to ensure that the solar irradiance does not change since any variations of the solar irradiance would impact the temperature of the hot-spotted solar cell as well as the amount of current passing though the hot-spotted PV sub-string. Therefore, the selected duration of the experiment lasts for a period of only 1 minute. This procedure was reconsidered while examining the second PV module affected by a different hot-spot type as shown in **Fig. 17(a)**.

Fig. 16(b) shows the results of the PV hot-spotted module while the PV sub-string is connected with the conventional bypass diode and the current limiter circuit; 1200 samples were taken, each sample is measured over a period of 50 ms. Therefore, the experiment duration is equal to $1200 \times 50 \text{ ms} = 1 \text{ minute}$. Remarkably, there is an increase of 14.2% in the output measured current due to the integration the proposed circuit with the PV module. Hence, this increase in the output current would result an increase in the output power generated by the PV module.

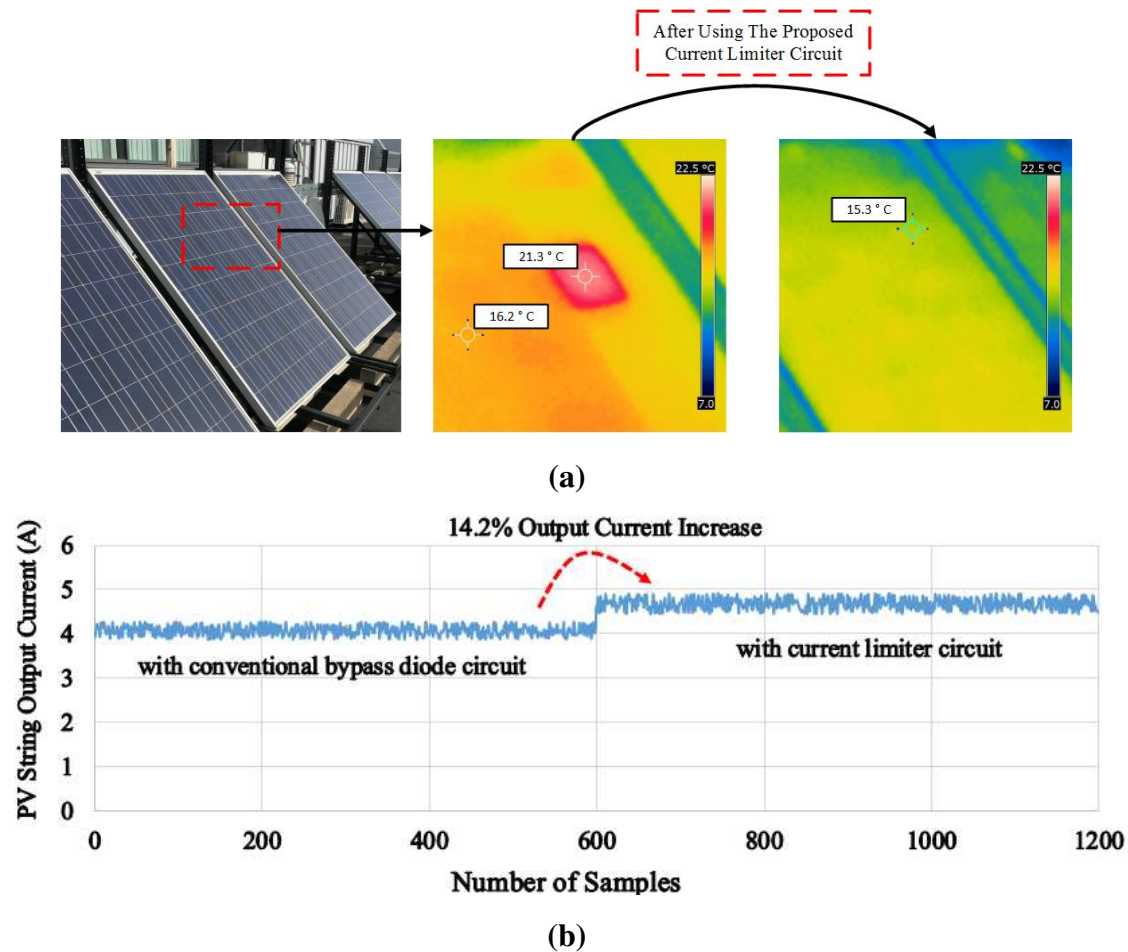


Fig. 16 (a) Thermal image of PV module affected by one hot-spotted solar cell, **(b)** Output current measurements

335 The second examined PV module is affected by two hot-spotted solar cells; thermal image of
 336 the hot-spots are shown in **Fig. 17(a)**. The temperature of the hot-spots is ranging from
 337 21.2~21.4 °C, compared to adjacent healthy/non-hot-spotted solar cells of 15.9 °C. In addition,
 338 the solar irradiance during the experiment was fixed at 677 W/m².

339 The proposed current limiter circuit were equipped with the PV module and as shown by the
 340 second thermal image, both hot-spots have been eliminated. The temperature of the PV module
 341 has been mitigated to 16.4 °C. Furthermore, there is an increase of 16.7% in the output
 342 measured current due to the integration of the current limiter circuit in the PV module, results
 343 are shown in **Fig. 17(b)**.

344 Despite the fact that the proposed current limiter circuit eliminates the hot-spots in the PV
 345 modules as well as increase the output power during partial shading scenarios, yet, it pays off
 346 an additional cost, practically speaking, there is a certain amount of power dissipation that
 347 would be lost during the mitigation/current-limitation process.

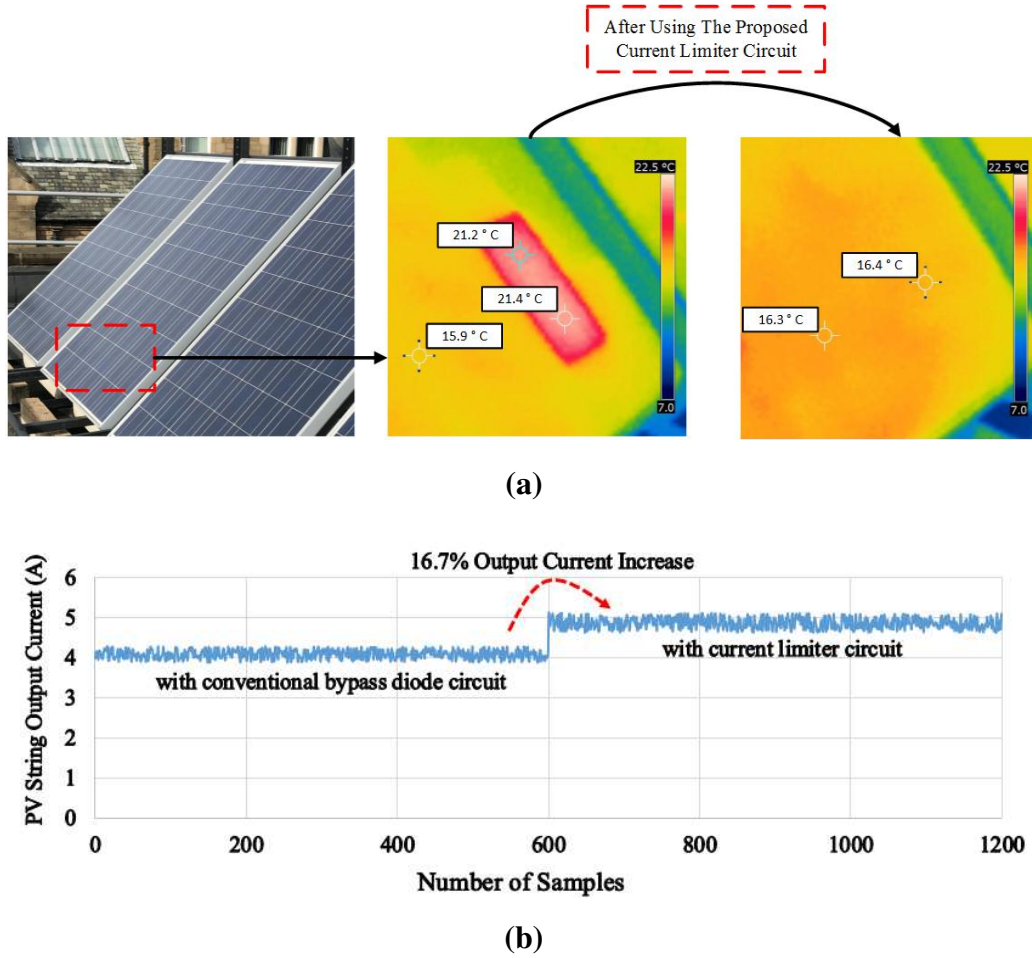


Fig. 17 (a) Thermal image of PV module affected by two hot-spotted solar cells, **(b)** Output current measurements

348 The dissipated power of the PV module equipped with the current limiter circuit vs. the
 349 conventional bypass diode circuit are shown in **Fig. 18(c)**, the experimental setup is shown in
 350 **Fig. 18(a)** where two solar cells are shaded by an opaque object. The test lasts for an hour;
 351 sampling rate: 1 sample/second. As noticed, the average power dissipation is equal to 0.16 W
 352 and 0.05 W using the current limiter and the conventional bypass diode circuit, respectively.

353 Theoretically, the forward voltage drop of the conventional bypass diode for a PV sub-string
 354 is equal to 25 mV typically at 1~8 A dc load. Since we have connected the PV module with 2
 355 A dc load, the power dissipation of the conventional bypass diode circuit shown in **Fig. 18(c)**
 356 is measured by (7).

$$357 \quad P_{dissipation}(\text{conventional bypass diode circuit}) = 25 \text{ mV (only one PV sub -} \\
 358 \text{ string is affected by shading)} \times I_{load} (2 \text{ A}) = 0.05 \text{ W} \quad (7)$$

359 In order to measure the total power dissipation of the proposed current limiter circuit, the
 360 voltage drop across the Q1 MOSFET and R_{sense} is measured. As shown previously in **Fig. 10**,

361 the circuit has three output pins to allow reading the total voltage drop in each of the PV module
 362 sub-strings. Accordingly, **Fig 18(b)** shows that the average voltage drop of 0.08 V occur in the
 363 first sub-string due to the existence of partial shading on this particular sub-string, hence the
 364 circuit has been automatically activated. On the other hand, the second and third sub-strings
 365 have a voltage drop of 0 V, since both sub-strings are not affected by partial shading.

366 The total power dissipated by the current limiter circuit is calculated using (8), where V_{drop} is
 367 the total voltage of Q1 MOSFET and R_{sense} of the current limiter circuit and I_{load} is the load
 368 current.

$$369 \quad P_{dissipation}(proposed\ method) = [(V_{drop\ 1^{st}\ sub\ -\ string}) + (V_{drop\ 2^{nd}\ sub\ -\ string}) +$$

$$370 \quad (V_{drop\ 3^{rd}\ sub\ -\ string})] \times I_{load} = [(0.08\ V) + (0\ V) + (0\ V)] \times 2\ A = 0.16\ W \quad (8)$$

371 As a result, the power dissipation calculated using (8) is identical with the average power
 372 dissipation shown in **Fig.18(c)**.

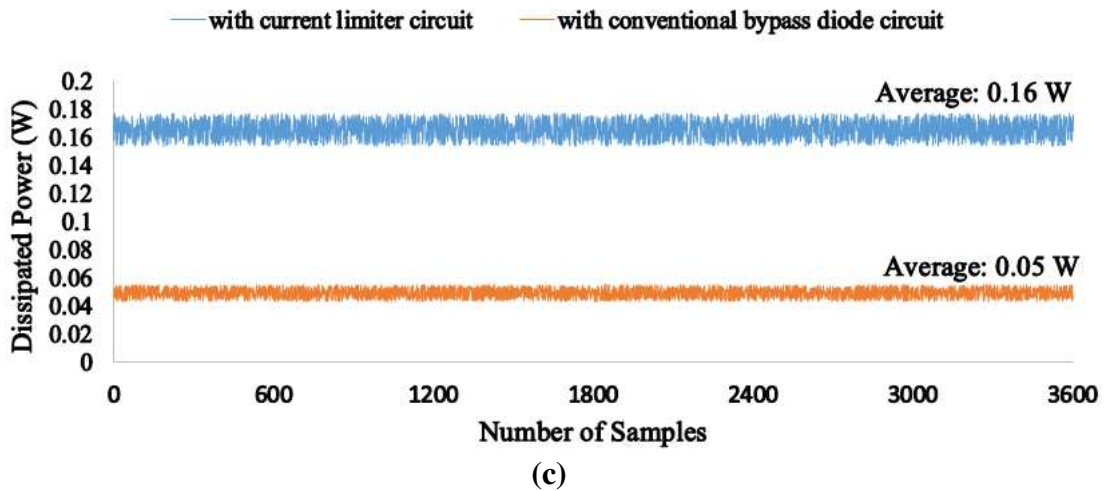
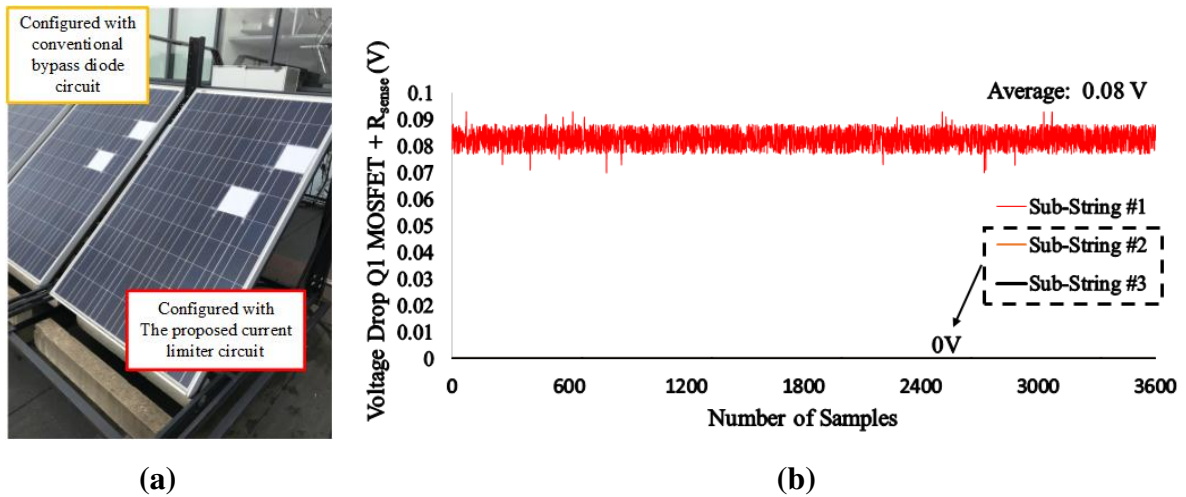


Fig. 18 (a) Experimental setup, (b) Total voltage drop in the current limiter circuit, (c) Comparison of the power dissipation

373 In this regard, it is worth noting that the actual power dissipation of the proposed current limiter
 374 circuit is dependent on the number of PV sub-strings affected by shading or hot-spotting
 375 condition. By contrast, we have examined a PV module under three different scenarios, where
 376 each scenario lasts for 20 minutes:

- 377 1) PV module affected by 20% shading condition; see **Fig. 19(a)**.
- 378 2) No shading is applied.
- 379 3) PV module affected by 60% shading condition; see **Fig. 19(b)**.

380 Since the same partial shading has been applied on all the PV module sub-strings, the voltage
 381 drop across Q1 MOSFET and R_{sense} are almost identical. The average V_{drop} is equal to 0.079
 382 V during 20% shading, while the V_{drop} slightly increase to 0.081 V during 60% shading.
 383 Therefore, it is possible to calculate the power dissipation of the PV module during both
 384 experiments using (9) and (10), respectively.

385
$$P_{dissipation}(20\% \text{ shading}) = [(0.079 \text{ V}) + (0.079 \text{ V}) + (0.079 \text{ V})] \times 2 \text{ A} = 0.474 \text{ W} \quad (9)$$

386
$$P_{dissipation}(60\% \text{ shading}) = [(0.081 \text{ V}) + (0.081 \text{ V}) + (0.081 \text{ V})] \times 2 \text{ A} = 0.486 \text{ W} \quad (10)$$

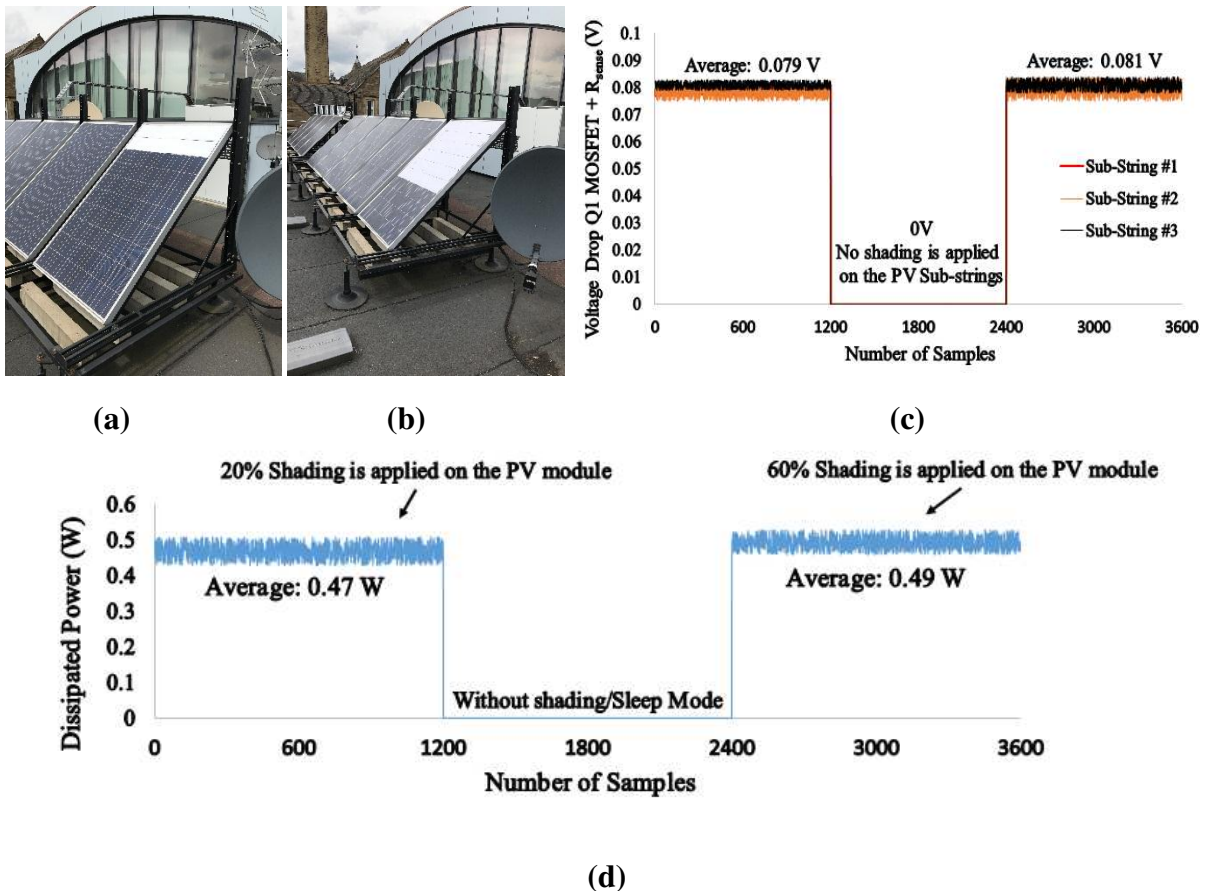


Fig. 19 (a) 20% shading is applied on the PV module, (b) 60% shading is applied on the PV module, (c) Output power dissipation of the current limiter circuit

387 As presented in **Fig. 19(c)**, in the first case, the average power dissipation of the current limiter
388 circuit is equal to 0.47 W, equivalent to the calculated power dissipation by (9). In the second
389 experiment, the circuit is inactivated “sleep mode”, and since the PV module has no shading,
390 the power dissipation of the current limiter circuit is equal to 0 W, while the V_{drop} is equal to
391 0 V in all PV module sub-strings. The third experiment, where the PV module is examined
392 under 60% shading condition, the average measured power dissipation of the circuit is equal to
393 0.49 W, nearly identical to the calculated power dissipation using (10).

394 **5. Conclusion**

395 In this paper a new current limiter circuit has been presented to overcome partial shading and
396 hot-spotting scenarios affecting PV modules. The circuit prevents the limited current generated
397 during partial shading conditions, and eliminating the hot-spots of the PV modules by
398 decreasing its temperature level. With respect to other solutions based on different principles,
399 the proposed circuit has an automatic control behaviour, in the sense that is self-triggering
400 when mismatch conditions such as partial shading or hot-spotting occur in the PV modules.

401 The biggest advantages of the proposed circuit that it does not need any processing unit such
402 as microcontrollers, or any other complex logic circuit implementation. In addition, the
403 developed circuit has a very limited forward voltage drop compared with conventional bypass
404 diodes such as Schottky diodes. It was shown that the actual drop of less than 0.24 V at 2 A of
405 current is required to function the circuit which translates into a typical maximum power
406 dissipation of 0.5 W.

407 The current limiter circuit was experimentally validated using various scenarios. During partial
408 shading conditions, it was evident that the proposed circuit enhances the output generated
409 power by 15% compared to conventional bypass diodes. While, the circuit could also eliminate
410 PV hot-spots, evidently reduces the abnormal PV hot-spots temperature to equivalent the
411 adjacent non-hot-spotted solar cells temperature.

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