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Current Limiter Circuit to Avoid Photovoltaic Mismatch Conditions including Hot-Spots and Shading

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Abstract:

Photovoltaic (PV) hot-spots are considered as one of the main reliability issues for PV modules. Although PV modules are capable to tolerate over-temperature, the hot-spots can lead to accelerated aging and, sometimes, to sudden failure with possible risk to fire. The common-practise for mitigating this phenomenon is the adoption of the conventional bypass diode circuit, yet, this method does not guarantee a decrease in the temperature of hot-spotted solar cell. Therefore, in this paper, we present the development of a new current limiter circuit that is capable of mitigating the current flow of PV modules affected by mismatch conditions including partial shading and hot-spotting phenomenon. The foundation of the proposed circuit is fundamentally based on an input buffer which allows high impedance input voltages, and an operational amplifier circuit which controls the current flow of an integrated MOSFETs. Hence, to allow the control of the amount of current passing though mismatched PV sub-strings, and therefore, increase the output power generation. Detailed circuit simulations and multiple experiments are presented to evidence the capability of the circuit. In contrast, the average dissipated power of the circuit is limited to 0.53 W.

Keywords: Hot-spots; bypass diode; Reliability Analysis; Photovoltaics.

1. Introduction

1.1 Overview of PV Mismatch Conditions

In the last years the Photovoltaic (PV) technology experienced a huge increase of the total installed capacity. As a worldwide point of view, the attainment of the fuel parity pushed large investments in the construction of new photovoltaic systems. By taking in mind that the return of investment (ROI), is not only reliant on the expected lifetime of the PV systems, but also on the continuity of the energy generation, it is clear that PV systems shut down for maintenance purposes should be avoided or, at least, minimized. It is quite understandable that the finest strategy to prevent production losses, and consequent maintenance demands, is to advance the technological solutions for reliability of photovoltaics modules.

Nowadays, PV reliability analysis became an important factor to utilize the main cause of PV degradation, failure and mismatch conditions. PV installations frequently suffers from partial shading conditions arise during cloud movements [1], permanent shade (i.e. tree coverage) [2], and dust particles [3]. Practically speaking, these issues are a considered as the major significant factors in decreasing the performance of the output power generation of PV modules, as well as creating an uneven increase in the cells temperature, causing a phenomenon named "PV hot-spots" [4]-[5].

It should be remarked that not only the impact of partial shading, mismatch conditions and aging would result hot-spotting phenomenon. But also, PV modules are affected by micro-cracks, snail trail contamination and internal corrosion and delamination, hence, these factors would also increase the probability of the existence of hot-spots. The rising in temperature due to hot-spots is caused by the reversed biasing of the output PV current, thus the affected solar cells will be dissipating power and getting hot [6]. In order to limit the determined reverse voltage and current bias, usually the PV modules are equipped with bypass diodes, as well explained early in 1986 [7]. Unfortunately, various studies including [8]-[10] confirm that bypass diodes cannot overcome the hot-spots events.

M. Dhimish *et al.* [8], shows that the mitigation of hot-spots is possible using the integration of MOSFETs parallelised with the PV modules, but, certainly it was observed that the conventional bypass diode fails to overcome the hot-spotting phenomenon. In addition, I. Geisemeyer *et al.* [9] argues that the integration of conventional bypass diodes in hot-spotted PV modules typically would increase the risk of increasing the surface-temperature of the affected PV modules, resulting an increase in the output power loss.

According to the survey conducted by P. Manganiello *et al.* [10], it was observed that mismatching conditions and aging of PV modules lead to the occurrence of PV hot-spotting phenomenon. It was recommend that the conventional procedure to overcome PV hot-spots cannot be though using the conventional bypass diodes circuits, but, a more complex power electronics system designs are required.

The ability to sustain hot-spots, it has been commercially certified by the international standard IEC 61215 that the integration of bypass diodes have to be the standard practise in PV manufacturing, however, future correspondence of PV hot-spots has to be further investigated. On the other hand, largest up-to-date study have investigated the impact and output power loss of 2580 PV modules distributed across the UK [11]. It was found that the power dissipation of

hot-spotted PV modules is varying from -2.7% to -19%. Ultimately, this power loss would increase the fault probability in PV installations due to the presence of the hot-spots.

1.2 Existing Hot-Spots Mitigating Techniques

In this section a comprehensive review of existing hot-spotting mitigating techniques will be discussed. A summary of available hot-spotting mitigation methods are presented in **Table 1**. K. Kim & P. Krein [12] proposed one of the first hot-spotting mitigation techniques which is based on the reconfiguration of the PV module bypass diodes. This technique moderately improves the hot-spotted solar cells temperature. On the other hand, S. Daliento *et al.* [13], presented a modified bypass diode configuration with the present of MOSFETs to state ON-OFF the PV module during hot-spotting scenarios, while the system output power improvement was not discussed.

Other methods, such as [14]-[17] use the relay-state controllable MOSFETs within the hot-spotted PV modules. There is a considerable increase in the output power during partial shading scenarios, as well as decrease in the hot-spotted cells temperature. However, these methods contains micro-controller based circuits, eventually, needs further modification and complex programming algorithms, as well as additional power supply for the equipped circuit.

In 2019, two novel algorithms based on two different mitigation process have been suggested to improve the performance of PV modules affected by hot-spots. P. Guerriero *et al.* [18] proposed a modified bypass diode circuit that is capable of decreasing the temperature of the hot-spots up to 50 °C; while during partial shading scenarios the circuit is only capable of enhancing the output power by at most 8%. In addition, M. Dhimish. [19], proposed suitable method improves the output power of hot-spotted PV module at least by 70%. The method uses a modified maximum power point tracking (MPPT) algorithm which is skilled of determining the amount of current and voltage loss for hot-spotted PV modules, subsequently, increasing the output power production. While the main drawback of this algorithm that it is not capable of decreasing the temperature of the hot-spots.

By contrast with above limitations, in this article, we propose a novel PV hot-spotting mitigation technique using the concept of a current limiter circuit. The proposed circuit is based on an input buffer which allows high impedance input voltages that occurs during mismatch conditions (i.e. partial shading), and an operational amplifier circuit which controls the current flow of an integrated MOSFETs. Hence, to allow the control of the amount of current passing though mismatched PV sub-strings, and therefore, increase the output power generation.

Differently from previous hot-spotting mitigation solutions, the new current limiter circuit is able to completely suppress the current flow into the reverse biased solar cell(s), therefore no leakage/reversed current is present in the affected PV module. It has also a significant lower forward voltage drop than conventional bypass diodes circuits such as Schottky diodes. Practically speaking, a drop of less than 0.24 V at 2 A of current is required to function the circuit which translates into a typical maximum power dissipation of 0.5 W.

Additional advantage of the proposed circuit that it can eliminate the increase of the hot-spotted solar cells temperature, resulting a maximum increase in the output current of 16.7% if the PV module is affected by multiple hot-spotted solar cells.

Table 1 Summary of existing PV hot-spotting mitigation techniques

Ref.	Year	Proposed Mitigation Technique	Hot-spots Temperature Improvement	% of Output Power Increase
[12]	2015	Reexamination of bypass diodes integration with PV module as well as improving the structure of the bypass diode equipped with hot-spotted PV modules	Moderately improvement in the cells temperature	Not discussed
[13]	2016	Modified bypass diode circuit integration with respect to ON/OFF MOSFETs process	Cooled down to 24 °C	Not discussed
[14]	2017	DC impedance of PV array current, while a two-state relay is used to open circuited the hot-spotted PV module	Not discussed	Up to 2.3%
[15]	2018	Current and voltage mitigation using MOSFET-based circuit	Cooled down to 13 °C	Up to 1.7%
[16]	2018	Mitigating of PV hot-spots using distributed power electronics and bypass diodes integration	Cooled down to ambient temperate	Up to 15.8%
[17]	2018	16F877A micro-controller based system to prevent hot-spotting using open circuited PV module operation	Cooled down to 17 °C	Up to 3.8%
[18]	2019	A bypass circuit using TLC555 digital oscillator and two N-Channel MOSFET	Cooled down to 50 °C	Up to 8%
[19]	2019	Enhanced Maximum Power point Tracking (MPPT) algorithm to control the decrease of the current for hot-spotted PV modules	Not applicable "PV remains hot-spotted"	Up to 70%

2. Current-Limiter Circuit Implementation – Proposed Method

In order to avoid the decrease of the current caused by PV hot-spots, we have used the principle of current limit circuit, hence to avoid possible decrease/increase in the current of the affected PV module.

The standard current limit operation [20] consists of a current sensor, control circuit and a pass transistor. As shown in **Fig. 1**, R_{sense} is a low-value resistor mainly used to sense the current. As long as the voltage across R_{sense} is less than 0.6 V, the transistor (*T1*) will operate at the conduction statue. Whenever the load current (I_L) reaches a value such that when R_{sense} voltage (R_{sense} *voltage* = I_L *x* R_{sense}) exceeds 0.6 V, the second transistor (*T2*) will start to conduct. The base current of *T1* is driven by *T2* and, as consequence the emitter current of *T1* drops.

The main limitation of this circuit that there is a large voltage drop in the operation of the current limiter, hence, the PV module voltage at output of the limiter would be affected and less power would be produced. This voltage drop is associated with the first transistor *T1* that requires almost 1 V to function, and across the R_{sense} of about 0.6 V. Therefore, the total drop is equivalent of 1.6 V (i.e. if the PV module is operating at 20 V at maximum power, the net output voltage at the load would be equal to 18.4 V).

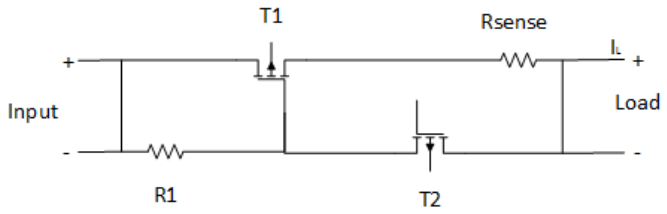


Fig. 1 Widely used current limiter circuit

In contrast with above limitation, we have implemented a novel current limiter circuit which is capable of mitigating the current of the hot-spotted or shaded PV modules with a limited output voltage loss of 0.08 V using 2 A dc load. The developed circuit is shown in **Fig. 2(a)**.

Twenty series connected solar cells which corresponds to a PV sub-string are connected in parallel with a bypass diode. In case, there is greater loss in the current, due to the impact of hot-spotting or high percentage of partial shading, the output current will be derived using the current limiter circuit. The circuit operates for a minimum supply voltage of 5 V, to higher values up to 40 V. The voltage across the R_{sense} resistor is amplified by a subtractor amplifier (LT1636) in a differential mode.

According to **Fig. 2(b)**, the differential amplifier (in other words called subtractor), acquires the output voltage (V_{out}) by the difference of *V1* and *V2* multiplied by the ratio of *R3* and *R1*; where *R3* is equal to *R2*+*R4*, and *R1* is equal to *R2*. Therefore, V_{out} is calculated as follows:

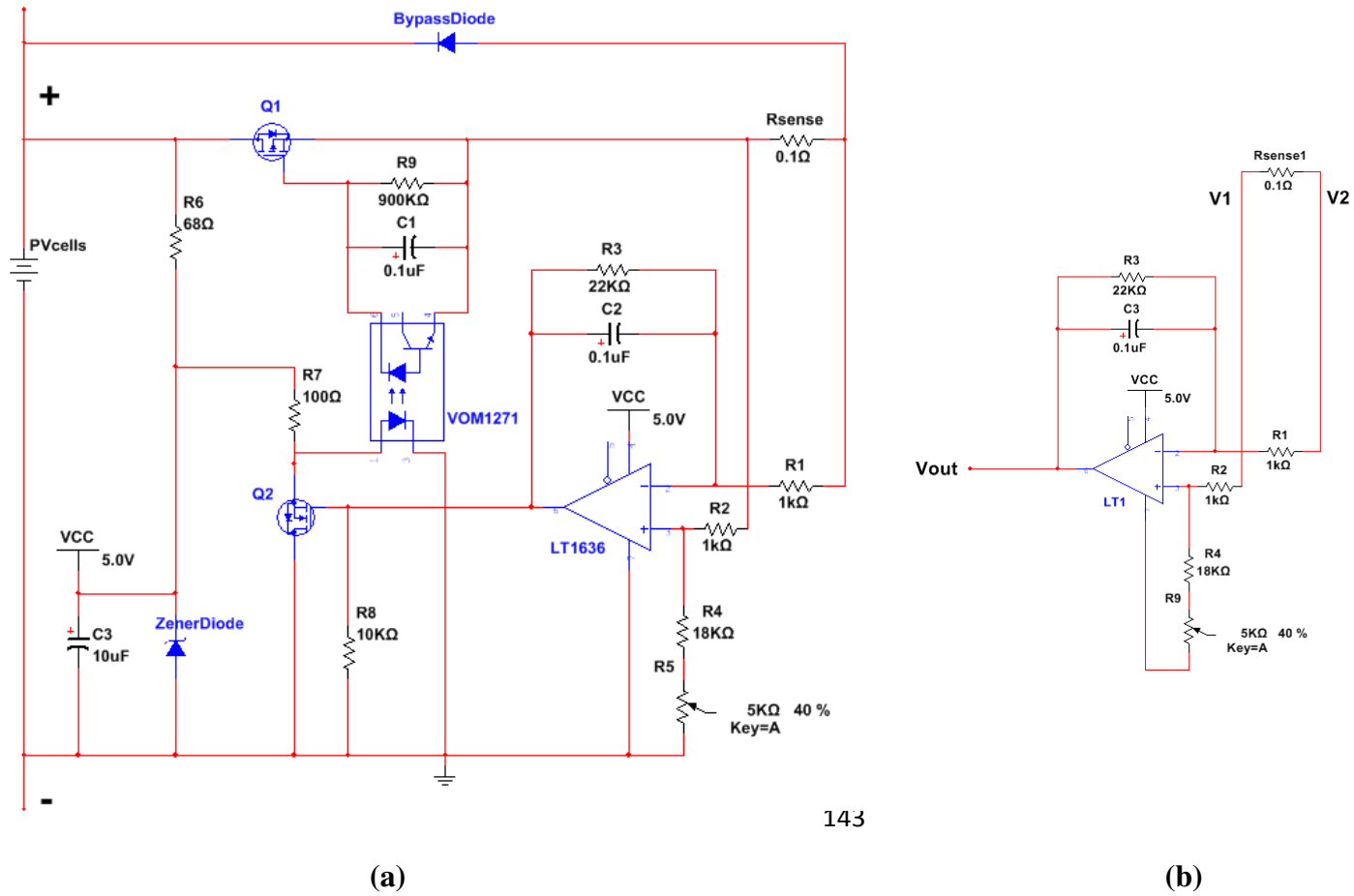
$$V+ = V1\ \frac{R3}{R3+R1} \tag{1}$$

$$V- = V2 + (V_{out} - V2)\ \frac{R1}{R3+R1} \tag{2}$$

Rearranging *V*+ and *V*-, the output voltage will be equal to:

$$V1R3 = V2(R1 + R3) + R1(V_{out} - V2) \tag{3}$$

$$V_{out} = (V1 - V2)\frac{R3}{R1} \tag{4}$$



(a) **(b)**

Fig. 2 (a) Proposed current limiter circuit for preventing PV hot-spots/shading, **(b)** Differential Amplifier where the V_{out} is the differential input voltage (*V1* – *V2*) multiplied by the ratio of *R3* and R1 (*R1* = *R2*)

To make the circuit generic, we have added a potentiometer *R9*, which adjusts the gain of the amplifier. Therefore, if the solar cells have greater current at maximum power point (I_{mpp}), the circuit will be attuned to gets its nominal output current. As shown in **Fig. 2(a)**, in order to control the drain-source resistance (R_{DS}), the amplifier output voltage is connected to Q2 MOSFET. On the other hand, the drain current of the Q2 MOSFET controls the LED current of VOM1271, a photovoltaic MOSFET driver.

When the load current is low, R_{sense} voltage is also low. As a result, the amplifier output voltage remains below the threshold of Q2 MOSFET. The consequential higher LED current of the MOSFET driver yields an output voltage which is high enough to drive Q1 MOSFET. Next, when the load current reaches a value that drives Q2 MOSFET into a conduction mode, the gate-source voltage V_{GS} of Q1 MOSFET goes low, subsequently forces the load current to go low. In case of PV hot-spotting or partial shading scenarios, the conduction mode of the Q2 MOSFET will no longer exists, since lower current will be driven by the circuit. Therefore, the V_{GS} of Q1 MOSFET goes high and forces the load to drive higher current. Consequently, improving the current flow of the hot-spotted or shaded solar cells, and resulting higher output power generation of the PV module.

The presented solution fully prevents the rising in the temperature of the hot-spotted solar cells through the control of the current driven by the circuit. Furthermore, different from other prevention methods such as [15]-[17], the proposed method does not exploit microprocessor or any other logic-based apparatuses, and it consume a very limited power during the mitigation events, since the MOSFET Q1 and LED current deriver are internally operated using the amplifier circuit, whereas the voltage drop across the MOSFET Q1 and R_{sense} is very limited.

Previous circuit shown in **Fig. 2(a)** has a differential amplifier with low-impedance capabilities, and since the purpose of the developed current limiter circuit has to work with mismatch conditions associated with PV modules, therefore, high impedance would be expected. Hence, the design of the amplifier circuit has been improved to overcome this issue. High input impedance instrumentation amplifier is used to allow high impedance measurement of the PV modules. According to **Fig. 3**, the two non-inverting amplifiers (*LT2* and *LT3*) are acting as a buffer amplifiers with a gain expressed by (5). The main advantage of this modification that the gain of the existing circuit could be adjusted only by changing the input gain resistance (R_{Gain}).

$$Input\ buffers\ gain = 1 + \frac{2R_{buffer}}{R_{Gain}}\ ; where\ R_{buffer1} = R_{buffer2} \qquad (5)$$

As the differential amplifier take no current, the difference in the voltage of R_{Gain} is equal to the difference in the voltage across R_{sense}. Therefore, the yielded output voltage of the differential amplifier is expressed as follows:

$$V_{out} = (V1 - V2)\left(1 + \frac{2R_{buffer}}{R_{Gain}}\right)\frac{R3}{R1}; where\ R1 = R2 \quad (6)$$

The values of the *R3* and *R1* is fixed at 1kΩ, R_{buffer} is equal to 10kΩ, *V1* and *V2* are the positive and negative input of the differential amplifier, respectively. R_{Gain} is the input gain resistance adjusted to increase/decrease the gain of the deferential amplifier in contrast with high impedance voltage levels measured at R_{sense} terminals. Hereafter, the modified circuit accepts high impedance input for mismatching conditions as well as has the capability to regulate the circuit gain based on a potentiometer allocated in the input buffer circuit.

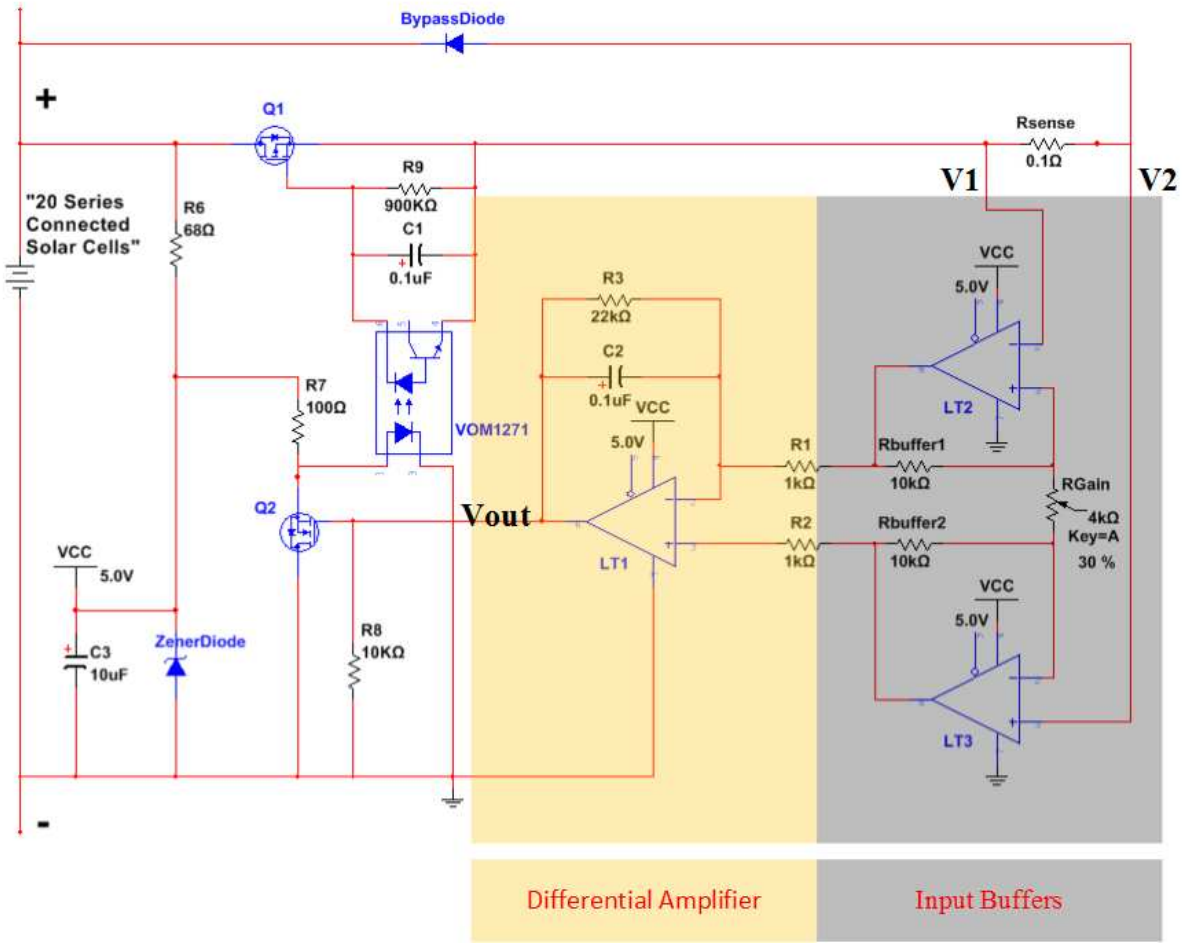


Fig. 3 Improved current limiter circuit with high input impedance characteristics

In order to observe the total voltage drop of the proposed current limiter circuit, we have tested the circuit using a high power resistive load. The resistive load was slowly reduced by factor of 0.5 A, and the voltage drop across *Q1* and *Q1*+R_{sense} are measured; the only loss in the voltage is across these components since Q2 MOSFET is derived internally by the differential amplifier as well as the LED current driver. According to **Fig. 4**, the maximum current limiter circuit voltage drop at 10 A dc load is equal to 0.09 V and 0.12 V across *Q1* and R_{sense}, respectively. Simply, this quantifies that the total loss of the voltage is equal to 0.21 V.

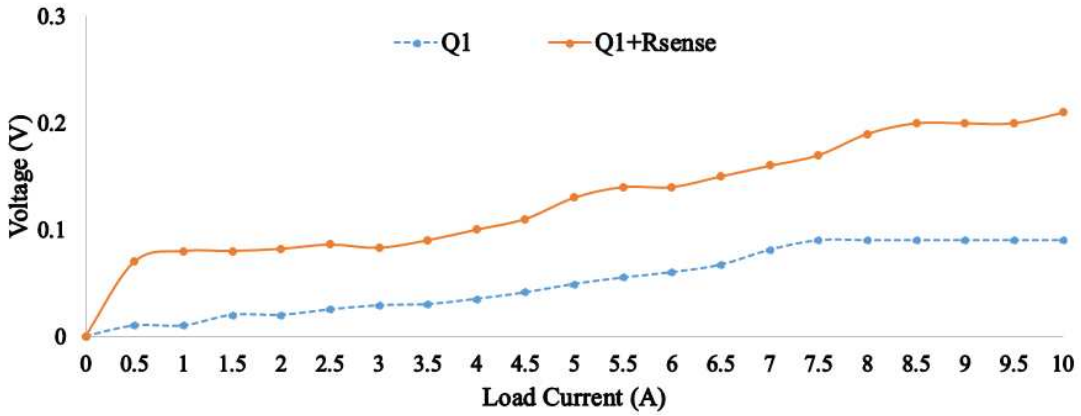


Fig. 4 Voltage drop of Q1 and Q1+R_{sense}

A complete connection of the circuit across three series-connected PV sub-strings are shown in **Fig. 5**. It is worth noting that the present circuit is designed for monocrystalline and polycrystalline solar modules, which are made by multiple sub-strings as shown in **Fig. 5**. While, other PV technologies such as thin films are based on multijunction solar cells that are manufactured in such a way that each solar cell is provided with its own bypass diode, where hot-spotting is not a concern.

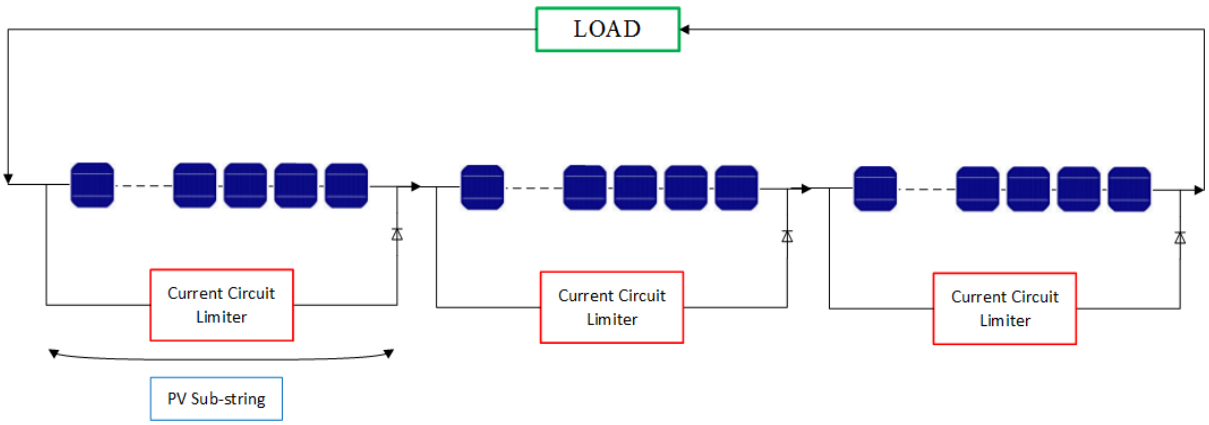


Fig. 5 Detailed connection of three series-connected PV sub-strings with the implemented current circuit limiter

3. Simulation Results

Three different simulation case studies were carried out by analyzing the performance of the current limiter circuit. The simulation was carried out using MTLAB/Simulink software, the simulation layout is shown in **Fig. 6**. A single PV sub-string comprising 20 series-connected solar cells was simulated, while the main electrical parameters at standard test conditions (STC) are shown in **Table 2**. We have also included a simple perturb and observe (P&O) maximum power point tracking algorithm to trace the output power-curve (P-V) in each simulated scenario, a further explanation on the implementation of typical P&O is discussed in previous articles such as [21]-[23]. The solar irradiance and temperature of each solar cell are taken from a MATLAB c-code. Therefore, any shading condition could be applied on every solar cell by changing the solar irradiance. As an example, if a first solar cell is affected by 30% shading, hence, the solar irradiance would be equal to 700 W/m^2, instead of 1000 W/m^2 at STC.

Table 2 PV sub-strings (20 series-connected solar cells) main electrical Parameter at STC

Electrical Parameter	Value
Maximum Power Point (P_{mpp})	73.32 W
Current at maximum power point (I_{mpp})	7.67 A
Voltage at maximum power point (V_{mpp})	9.56 V
Short circuit current (I_{sc})	8.18 A
Open circuit voltage (V_{oc})	12.25 V

In the first case (case #1), four solar cells are affected by 30% partial shading condition, while in the second case (case #2) three solar cells are affected by 30% shading condition and other three are under 75% shading. In the last case (case #3), the implemented current circuit limiter was examined while 15 solar cells are under 70% shading. Obtained results were compared with conventional bypass diode circuit [24].

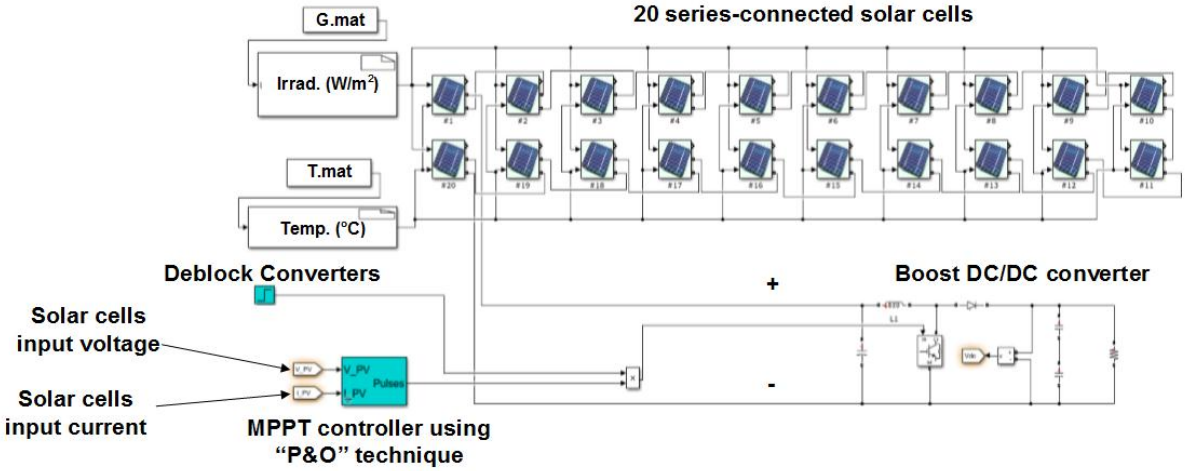


Fig. 6 Simulation layout using MATLAB/Simulink software

In the first case (case #1) four solar cells are affected by 30% shading condition, the simulation results of the P-V curves are shown in **Fig. 7(a)**. Without using the current limiter circuit, the maximum output power is equal to 64.87W; while there is an increase of 29.2% in the output power after using the proposed mitigation method. Likewise, results of the second case are shown in **Fig. 7(b)**. Evidently, the proposed current limiter circuit increases the output power by 34.2%. According to the results of the last case, shown in **Fig. 7(c)**. The P-V curves show that without using the current limiter circuit the maximum power is equal to 20.34W; while the output power is increase by 25% (up to 25.43W) after using the current limiter circuit.

As a result, simulation results show that the proposed method is capable of increasing the output power of the shaded solar cells, typically in a range of 25% to 34%.

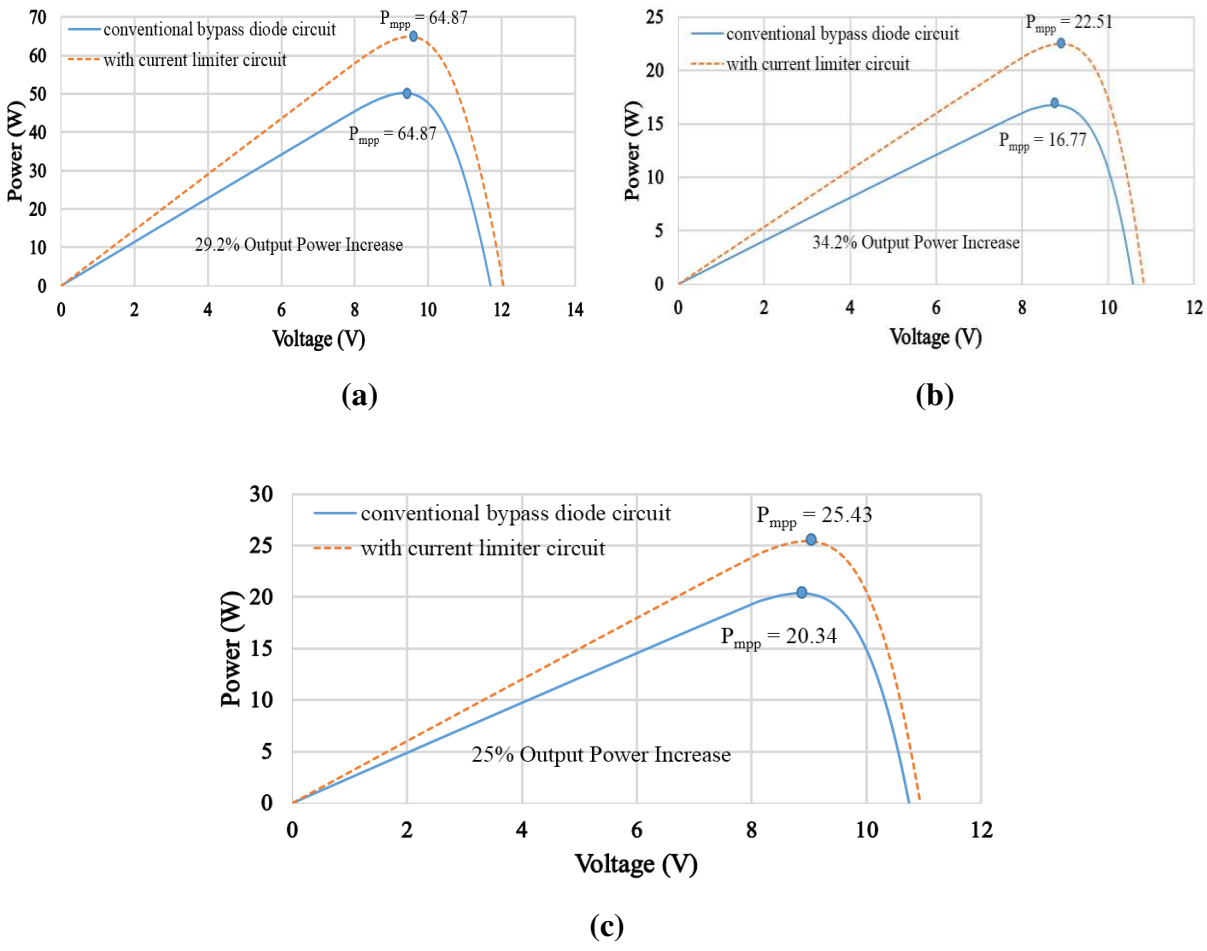


Fig. 7 Simulation results of the Power-Voltage curves for different case studies shown earlier in Fig. 6. **(a)** Case #1, **(b)** Case #2, **(c)** Case #3

Despite the improvement in the output power using the current limiter circuit, it is worth declaring that the proposed circuit on average would dissipated around 0.46W during conduction mode; where a PV module is affected by a mismatch condition (i.e. shading or hot-spotting affecting a PV module). **Fig. 8** shows the simulation results of the dissipated output power of the current limiter circuit while mitigating the current level using the third simulation case study (Case #3); simulation results captured over a period of one minute; while the minimum and maximum dissipated power are equal to 0.44 W and 0.47 W, respectively.

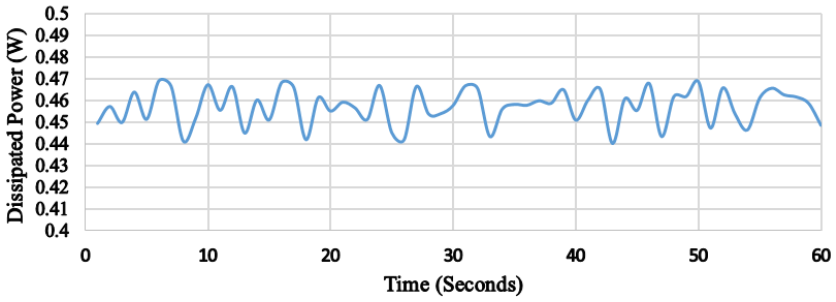


Fig. 8 Power dissipation of the developed current limiter circuit; the simulation is taken form the third case study (Case #3)

4. Experimental Results

In order to experimentally observe the performance of the new proposed current limiter circuit, the circuit was integrated with a PV module that will be examined under different scenarios. The PV module adopted for the experiments is shown in **Fig. 9**. For comparison purposes, the output measured data for an adjacent PV module configured with a conventional bypass diode circuit has been considered. The examined PV modules consists of 60 solar cells manufactured as in three sub-strings, their main electrical parameters are as follows: P_{mpp}: 220.2 W; V_{mpp}: 28.7 V, V_{oc}: 36.7 V, I_{mpp}: 7.67 A, and I_{sc}: 8.18 A.

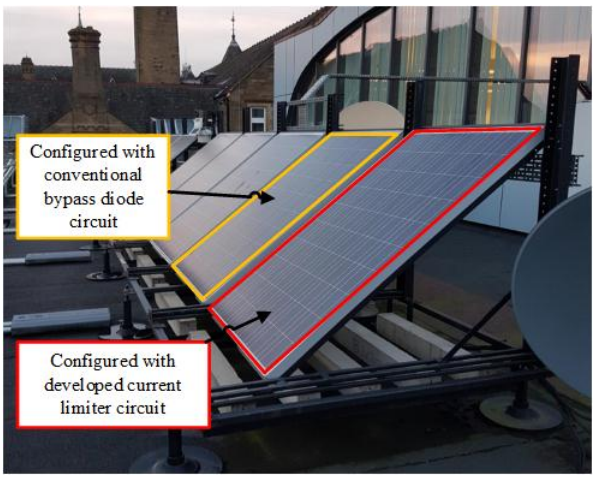


Fig. 9 Examined PV modules

The circuit implementation of the new junction-box is shown in **Fig. 10**. Typically for high power PV modules, there are three to four sub-strings. However, low power PV modules normally contain 2 sub-string. Therefore, the develop circuit (junction-box) can accept up to four different sub-strings connection, while the measurements of each sub-string voltage, current can be monitored. On the other hand, the total voltage loss in the current limiter circuit can be obtained using the measurement of the voltage drop in across Q1 MOSFET and R_{sense}.

It is worth noting that the current is measured using AD8218 a high voltage, high resolution current shunt sensor [25]. The AD8218 performs bidirectional current measurements across a shunt resistor with a range of ±15 A. The sensor is capable of breakthrough performance throughout the −40 °C to +125 °C temperature range, with a maximum measurement error of 0.35%. According to the voltage transducer, the circuit is implant with B25 voltage sensor [26] that can measure maximum sub-string voltage of 25 V, typically with a maximum measurement error of 0.1% in a temperature range between −30 °C to +175 °C.

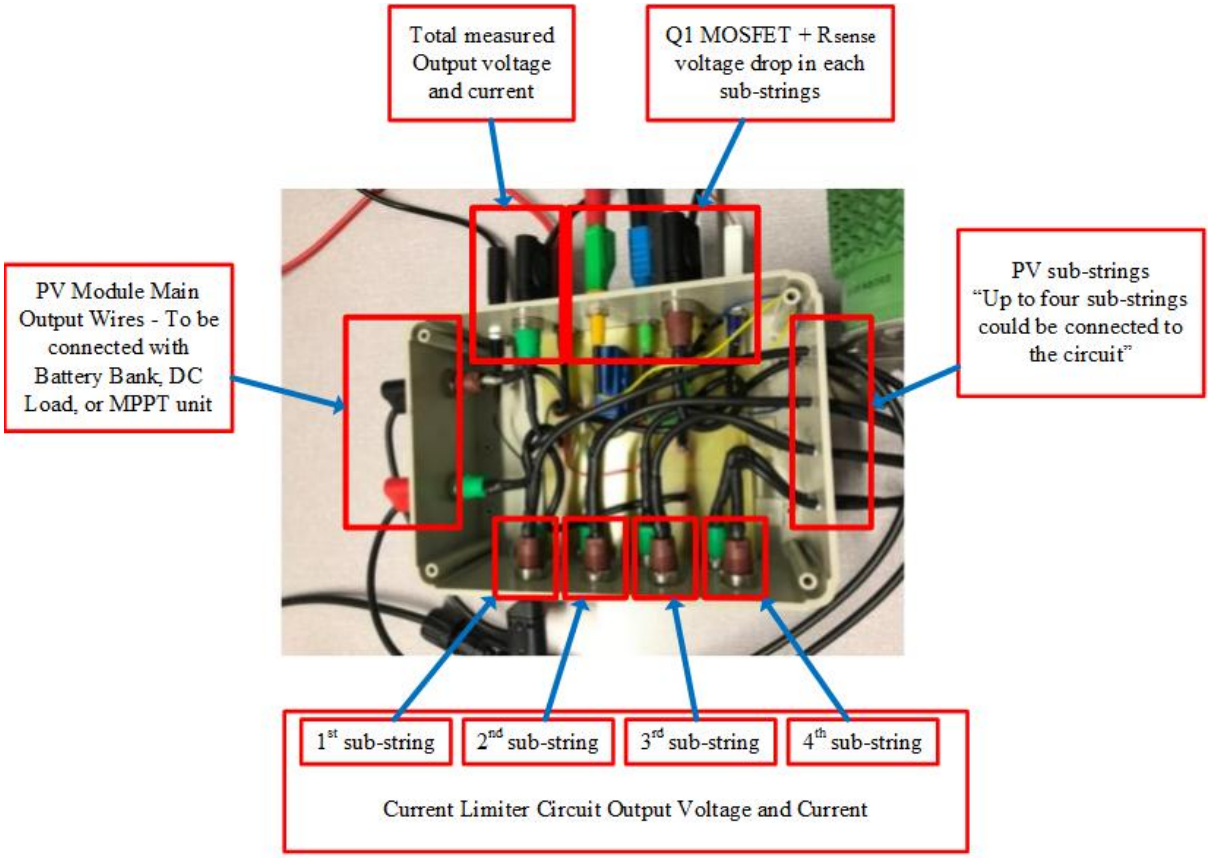
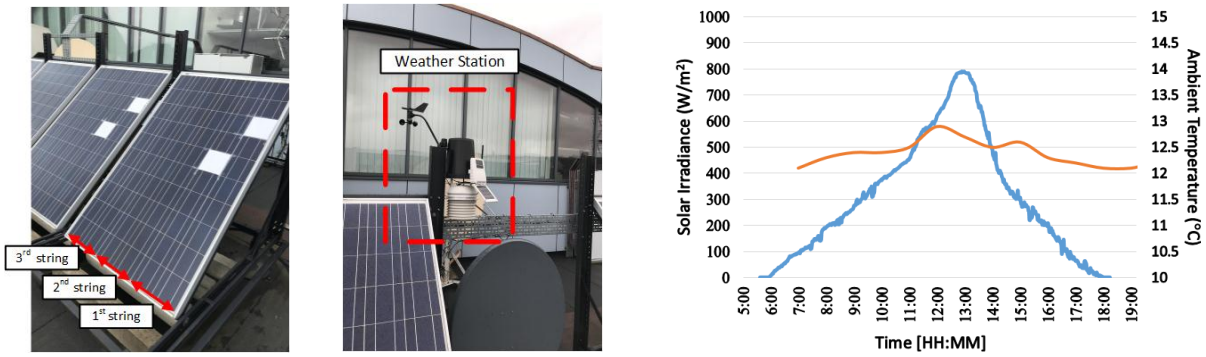


Fig. 10 Developed PV module junction box

4.1 Partial Shading Scenarios

This section presents the evaluation of the current limiter circuit vs. the conventional bypass diode circuit throughout various partial shading scenarios. The examination of each shading scenario lasts for 1-day. In order to observe the effectiveness of the proposed circuit, tested PV modules output voltage, current and power have been recorded.

The first partial shading scenario is shown in **Fig. 11(a)**. Two solar cells are covered by opaque object. In contrast, one PV sub-string is affected by a shade (1st sub-string). Same experiment is applied for the 2nd PV module equipped with the conventional bypass diode circuit. Solar irradiance over the day is shown in **Fig. 11(c)**; the solar irradiance and ambient temperature are measured using a ground-based weather station shown in **Fig. 11(b)**, sited adjacent to the examined PV modules, while the average temperature over the day is equal to 12.3 °C.

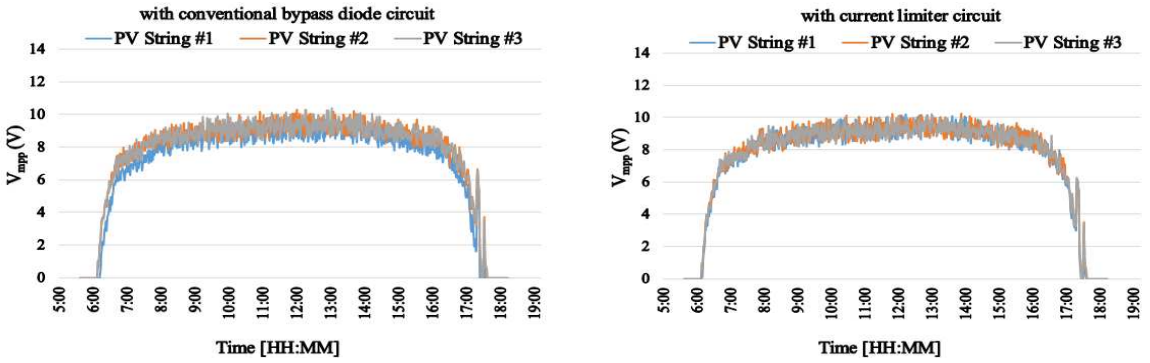


(a) **(b)** **(c)**

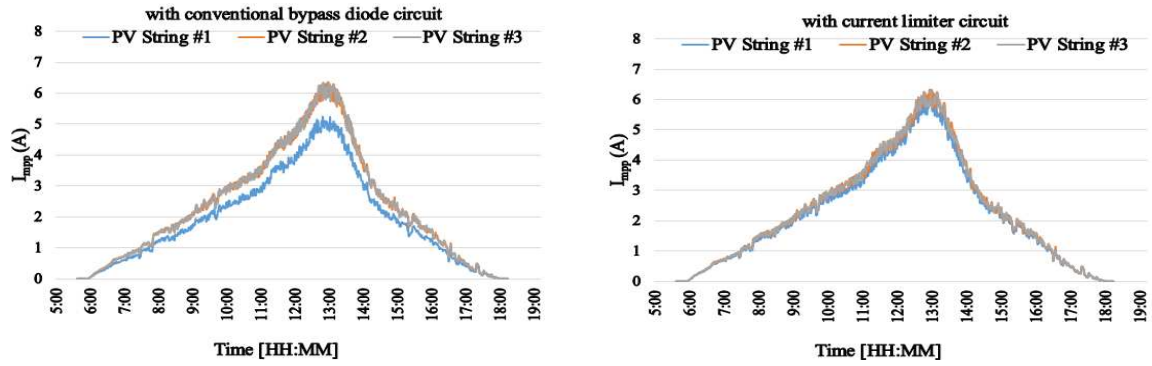
Fig. 11 (a) Shading scenario #1; two solar cells at the same sub-string are coved by opaque object, **(b)** Weather station, **(c)** Measured solar irradiance and ambient temperature during the experiment

As shown in **Fig. 12(a)**, the PV sub-strings output voltage are almost identical, with a very limited decrease in the output measured voltage over the shaded PV sub-string (PV string #1). However, the output current shown in **Fig. 12(b)** has a drop in the first PV string of the PV module equipped with the bypass diode circuit, whereas this drop in the output current is no longer exists for the PV module equipped with the proposed current limiter circuit. Subsequently, it is expected to have a drop in the output power generated from the 1st PV sub-string as shown in **Fig. 12(c)**, whistle there is a limited output power loss measured in the PV module equipped with the proposed circuit.

According to **Fig. 12(d)**, the yielded output power has an average increase of 5.68% using the proposed circuit. In fact, this increase in the amount of power is allied to the increase in the first PV sub-string output current; whistle, the voltage drop has no signification impact over this particular shading scenario.



(a)



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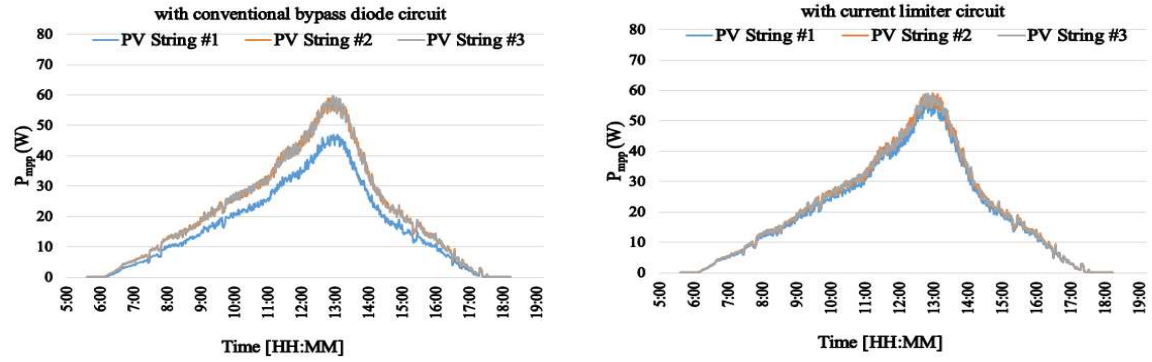
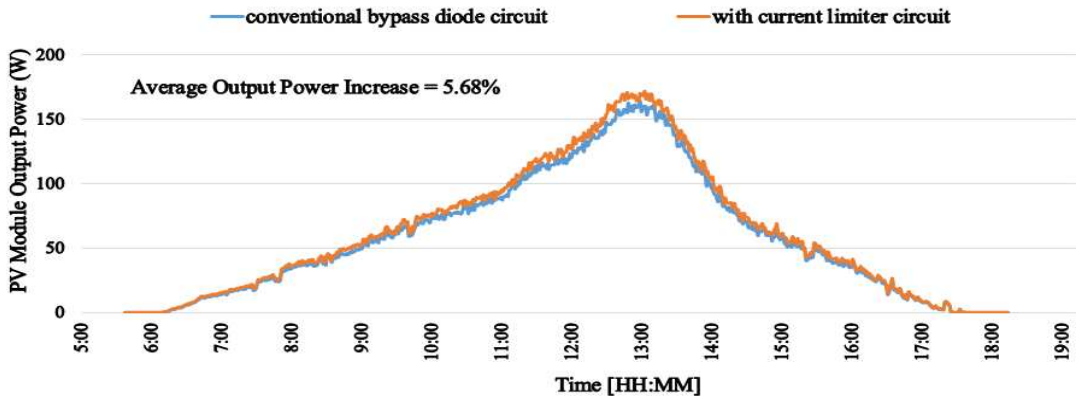


(c)

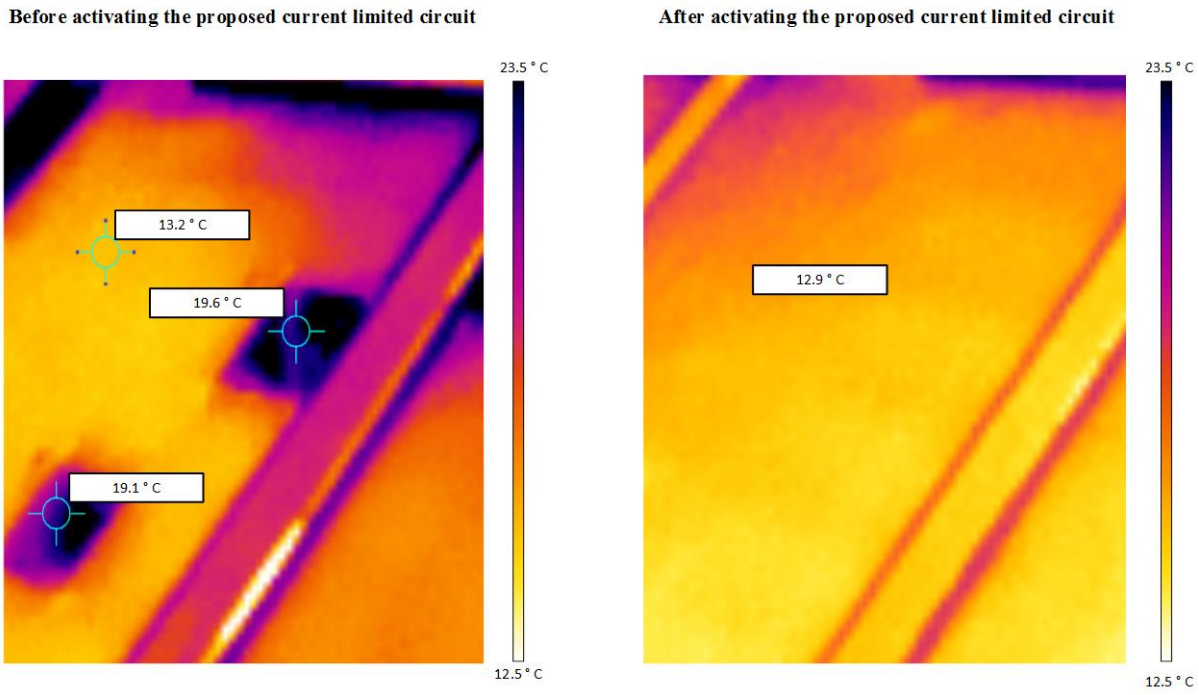


(d)

Fig. 12 (a) Measured V_{mpp}, **(b)** Measured I_{mpp}, **(c)** Measured P_{mpp}, **(d)** PV modules measured output power

277 In order to test the Feasibility of the proposed method to overcome the hot-spotting
278 phenomenon during partial shading conditions, we have examined the PV module shown in
279 **Fig. 11(a)**. The thermal image of the PV module before using the current limiter circuit is
280 shown in **Fig. 13(a)**. Since two solar cells are shaded by opaque object, hence, the shaded PV
281 cells electrically operate as load, and the electrical power is transformed into heat causing an
282 increase of the cells temperature from 19.1 to 19.6 °C. However, adjacent solar cells, non-
283 shaded cells, have a temperature of 13.2 °C.

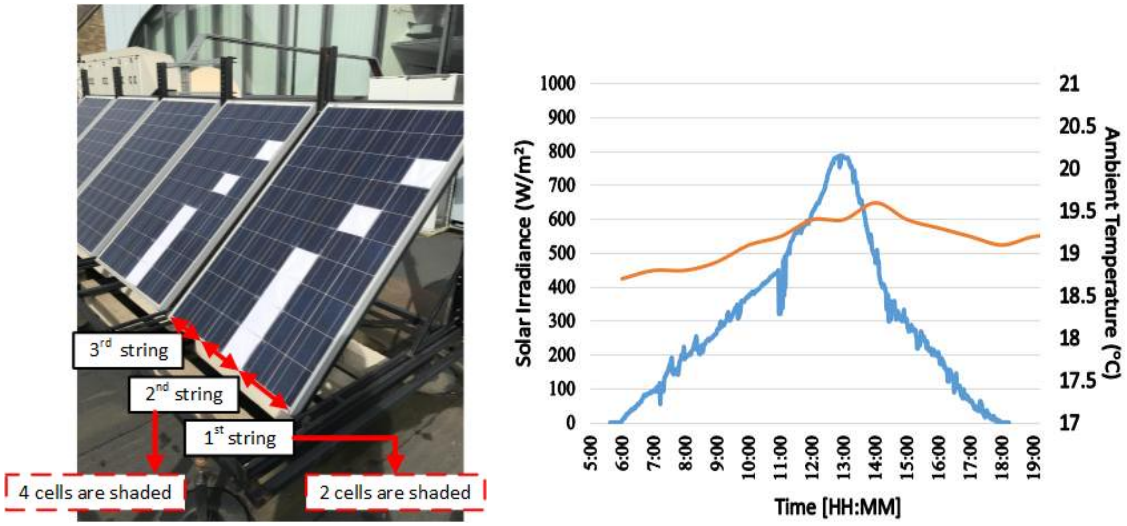
284 At this point, we have manually connected the PV module to the current limiter circuit in order
285 to test its impact on the hot-spots temperature. As shown in **Fig. 13(b)**, the PV module no
286 longer have the hot-spotted solar cells, in fact, this is due to the limitation of the current
287 controlled by the proposed technique. As a result, the PV module solar cells have a temperature
288 of 12.9 °C.



(a) **(b)**

Fig. 13 Impact of using the proposed current limiter circuit on the hot-spots of the PV module present due to the existence of partial shading. (a) Thermal image of the PV module before using the current limiter circuit, (b) Thermal image of the PV module after using the current limiter circuit

The second partial shading scenario is shown in **Fig. 14(a)**. Two and four solar cells are shaded in the first and second PV sub-strings, respectively. Same experiment is applied for the 2nd PV module equipped with the conventional bypass diode circuit. The Solar Irradiance and ambient temperature over the day is measured and presented in **Fig. 14(b)**.



(a) **(b)**

Fig. 14 (a) Shading scenario #2; two and four solar cells are shaded in the first and second PV sub-strings, subsequently, **(b)** Measured solar irradiance and ambient temperature during the experiment

As shown in **Fig. 15(a)**, the PV sub-strings output voltage is almost identical, with a very limited decrease in the V_{mpp} over the shaded PV sub-strings (#1 and #2). However, the output current shown in **Fig. 15(b)** has a drop in the first and second PV strings of the PV module equipped with the bypass diode circuit, while this drop in the output current is no longer exists for the PV module equipped with the proposed current limiter circuit. Consequently, it is expected to have a drop in the output power generated from the 1st and 2nd PV sub-strings as presented in **Fig. 15(c)**. The yielded output power has an average increase of 12.3% using the proposed circuit as presented in **Fig. 15(d)**. Indeed, this increase in the amount of power allied with the increase in the first and second PV sub-strings output current.

As a result, the output power enhancement in both shading scenarios #1 and #2 confirm the ability of the proposed current limiter circuit to increase the yielded power generation of the PV modules by mitigating the amount of the current distributed by the mismatched PV sub-string(s).

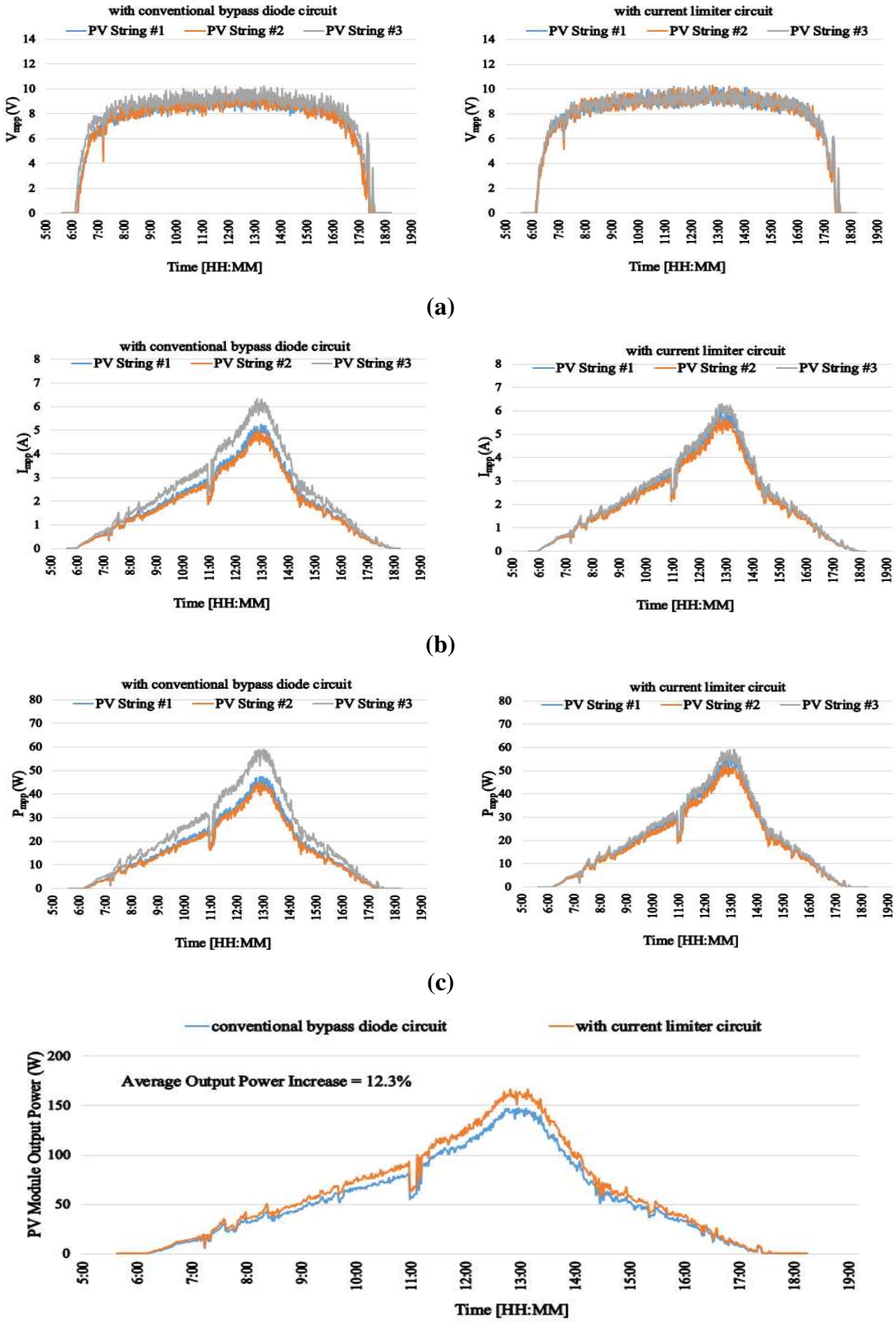


Fig. 15 (a) Measured V_{mpp}, **(b)** Measured I_{mpp}, **(c)** Measured P_{mpp}, **(d)** PV modules measured output power

4.2 PV Modules Affected by Hot-Spots

In this section, the current limiter circuit will be evaluated using two different PV modules affected by dissimilar hot-spotting type; namely one hot-spotted solar cell, and two hot-spotted solar cells.

The first examined PV module is affected by one hot-spotted solar cell. The thermal image of the hot-spot is shown in **Fig. 16(a)**. As noticed, the hot-spotted solar cell has a temperature of 21.3 °C, compared to adjacent healthy/non-hot-spotted solar cells of 16.2 °C. The proposed current limiter circuit were equipped in the PV module and as presented by the second thermal image, the hot-spot has been completely eliminated; the temperature of the PV module is equal to 15.3 °C. It is worth noting that the used thermal camera (FLIR i5) has a resolution of ±0.3 °C. By contrast with the results shown in Fig. 16(a), it is evident that the proposed circuit decreases the hot-spot temperature to equivalent with adjacent healthy solar cells. The removal of the hot-spots was guaranteed since the current limiter circuit mitigates the mismatched current flowing through the PV sub-strings, subsequently, warrant an equivalent amount of current flowing into all solar cells.

At first stage the PV module was connected to the conventional bypass diode circuit. Manually, we have reconnected the PV module sub-strings to the current limiter circuit. The solar irradiance during the experiment was fixed at 670 W/m^2. Here, we have to ensure that the solar irradiance does not change since any variations of the solar irradiance would impact the temperature of the hot-spotted solar cell as well as the amount of current passing though the hot-spotted PV sub-string. Therefore, the selected duration of the experiment lasts for a period of only 1 minute. This procedure was reconsidered while examining the second PV module affected by a different hot-spot type as shown in **Fig. 17(a)**.

Fig. 16(b) shows the results of the PV hot-spotted module while the PV sub-string is connected with the conventional bypass diode and the current limiter circuit; 1200 samples were taken, each sample is measured over a period of 50 ms. Therefore, the experiment duration is equal to 1200 x 50 ms = 1 minute. Remarkably, there is an increase of 14.2% in the output measured current due to the integration the proposed circuit with the PV module. Hence, this increase in the output current would result an increase in the output power generated by the PV module.

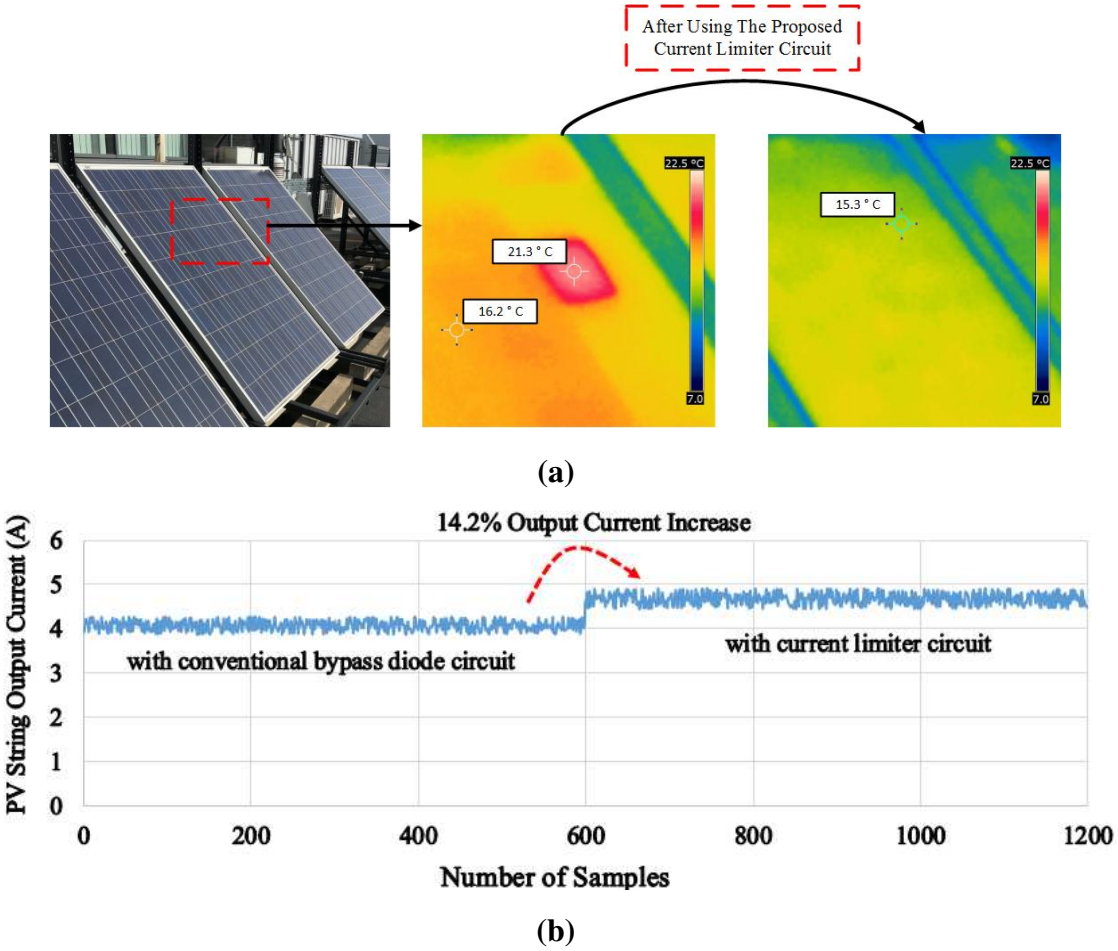
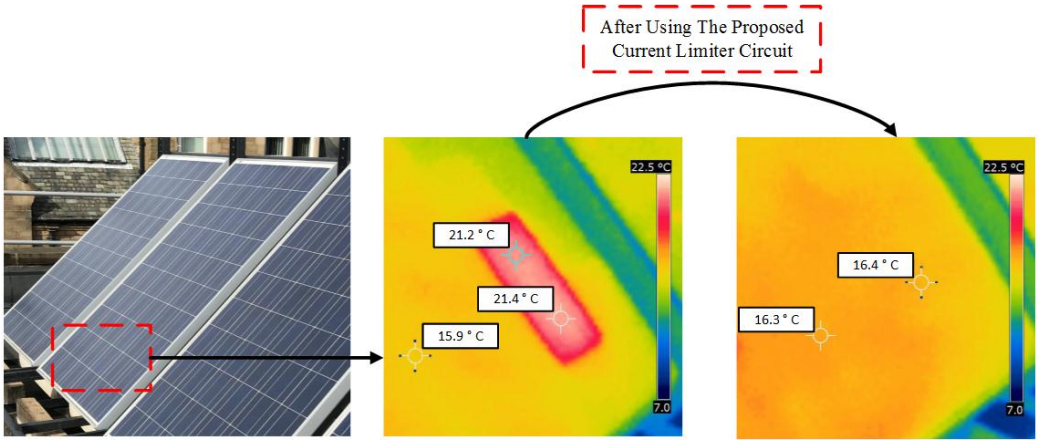


Fig. 16 (a) Thermal image of PV module affected by one hot-spotted solar cell, **(b)** Output current measurements

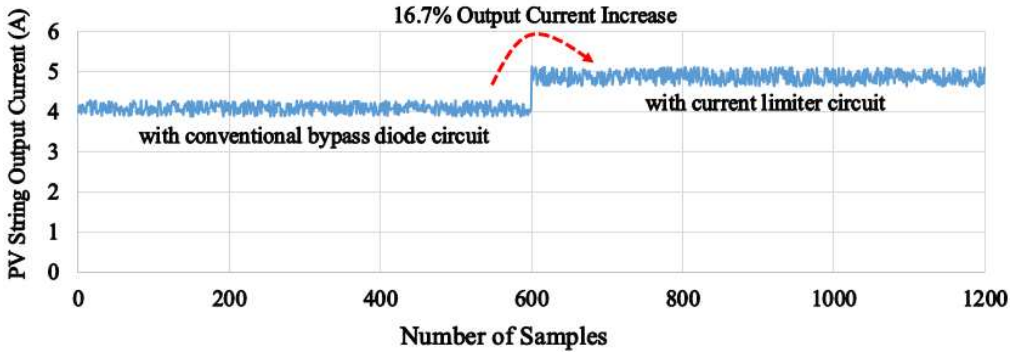
The second examined PV module is affected by two hot-spotted solar cells; thermal image of the hot-spots are shown in **Fig. 17(a)**. The temperature of the hot-spots is ranging from 21.2~21.4 °C, compared to adjacent healthy/non-hot-spotted solar cells of 15.9 °C. In addition, the solar irradiance during the experiment was fixed at 677 W/m^2.

The proposed current limiter circuit were equipped with the PV module and as shown by the second thermal image, both hot-spots have been eliminated. The temperature of the PV module has been mitigated to 16.4 °C. Furthermore, there is an increase of 16.7% in the output measured current due to the integration of the current limiter circuit in the PV module, results are shown in **Fig. 17(b)**.

Despite the fact that the proposed current limiter circuit eliminates the hot-spots in the PV modules as well as increase the output power during partial shading scenarios, yet, it pays off an additional cost, practically speaking, there is a certain amount of power dissipation that would be lost during the mitigation/current-limitation process.



(a)



(b)

Fig. 17 (a) Thermal image of PV module affected by two hot-spotted solar cells, **(b)** Output current measurements

The dissipated power of the PV module equipped with the current limiter circuit vs. the conventional bypass diode circuit are shown in **Fig. 18(c)**, the experimental setup is shown in **Fig. 18(a)** where two solar cells are shaded by an opaque object. The test lasts for an hour; sampling rate: 1 sample/second. As noticed, the average power dissipation is equal to 0.16 W and 0.05 W using the current limiter and the conventional bypass diode circuit, respectively.

Theoretically, the forward voltage drop of the conventional bypass diode for a PV sub-string is equal to 25 mV typically at 1~8 A dc load. Since we have connected the PV module with 2 A dc load, the power dissipation of the conventional bypass diode circuit shown in **Fig. 18(c)** is measured by (7).

$$P_{dissipation}(conventional\ bypass\ diode\ circuit) = 25\ \text{mV}\ (only\ one\ PV\ sub-string\ is\ affected\ by\ shading) \times I_{load}(2\ \text{A}) = 0.05\ \text{W} \quad (7)$$

In order to measure the total power dissipation of the proposed current limiter circuit, the voltage drop across the Q1 MOSFET and R_{sense} is measured. As shown previously in **Fig. 10**,

the circuit has three output pins to allow reading the total voltage drop in each of the PV module sub-strings. Accordingly, **Fig 18(b)** shows that the average voltage drop of 0.08 V occur in the first sub-string due to the existence of partial shading on this particular sub-string, hence the circuit has been automatically activated. On the other hand, the second and third sub-strings have a voltage drop of 0 V, since both sub-strings are not affected by partial shading.

The total power dissipated by the current limiter circuit is calculated using (8), where V_{drop} is the total voltage of Q1 MOSFET and R_{sense} of the current limiter circuit and I_{load} is the load current.

$$P_{dissipation}(proposed\ method) = \left[(V_{drop}\ 1^{st} sub-string) + (V_{drop}\ 2^{nd} sub-string) + (V_{drop}\ 3^{rd} sub-string)\right] \times I_{load} = [\,(0.08\ \text{V}) + (0\ \text{V}) + (0\ \text{V})] \times 2\ \text{A} = 0.16\ \text{W} \quad (8)$$

As a result, the power dissipation calculated using (8) is identical with the average power dissipation shown in **Fig.18(c)**.

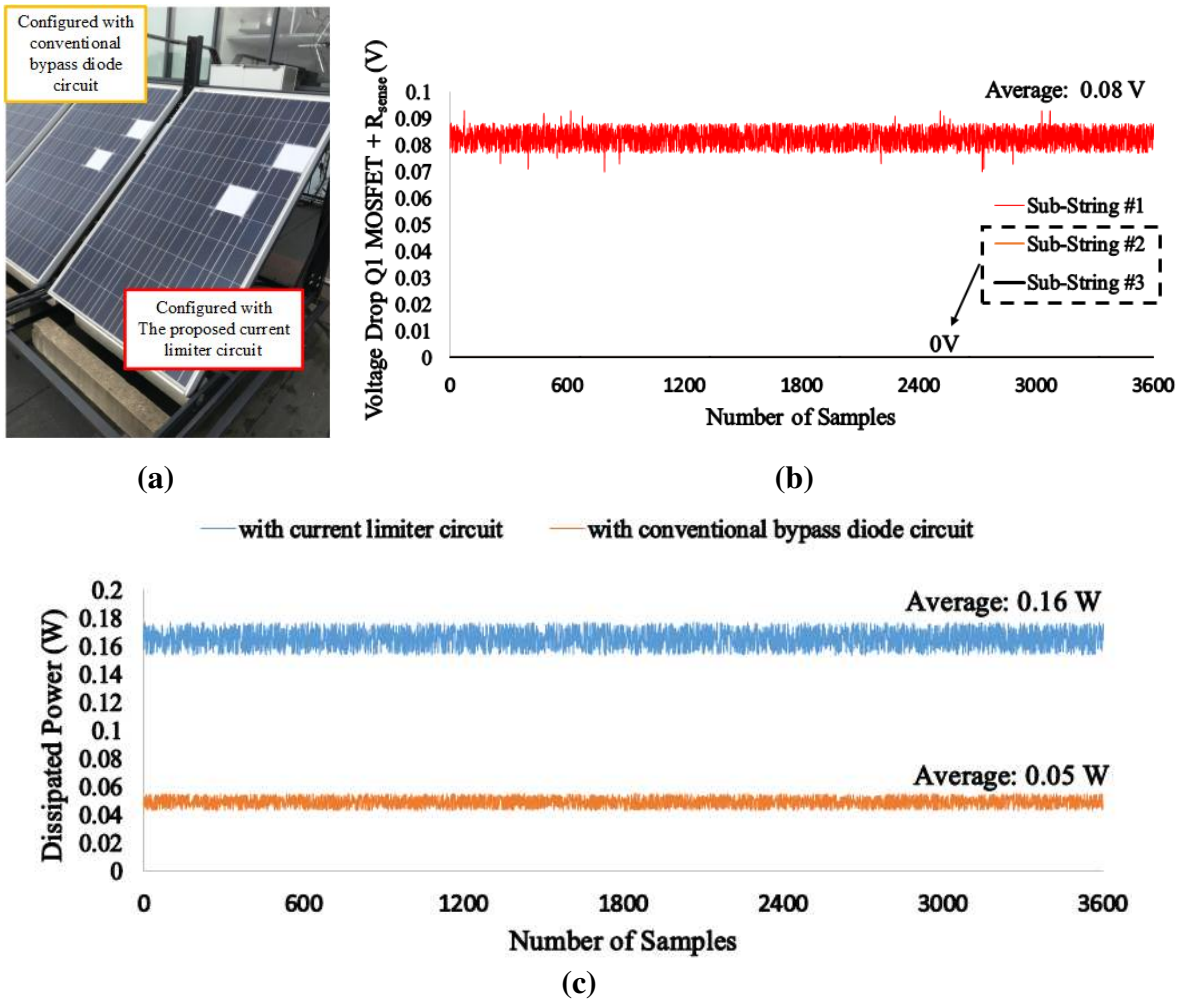


Fig. 18 (a) Experimental setup, **(b)** Total voltage drop in the current limiter circuit, **(c)** Comparison of the power dissipation

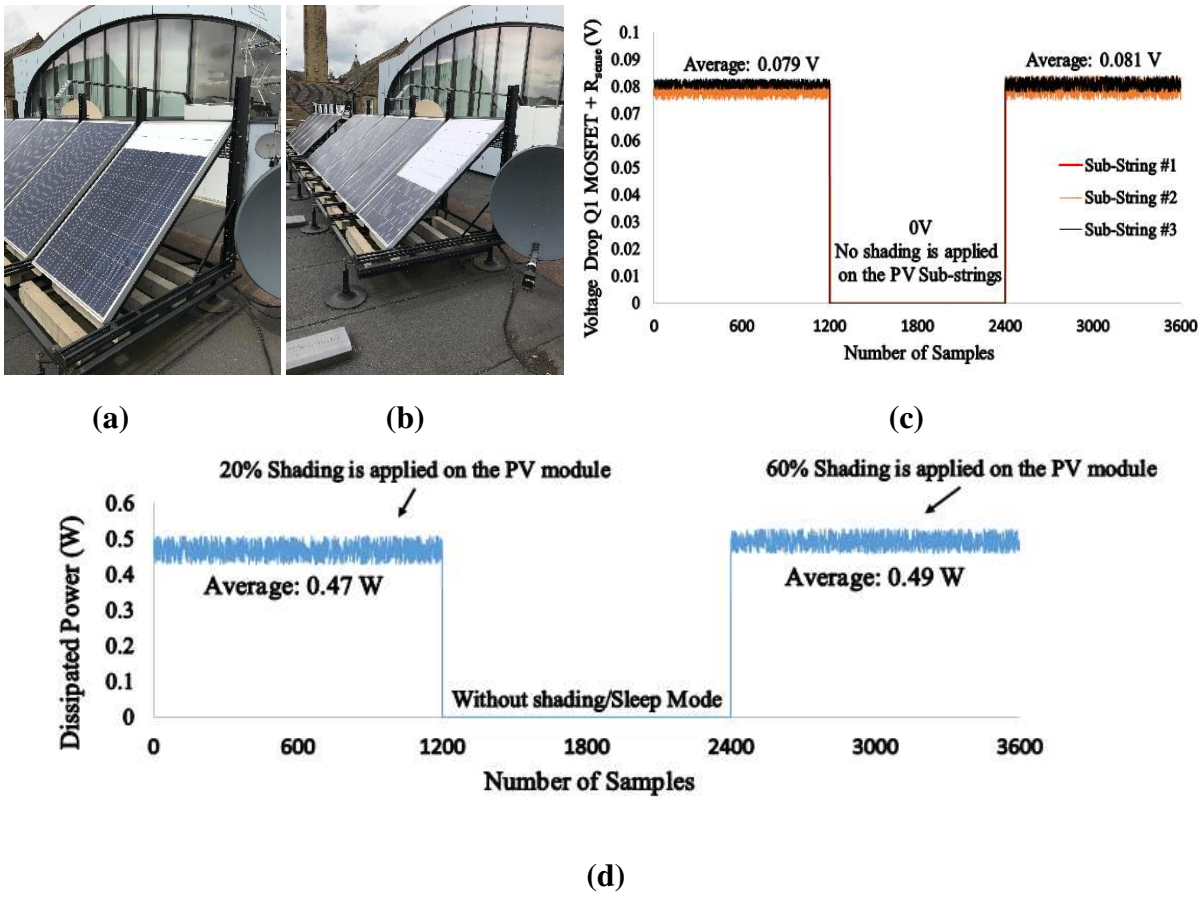
In this regard, it is worth noting that the actual power dissipation of the proposed current limiter circuit is dependent on the number of PV sub-strings affected by shading or hot-spotting condition. By contrast, we have examined a PV module under three different scenarios, where each scenario lasts for 20 minutes:

1) PV module affected by 20% shading condition; see **Fig. 19(a)**.
2) No shading is applied.
3) PV module affected by 60% shading condition; see **Fig. 19(b)**.

Since the same partial shading has been applied on all the PV module sub-strings, the voltage drop across Q1 MOSFET and R_{sence} are almost identical. The average V_{drop} is equal to 0.079 V during 20% shading, while the V_{drop} slightly increase to 0.081 V during 60% shading. Therefore, it is possible to calculate the power dissipation of the PV module during both experiments using (9) and (10), respectively.

$$P_{dissipation}(20\%\ shading) = [\,(0.079\ \text{V}) + (0.079\ \text{V}) + (0.079\ \text{V})] \times 2\ \text{A} = 0.474\ \text{W} \quad (9)$$

$$P_{dissipation}(60\%\ shading) = [\,(0.081\ \text{V}) + (0.081\ \text{V}) + (0.081\ \text{V})] \times 2\ \text{A} = 0.486\ \text{W} \quad (10)$$



(a) **(b)** **(c)**

(d)

Fig. 19 (a) 20% shading is applied on the PV module, **(b)** 60% shading is applied on the PV module, **(c)** Output power dissipation of the current limiter circuit

As presented in **Fig. 19(c)**, in the first case, the average power dissipation of the current limiter circuit is equal to 0.47 W, equivalent to the calculated power dissipation by (9). In the second experiment, the circuit is inactivated "sleep mode", and since the PV module has no shading, the power dissipation of the current limiter circuit is equal to 0 W, while the V_{drop} is equal to 0 V in all PV module sub-strings. The third experiment, where the PV module is examined under 60% shading condition, the average measured power dissipation of the circuit is equal to 0.49 W, nearly identical to the calculated power dissipation using (10).

5. Conclusion

In this paper a new current limiter circuit has been presented to overcome partial shading and hot-spotting scenarios affecting PV modules. The circuit prevents the limited current generated during partial shading conditions, and eliminating the hot-spots of the PV modules by decreasing its temperature level. With respect to other solutions based on different principles, the proposed circuit has an automatic control behaviour, in the sense that is self-triggering when mismatch conditions such as partial shading or hot-spotting occur in the PV modules.

The biggest advantages of the proposed circuit that it does not need any processing unit such as microcontrollers, or any other complex logic circuit implementation. In addition, the developed circuit has a very limited forward voltage drop compared with conventional bypass diodes such as Schottky diodes. It was shown that the actual drop of less than 0.24 V at 2 A of current is required to function the circuit which translates into a typical maximum power dissipation of 0.5 W.

The current limiter circuit was experimentally validated using various scenarios. During partial shading conditions, it was evident that the proposed circuit enhances the output generated power by 15% compared to conventional bypass diodes. While, the circuit could also eliminate PV hot-spots, evidently reduces the abnormal PV hot-spots temperature to equivalent the adjacent non-hot-spotted solar cells temperature.

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