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Necessary conditions for steep switching in a constant Resistor-Capacitor RCFET

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Abstract

We establish that the phenomenon of transient negative capacitance, conventionally linked to the delay in the response of a domain switching, of a ferroelectric material, and modelled by a non-linear capacitor, can in fact be considered to be more generally applicable to any phenomenon that can be represented by an RC-equivalent circuit. We demonstrate the conditions for sub-60 mV/dec switching in an RC-FET, even if the R and C were constant along both forward and backward sweeps. For semiconductor charge Q_{ch} , we show that the necessary condition for sub-60 mV/dec switching $(dQ_{\text{ch}})/(d\Psi_s) = (q/(k_B T))Q_{\text{ch}}$, where Ψ_s is the surface potential, is possible only if $Q_{\text{ch}} > 0$ (i.e. when the transistor is ON) during the backward sweep. This insight contributes further understanding on the causes of hysteresis in commonly used SPICE models of FE-FETs.

Introduction

Current research in negative capacitance phenomena is focussed on attempts to eliminate hysteresis in negative capacitance FETs (NCFETs), whilst achieving Steep Sub-threshold (SS) characteristics well below 60 mV/decade. Ferroelectric (FE) materials such as HfZrO are fully compatible with CMOS and their ease of integration makes them a promising technology to continue voltage scaling below the 5 nm technology node [1]. The sub-60mV/dec behaviour observed in NCFETs can result from the following mechanisms: (1) Negative permittivity or the S shaped behaviour in a single-domain FE [2] under quasi-static conditions as governed by the Landau-Khalatnikov (LK) equation [3], (2) transient negative capacitance in a multi-domain FE or even a paraelectric [4] as represented historically by the Miller model [5–7] via a non-negative series R – C circuit. In fact, even organic or solid-electrolyte FETs, with a redox mechanism in the gate insulator [8] have been demonstrated with sub-60 mV/dec behaviour by us in [9]. Similar to FEFET, these devices can also be represented by an R – C circuit. 3) In practice transfer characteristics of FEFET are always

measured in non-quasi-static conditions with a finite scan rate. In this case, the sub-threshold slope depends upon both intrinsic negative permittivity as well as transient negative capacitance as a consequence of the scan rate. Therefore, an FEFET is a combination of both cases (1) and (2). FETs utilising negative permittivity promise hysteresis-free sub-60 mV/dec [10, 11], that is typically observed at smaller scan rate or frequency of gate bias sweep, only if the negative capacitance is stabilised. However, if the negative capacitance is not stabilised, these FETs can still exhibit sub-60 mV/dec in both directions of gate bias sweep, albeit with a hysteresis in the transfer characteristics [10, 12], *irrespective of how slowly the gate bias is scanned*. As the scan rate of gate bias is increased, the transient negative capacitance also starts to play a role because of the finite time it takes for the polarisation to switch that gives rise to a resistor in series with the capacitor of FE. This interplay of the two mechanisms typically results in improvement in SS during the backward sweep but a degradation during the forward sweep and eventually causes it to become greater than 60mV/dec at sufficiently high frequency of gate bias [9]. In case 2, the sub-60mV/dec arising purely from transient negative capacitance is often accompanied by a counter-clockwise hysteresis in the transient transfer characteristics unless it has been offset by trap-induced hysteresis in the clockwise direction [6].

To achieve hysteresis-free operation, the steep switching behaviour arising from a purely negative permittivity in a ferroelectric material is required to be separated from

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the one that stems from transient negative capacitance as expressed by the Miller model. The phenomenon of transient negative capacitance, despite having completely disparate origins in the case of multi-domain as opposed to single-domain ferroelectric, remains closely interlinked with negative capacitance. The single-domain regime, which is governed by the LK equation, can be expressed by a series R – C circuit in parallel with an oxide capacitor C_{ox} , where C is considered non-linear and can attain negative values for a certain range of polarisation or can even be positive to yield steep switching [13]. In contrast, the multi-domain approximation is modelled by the Kolmogorov–Avrami–Ishibashi (KAI) model, which utilises a time-dependent polarisation [14] or the Miller model [15], which akin to the LK framework, can be equivalently described as a series R – C circuit. In the Miller model, where the gate insulator can be expressed as an R – C circuit, the C remains strictly greater than 0. During the transient sweep, the delay introduced by the R – C circuit leads to scenarios where a change in the surface potential of the semiconductor channel becomes greater than that of the gate bias, thus resulting in a body factor of less than 1. Equivalently, the voltage across the gate insulator changes in a direction that is opposite to both the applied gate bias and the surface potential of the semiconductor channel to accommodate this amplification. Since the surface potential directly affects the charge density in the channel, we can also say that the voltage across the insulator changes in the direction opposite to the change in the charge density in the channel, thus producing a transient negative capacitance. This phenomenon emerges purely from a delay introduced within the gate insulator. In different variations of such models at least one of the elements between R and C is always considered non-linear (with respect to polarisation) [13] to help explain the steep switching behaviour.

Here we establish that the phenomenon of transient negative capacitance can be considered more general than reported earlier. We demonstrate the conditions for sub-60 mV/dec switching in an RC-FET, even if both the R and C are constant.

Methodology

A schematic of a typical RC-FET gate stack is shown in Fig. 1a. In addition to an oxide capacitor C_{ox} , the equivalent circuit of a gate dielectric also contains another branch with a series R – C circuit. Similar to a conventional n-MOSFET, an application of gate voltage V_{GS} induces a sheet charge density Q_{ch} of mobile carriers in the channel. When a voltage V_{DS} is applied across its drain and source terminals, we observe a current I_{DS} , owing to the presence of these mobile carriers in the channel.

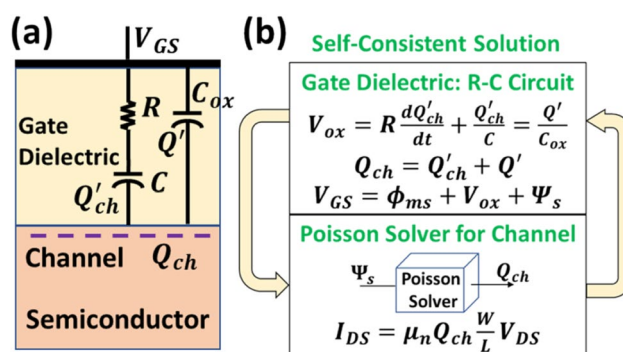


Fig. 1 **a** Schematic of the gate stack of an RC-FET. **b** Self-consistent solution of the gate insulator equivalent circuit, with the Poisson solver within the semiconductor channel

To calculate the current and the transfer characteristics, we solve the equation of the R – C circuit of the gate dielectric in conjunction with the Poisson solver in the semiconductor channel, in a self-consistent manner, as illustrated in Fig. 1b. Q_{ch} consists of two terms Q'_{ch} and Q' that are contributed by the two branches of the equivalent circuit in gate oxide, consisting of the elements R – C in series and C_{ox} (see Fig. 1 (a)). The gate voltage V_{GS} is dropped across the gate oxide V_{ox} , work function between the gate metal and the semiconductor Φ_{ms} and the surface potential Ψ_s at the semiconductor channel as

$$V_{GS} = \phi_{ms} + V_{ox} + \Psi_s \quad (1)$$

Poisson solver for the channel takes Ψ_s as input and produces Q_{ch} as output, given the energy band parameters of the semiconductor.

The simulations in this work are generated for fixed values of the oxide and semiconductor parameters, R , C , and C_{ox} as $6.26 M\Omega \cdot cm^2$, $3.19 \mu F/cm^2$, and $67 nF/cm^2$, derived from a Solid Electrolyte FET that shows steep switching via a redox mechanism in the insulator [9]. Nevertheless, the results can be generalised to any other values, but would apply under a different range of scan rate of the gate voltage, as will be proven by deriving the conditions for the body factor (m) to become less than unity.

Results and discussion

The simulated transfer characteristics of the RC-FET from the self-consistent model for different sweep rates of the gate voltage are plotted in Fig. 2. At extremely low scan rate (quasi-static), any delay introduced by the series R – C branch becomes inconsequential and a large capacitor $C \gg C_{ox}$ in this branch induces a very high charge in the channel, thereby producing the highest possible I_{DS} at any given V_{GS} in the forward sweep. During the backward sweep the I_{DS} simply retraces its

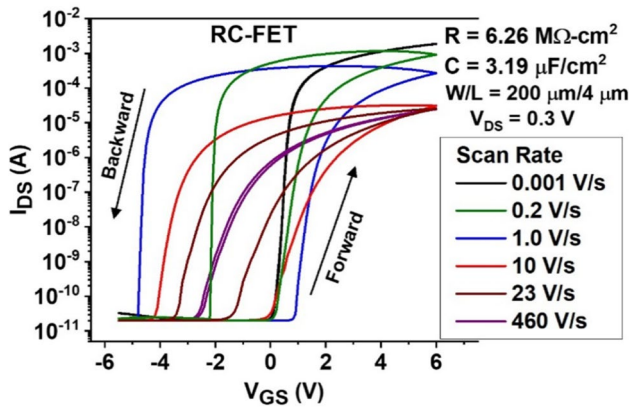


Fig. 2 Transfer characteristic of an RCFET at different scan rates of gate bias V_{GS}

value, owing to almost no delay in the discharging of C , at this extremely slow scan rate.

As the scan rate of the gate voltage is increased, a delay in the R – C circuit results in a counter-clockwise hysteresis, with the subthreshold slopes during the forward and backward sweeps becoming gentler and steeper, respectively. This trend continues up to a scan rate of 1.0V/s , where the counter-clockwise hysteresis becomes the widest, whilst the subthreshold slope in the backward sweep falls below 60mV/dec . For the scan rate beyond this point, the delay introduced by the R – C becomes so large that very little charging or discharging of C in this branch takes place, leading to a decline in the width of the hysteresis and the subthreshold slope in the backward sweep. At the maximum scan rate of 460V/s , the delay in the R – C becomes so large that this branch almost becomes non-responsive to the changes in gate voltage, and most of the charge in the semiconductor is now induced by C_{ox} . Thus, the coupling of the gate to the semiconductor reduces to that of a typical MOS capacitor, without any 60mV/dec switching. Since these transfer characteristics correspond to a slow-switching SE-FET, the transfer characteristics reduce to that of a MOSFET at relatively smaller scan rate owing to a large R in the mega-ohm range. If, however, R is reduced to a few ohms for instance, the scan rate will also be boosted by 6 orders of magnitude.

To understand the behaviour of the subthreshold slope in the forward and backward sweeps, the gate dielectric of the RC-FET is first approximated at its limits of low and high scan rates. Following Fig. 1 (a), the mobile sheet charge density in the channel Q_{ch} can be described as the sum of the charge densities contributed by the two branches of the equivalent circuit in the gate oxide:

$$Q_{ch} = Q' + Q'_{ch} = C_{ox}V_{ox} + Q'_{ch} \quad (2)$$

The voltage drop across the gate oxide V_{ox} can be described as:

$$V_{ox} = R \frac{dQ'_{ch}}{dt} + \frac{Q'_{ch}}{C} \quad (3)$$

At low scan rate, $dV_{ox}/dt \rightarrow 0$, taking the derivative of Eq. (2) and substituting $dV_{ox}/dt = 0$,

$$\frac{dQ_{ch}}{dt} = \frac{dQ'_{ch}}{dt} \quad (4)$$

Substituting dQ'_{ch}/dt from Eq. (4) and Q'_{ch} from Eq. (2) into Eq. (3), yields

$$V_{ox} = R \frac{dQ_{ch}}{dt} + \frac{Q_{ch} - Q'}{C} \quad (5)$$

Since we assume $C \gg C_{ox}$, the charge density contributed by the series R – C branch in the limit of a low scan rate is much larger than that in the branch containing C_{ox} . Thus Eq. (5) can be further simplified to

$$V_{ox} = R \frac{dQ_{ch}}{dt} + \frac{Q_{ch}}{C} \quad (6)$$

Hence, at low scan rate, the gate oxide circuit behaves simply as a series R – C circuit, having a negligible influence from the parallel capacitor C_{ox} . Similarly, to derive an expression at a high scan rate ($dV_{ox}/dt \rightarrow \infty$), we first take the derivative of Eq. (2) with respect to V_{ox} to yield

$$\frac{dQ_{ch}}{dV_{ox}} = C_{ox} + \frac{dQ'_{ch}/dt}{dV_{ox}/dt} \quad (7)$$

Substituting dQ'_{ch}/dt from Eq. (3), and Q'_{ch} from Eq. (2) this results in

$$\frac{dQ_{ch}}{dV_{ox}} = C_{ox} + \frac{1}{RC} \frac{(C + C_{ox})V_{ox} - Q_{ch}}{dV_{ox}/dt} \quad (8)$$

Finally, in the limit of $dV_{ox}/dt \rightarrow \infty$, the above reduces to

$$\frac{dQ_{ch}}{dV_{ox}} \approx C_{ox} \quad (9)$$

Hence in the limit of a high scan rate, the behaviour of the gate oxide reduces to that of an oxide capacitor, thus confirming the behaviour observed in Fig. 2, at a scan rate of 460V/s .

To understand the mechanism of steep subthreshold switching, we next investigate how the behaviour of the coupling between the gate and the semiconductor varies with scan rates, in the limit where the scan rate remains so low that V_{ox} can be described by Eq. (6). Differentiating

this equation with respect to the surface potential of the semiconductor Ψ_s leads to

$$\frac{dV_{ox}}{d\Psi_s} = R \frac{d}{d\Psi_s} \frac{dQ_{ch}}{dt} + \frac{1}{C} \frac{dQ_{ch}}{d\Psi_s} \quad (10)$$

In the subthreshold regime, the dependence between Q_{ch} and Ψ_s that is governed by the Poisson equation (see Fig. 1 (b)), can be simplified to an exponential dependence as

$$Q_{ch} \approx Q_0 \exp\left(\frac{q\Psi_s}{k_B T}\right) \quad (11)$$

where Q_0 and k_B are the intrinsic charge density of the semiconductor and Boltzmann constant, respectively. Differentiating Eq. (11) with respect to Ψ_s and substituting the result for $dQ_{ch}/d\Psi_s$ in Eq. (10) gives:

$$\frac{dV_{ox}}{d\Psi_s} = R \left(\frac{q}{k_B T}\right)^2 Q_{ch} \frac{d\Psi_s}{dt} + \frac{1}{C} \left(\frac{q}{k_B T}\right) Q_{ch} \quad (12)$$

In the first term on the right-hand side, we have leveraged the chain rule to first write dQ_{ch}/dt as $[(dQ_{ch}/d\Psi_s)(d\Psi_s/dt)]$ before applying the differentiation with respect to Ψ_s . We have also ignored the contribution from the term $d^2\Psi_s/d\Psi_s dt$ in the limit of a small scan rate. For the body factor m , to become less than unity, we must have $m = dV_{GS}/d\Psi_s < 1$ or $dV_{ox}/d\Psi_s < 0$, following Eq. (1). Substituting this into Eq. (12) results in

$$Q_{ch} \frac{d\Psi_s}{dt} < -\frac{k_B T}{qRC} Q_{ch} \quad (13)$$

Again, for the body factor $m = dV_{GS}/d\Psi_s$ to be less than unity we must also have:

$$\frac{dV_{GS}}{d\Psi_s} < 1 \Rightarrow \frac{dV_{GS}}{dt} < \frac{d\Psi_s}{dt} \quad (14)$$

If $Q_{ch} > 0$, we can drop Q_{ch} from both the sides of Eq. (13) without changing the direction of inequality, and utilising Eq. (14), we arrive at

$$\frac{dV_{GS}}{dt} < \frac{d\Psi_s}{dt} < -\frac{k_B T}{qRC} \quad (15)$$

Equation (15) represents the condition for the body factor to be less than unity when $Q_{ch} > 0$ i.e. when the device is in the ON state. In the above equation, since dV_{GS}/dt is negative, it signifies that Eq. (15) is only applicable during the backward sweep. Equation (13) also presents another condition when $Q_{ch} < 0$, i.e. when the device is in OFF state. With $Q_{ch} < 0$, dropping Q_{ch} from both the sides results in flipping of the inequality sign, thereby leading to the desired expression:

$$\frac{d\Psi_s}{dt} > -\frac{k_B T}{qRC} \quad (16)$$

Since the device remains OFF during the above condition, the transfer characteristics show no steep switching, even though the body factor is less than unity [3].

Figures 3a and b show the behaviour of V_{ox} with respect to V_{GS} for different scan rates during forward and backward sweeps, respectively. At extremely small scan rate of 0.001 V/s, the slope dV_{ox}/dV_{GS} remains greater than 0, throughout in both forward and backward sweeps, hence no steep switching is observed, as confirmed in Fig. 3. As the scan rate is increased, the regions with negative slopes start to emerge in both forward and backward sweeps, as seen for the scan rate of 0.2 and 1.0 V/s, responsible for driving the body factor below unity.

The body factor and the minimum subthreshold swing SS_{min} as a function of scan rate are plotted in Figs. 4 (a) and (b), respectively. The body factor shows a decline as the scan rate increases. During the backward sweep, that is $dV_{GS}/dt < 0$, as soon as the scan rate $|dV_{GS}/dt|$ increases beyond 0.0013 V/s the body factor becomes less than unity,

Fig. 3 $V_{ox} - V_{GS}$ curve in **a** forward and **b** backward sweeps at various scan rates, showing an emergence of the region of negative slope

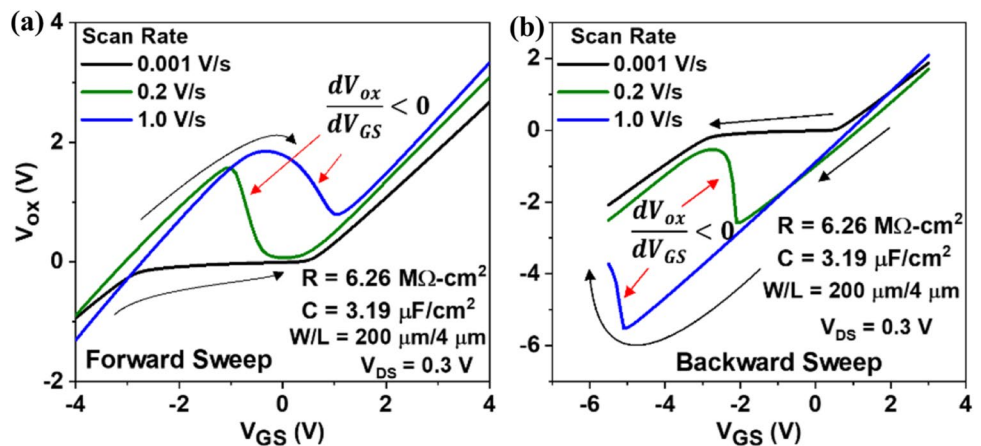
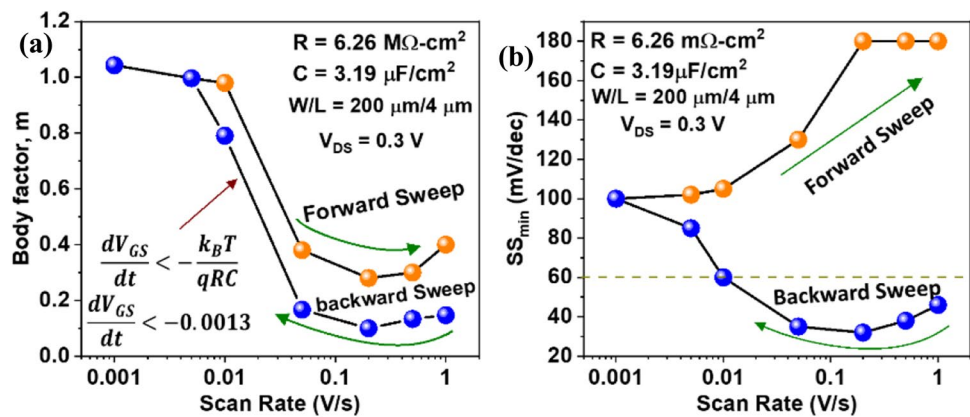


Fig. 4 Change in (a) body factor and (b) min subthreshold swing (SS_{min}) with scan rate. Whilst body factor becomes less than unity in both forward and backward sweeps, SS_{min} shows a decline only in backward sweep, in agreement with the derived conditions in Eqs. (15) and (16)



consistent with the derived condition in Eq. (15). This directly translates to a drop in SS_{min} , from 100 mV/dec to less than 60 mV/dec in the backward sweep. During the forward sweep, despite a body factor less than unity, SS_{min} shows no signs of decrease, in agreement with Eq. (16), which is only satisfied when the device remains in the OFF state ($Q_{ch} < 0$) and not in the subthreshold regime. A similar behaviour is noted in [6] of long channel FETs where they point out misalignment with the sub-threshold values of the surface potential as a cause of $SS > 60 \text{ mV/dec}$. Moreover, a wider hysteresis at higher scan rates causes a degradation in SS_{min} in the forward sweep.

Conclusion

The gate insulator of many steep switching devices, such as multi-domain FE-FETs, SE-FETs, and other organic FETs can often be reduced to an equivalent series R - C circuit. Here, we present a generic RC-FET device, with its gate insulator modelled as a series R - C circuit. We have shown that the transfer characteristics of such devices show sub- 60 mV/dec behaviour in the backward sweep and derive the conditions to explain this behaviour. Our results and the derived conditions conclusively establish that despite a promise to achieve a body factor below unity in both forward and backward sweeps, such devices that are affected by transient phenomena can only show sub- 60 mV/dec of SS during the backward sweep. We believe that our results will help distinguish the sub- 60 mV/dec behaviour originating either from negative capacitance or other redox mechanisms, resembling a series R - C circuit. Hence for the continuation of the supply voltage scaling, future research should focus on sub- 60 mV/dec behaviour in the forward sweep, as this

cannot be facilitated by the undesirable transient negative capacitance.

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