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ORIGINAL RESEARCH PAPER

An ultra-fast protection scheme for normally-on wide bandgap devices

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Abstract
Here, an ultra-fast protection scheme that is dedicated to depletion-mode (d-mode) devices is proposed. The key to the d-mode device gate drive design is the negative supply and overcurrent protection, due to the safety concern for d-mode devices when a failure happens in power conversion applications. This work evaluates specific requirement of d-mode devices, such as the isolated negative power supply and short-circuit protection. Normally-on d-mode GaN devices have lower on-resistance and minimal dead time in comparison with enhancement-mode (e-mode) GaN devices, which can further reduce the switching loss and conduction loss. Both simulation and experimental verification are conducted in this work to evaluate the performance of the proposed protection scheme. The proposed desaturation scheme can wipe out the overcurrent event within 341 ns. Furthermore, the proposed negative power supply scheme can sustain its output for 60.5 ms, providing sufficient action time for the control unit to isolate the converter.

1 | INTRODUCTION

Wide bandgap (WBG) technologies such as Gallium Nitride (GaN) or Silicon Carbide (SiC) as emerging candidates to achieve the higher switching frequency and higher efficiency than Silicon (Si) counterparts in power converters. GaN-based solutions enable a device with lower on-resistance and the smaller switching loss in comparison to that of Si for comparable current and voltage capabilities [1–3]. Furthermore, the inherent bidirectional current flow capability of GaN devices guarantees the interests of GaN for those applications, which require bidirectional switching operation, such as motor drives, EV chargers and server power supplies [4].

GaN devices can be classified into two types in terms of the gate structure: depletion-mode (d-mode) and enhancement-mode (e-mode). Due to the safety concern for most power conversion applications and complex gate drivers, the e-mode GaN device is more favourable. Lateral GaN high electron mobility transistors (HEMTs) are inherent d-mode devices. To enable the normally-off operation, several approaches have been developed, which include recessed-gate, Fluorine implantation and p-GaN gate [5–11]. Moreover, the cascode structure which consists of one low-voltage Si MOSFET and one high-voltage GaN HEMT has been proposed as a compromised option to achieve normally-off operation [12–14].

In comparison with e-mode GaN devices, d-mode GaN devices have lower on-resistance because the 2D electron gas (2DEG) is induced at GaN/AlGaN interface. In addition, the 2DEG does not have to be disrupted and re-created to turn on the device [15]. Therefore, it is worth developing and exploring d-mode GaN devices to fully enable all advantages that GaN brings. As aforementioned, the gate driver design poses difficulty towards the use of the d-mode GaN device. Several gate drive schemes with protection for normally-on device have been studied in [16–19], where the response time that is necessary to wipe out the fault condition is not faster enough to cope with the extremely fast WBG devices. This work proposes a gate driver design for normally-on GaN devices with effective protection in terms of the failure of negative gate voltage supply and the overcurrent/short-circuit event. Furthermore, GaN devices can exhibit the bidirectional current flow capability. In this work, both the desaturation and negative power supply protection circuits are applied to a 1.2 kV polarisation super-junction (PSJ) GaN FET [20, 21]. Since 1.2 kV PSJ GaN FETs have a limited current rating of 8A, a 650 V/85 A SiC JFET (UJ3N065025K3S) is used to validate the desaturation

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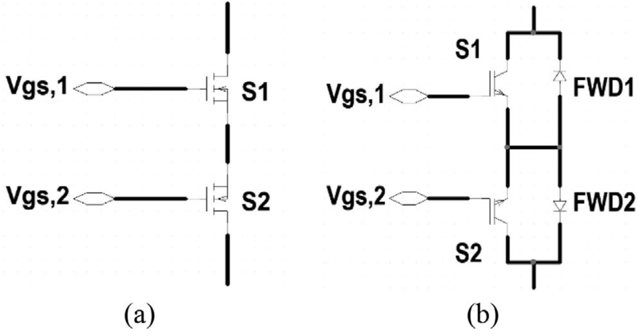

FIGURE 1 The schematic of bidirectional switching (BDS) module using (a) GaN-based; (b) IGBT-based

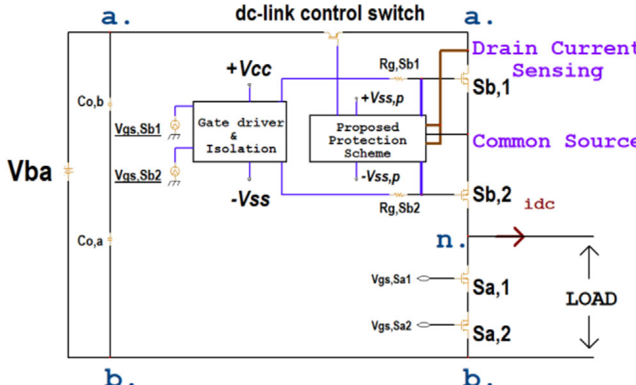

FIGURE 2 The implementation of the protection circuit for GaN-based bidirectional switching (BDS) module

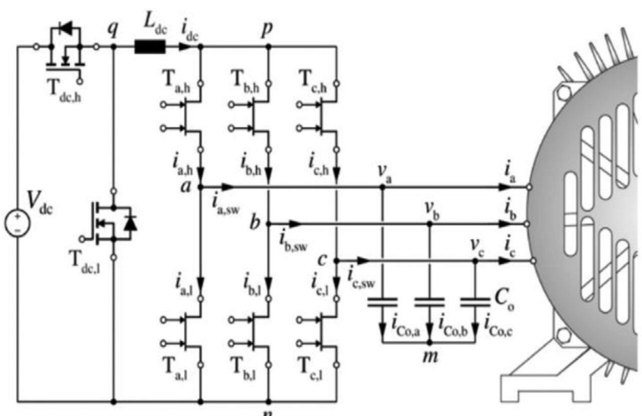

FIGURE 3 The schematic of three-phase buck-boost current source inverter (CSI) systems [23]

protection scheme for the higher current operation. Both simulated and experimental verification are conducted in this work to evaluate the proposed protection scheme.

2 | BIDIRECTIONAL SWITCHING MODULE USING GAN-BASED DEVICES

Different from traditional IGBT-based bidirectional switching modules, GaN devices are capable of bidirectional current flowing, which allows the elimination of external diodes. Figure 1 shows traditional IGBT-based and GaN-based bidirectional switching (BDS) module. The benefits of replacing IGBT with GaN FET for low voltage, high frequency applications can be concluded as following: First, the use of GaN FET can reduce the conduction loss owing to lower specific on-resistance compared to that of Si IGBT for given voltage rating and the absence of offset voltage; second, more efficient switching can be obtained due to GaN device is majority carrier device; last but not the least, it eliminates the antiparallel diode and therefore further reduces the loss caused by diode forward voltage drop [22].

As depicted in Figure 1, GaN-based switching module has no external free-wheeling diode. For example, when $V_{gs,1}$ is ON while $V_{gs,2}$ is OFF, current can still flow from the top toward the bottom.

3 | PROTECTION SCHEME FOR NORMALLY-ON WBG DEVICES

The proposed protection circuit is implemented in a single-phase (1-Φ) half-bridge as depicted in Figure 2, which is part of the low side switches of a three-phase (3-Φ) buck-boost inverter for industrial motor drives as shown in Figure 3 [21]. The GaN-based bidirectional module is constructed by two discrete GaN HEMT in source-to-source connection as $S_{a,1}$ and $S_{a,2}$ or $S_{b,1}$ and $S_{b,2}$ in Figure 3.

The proposed protection scheme consists of two parts: one is used to protect the device from short-circuit and overcurrent events, namely the desaturation scheme; another one is aimed to protect the negative voltage fail, so-called negative power supply protection scheme. This negative power supply is used to provide negative voltage for both the desaturation circuit and the gate drive circuit. The proposed desaturation circuit and negative power supply protection circuit are illustrated in Figure 4 and Figure 5 respectively. As the gate signals injected to $S_{x,1}$ and $S_{x,2}$ are not identical, separation of desaturation circuit for each switching device within one BDS module is desired.

With respect to the desaturation circuit, during normal operation, the comparator ($COMP_{desat}$) sends a logic '0' signal to the opto-coupler. The opto-coupler in response sends inverted logic 1 as an ENABLE (EN) signal to the gate driver of the device. As a result, the device will follow the gate driving signal (V_{gs_EN}) to turn on or off. Thanks to the combination of Complementary Metal-oxide-semiconductor (CMOS) module and MOSFET ($S_{comp,desat}$), the comparison between V_{ref} and V_{desat} via the comparator ($COMP_{desat}$) only occur when the Device Under Test (DUT) is ON. It is worth pointing out that the V_{gs_iso} injected to CMOS module is controlled by another isolated gate driver IC while it has identical shape of V_{gs_EN} during normal operation. When the device is in the OFF state, the MOSFET ($S_{comp,desat}$) is turned on and thereby the V_{desat} is pulled down to $-V_{ss}$ which is below V_{ref}. The high voltage diode D_{sense} with low voltage drop and fast recovery feature is aimed to monitor the

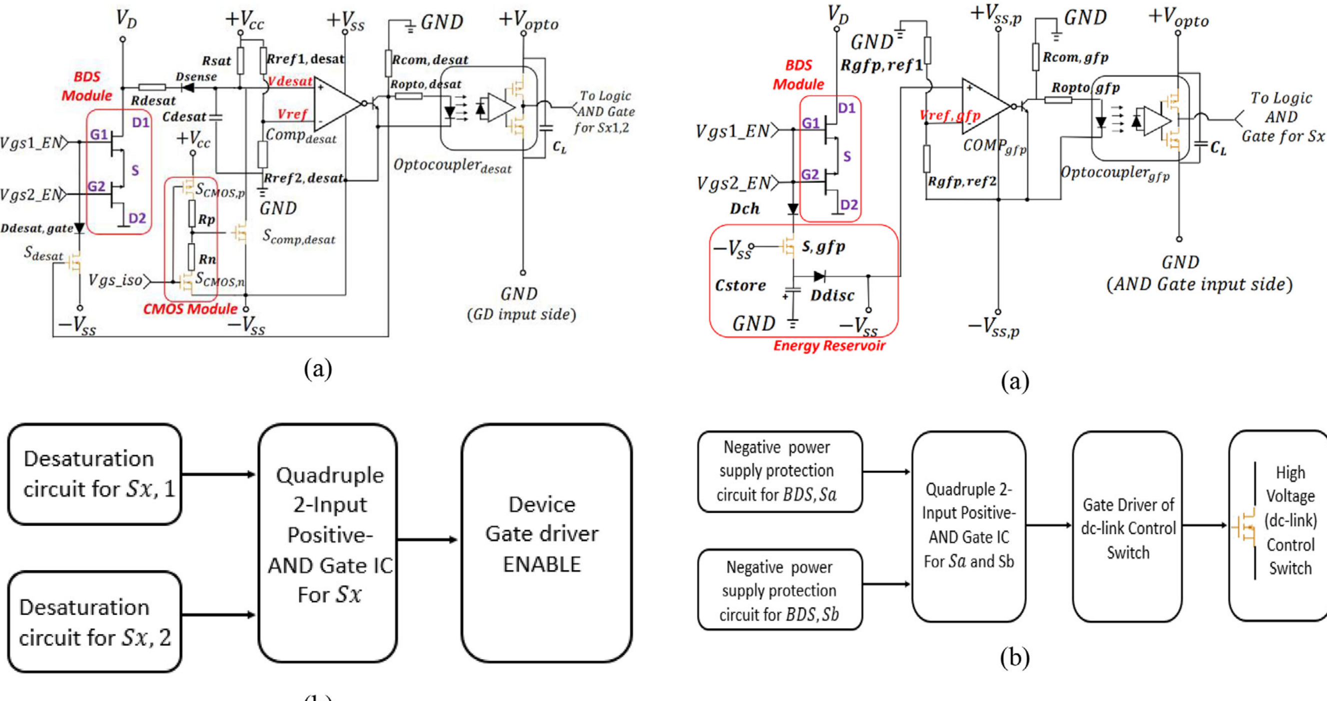

FIGURE 4 The proposed desaturation circuit for depletion-mode GaN device of (a) circuit diagram; (b) implementation block diagram

FIGURE 5 The proposed negative power supply protection scheme for GaN-based bidirectional switching module (a) circuit diagram; (b) implementation block diagram

drain current of the DUT. R_{desat} and C_{desat} perform as a low pass RC filter to stabilize the V_{desat} from noise. V_{ref} is set by the voltage divider constructed by two resistors, namely $R_{ref1,desat}$ and $R_{ref2,desat}$. This reference voltage determines the limit of drain current (I_{d_max}), and is used to compare with V_{desat}. Thus, the comparator ($COMP_{desast}$)in the desaturation circuit will produce a fault signal to opto-coupler and eventually pull-down the gate-to-source signal of the DUT. The most important objective in this desaturation circuit is the response time between V_{gs_EN} and V_{desat}. For instance, when V_{gs_EN} has been pulled down to $-V_{ss}$ by gate driving signal, while the MOSFET ($S_{comp,desat}$) is still turned-off, the V_{deast} is now equal to $+V_{CC}$. This results in a fault triggering of the desaturation circuit. This time is defined by V_{desat} rising to the steady-state level at a time constant. Where R is formed by R_{desat} and $R_{Dsense,on}$, and C is formed by C_{desat} and the output capacitance of $S_{comp,desat}$. Furthermore, by employing different resistor value in CMOS configuration can amend the turn-on and turn-off time of the MOSFET ($S_{comp,desat}$). The desired synchronisation of V_{gs_EN} and V_{desat} can be achieved by the MOSFET ($S_{comp,desat}$) with ultra-fast turn-on transition. The effectiveness of synchronisation of these two signals is the main limitation of the proposed desaturation scheme since it has direct impact on the response time. The value of V_{desat} during normal operation can be expressed as Equation (1).

$$V_{desat} = \frac{R_{sat}}{R_{sat} + R_{desat}} \left(V_{ds,on} + V_{D,sense}\right) + \frac{R_{desat}}{R_{sat} + R_{desat}} V_{CC} \tag{1}$$

The detailed operation of the desaturation circuit can be described as follows. When overcurrent events take place, the V_{desat} will rise above V_{ref}. Then a fault signal (logic 1) will be triggered by comparator ($COMP_{desat}$), since the IN+ of the comparator is now greater than IN-. This fault signal is received by the opto-coupler, and the opto-coupler sends logic '0′ signal toward the gate driver of the device to turn off the device via an AND gate IC. It is necessary to emphasise that every BDS module protection circuit including both desaturation circuit and negative power supply protection circuit only require one AND gate IC as BDS module is two-source connected. When the desaturation circuit is activated, the MOSFET (S_{desat}) will be triggered ON as well. Once this MOSFET is turned-on, the gate driving signal of the device will be pulled down towards $-V_{SS}$ to turn the device off.

Negative power supply protection circuit is designed to protect the desaturation circuit as well as provide the negative gate voltage for gate driver. When the negative voltage supply used for desaturation circuit and gate driver fail. The gate driver is unable to turn-off the d-mode bidirectional switching module anymore, and hence it cannot generate desired negative bias to switch-off the device. The detailed circuit of this negative power supply protection as illustrated in Figure 5, and the operation of the proposed negative power supply protection scheme can be described as follows. During normal operation, the MOSFET (S_{gfp}) stays in OFF state. It is because the reservoir capacitor (*Cstore*) is charged to $-V_{SS}$ via discharging diode (D_{disc}), and hereby the gate-to-source voltage is about zero during normal operation. Another comparator ($COMP_{gfp}$) with collector output is employed to monitor the state of the

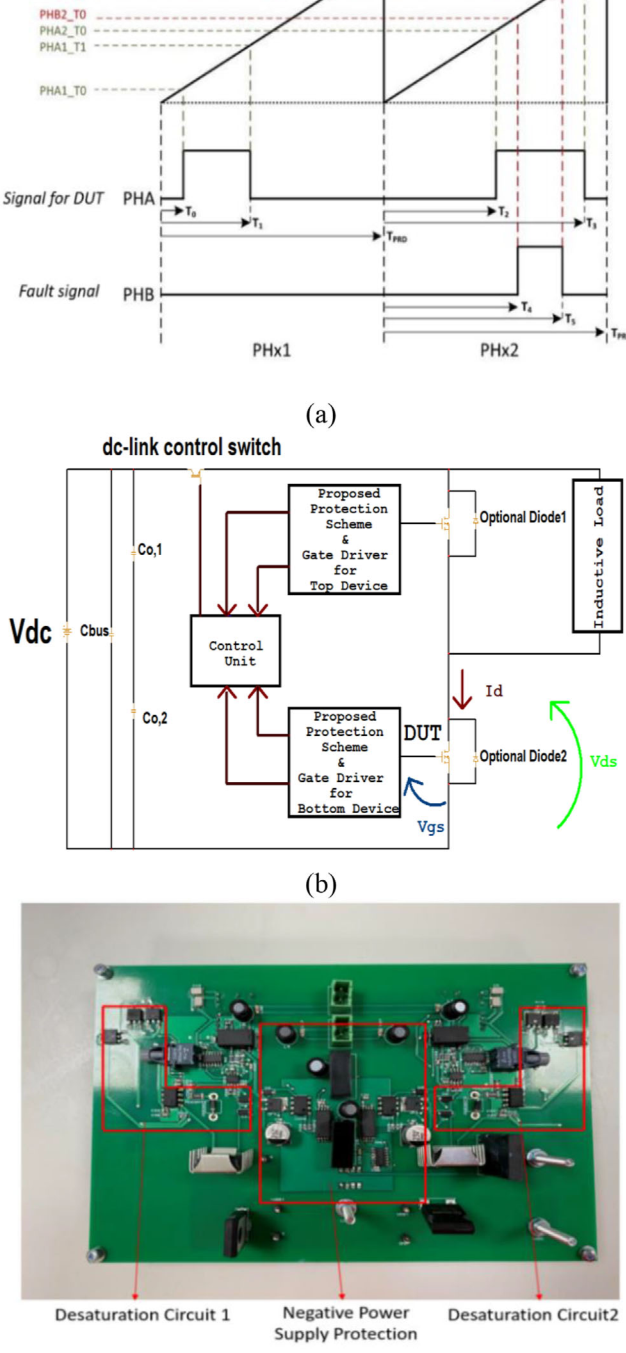

FIGURE 6 (a) Fault signal triggered by Ti F28027F; (b) experimental circuit; (c) top view of the practical PCB

negative power supply ($-V_{SS}$). As shown in Figure 6(a), the $-V_{SS}$ is connected to the positive input (IN+) of the comparator ($COMP_{gfp}$). An adjustable potential divider formed by two resistors is used to set the reference voltage and is connected to the negative input of the comparator ($COMP_{gfp}$), and this reference voltage ($-V_{ref_gfp}$) is below 0V. Since IN+ is lower than IN- in normal operation, the comparator sends logic 0 toward the opto-coupler. Hence, the opto-coupler outputs logic '1' to the AND gate. As shown in Figure 6(b), each AND gate IC can in charge of two devices or one bidirectional switching module. If both devices in a bidirectional switching module work, in accordance with the truth table of AND logic, the AND gate IC will send logic 1 as ENABLE signal toward gate driver of the dc-link switch and thereby connecting the converter to the high voltage power supply. Compared to [18], the proposed protection circuit realises lower number of components at a cost of increased power supply due to additional protection power supply ($-V_{SS,p}$). Thanks to the two-source-connected method, each bidirectional switching module consisting of two discrete devices as in this work only will require the same number of power supply as a single device.

FIGURE 7 I_{DS} vs. V_{DS} characteristics and selected forward operation points of (a) PSJ GaN FET; (b) SiC JFET [24]

To resolve the current commutation issue in such a one-phase half bridge converter, a current driven multi-step commutation strategy is used in this work [25]. The normal operation of this one-phase half bridge is shown in Figure 8(a), and zoom-in view of switching node voltage (V_{na}) versus DC-link current (I_{dc}) as indicated in Figure 2 during switching transitions as well as V_{gs} signals driven by multi-step commutation strategy are drawn in Figures 8(b) and 8(c) respectively.

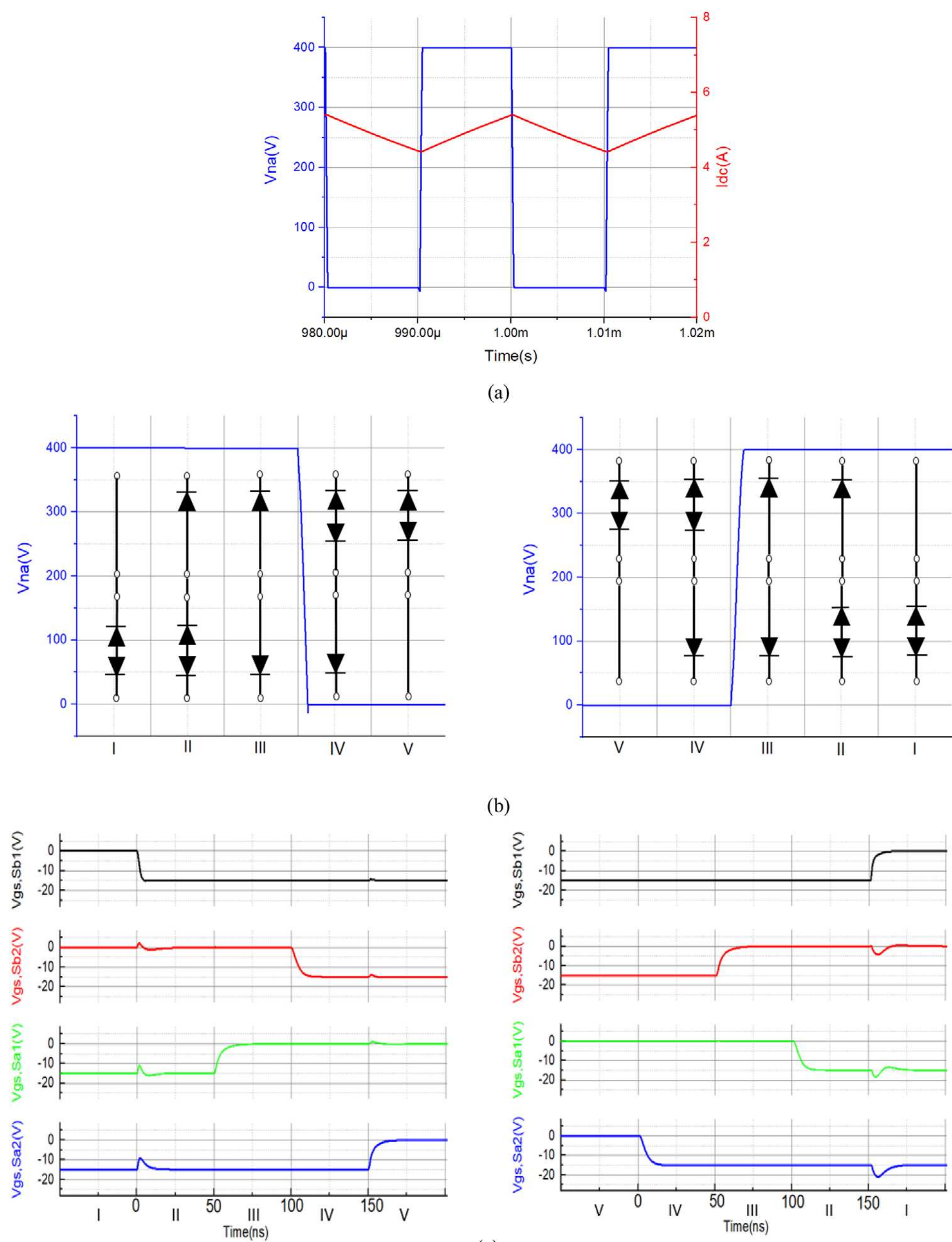

FIGURE 8 The normal operation of one-phase half-bridge using 2-S connected bidirectional switching module @400 V/10 A (a) V_{na} and I_{dc} versus time; (b) zoom-in view of switching transition; (c) V_{gs} pattern of commutation strategy

The key components and parameters used in proposed desaturation and negative power supply protection scheme are shown in Tables 1 and 2. The experimental set-up is shown in Figure 9.

When the negative power supply ($-V_{SS}$) fail, the gate voltage of the MOSFET (S_{gfp}) rises towards zero. This leads to the gate-to-source voltage of the MOSFET (S_{gfp}) become positive and therefore MOSFET (S_{gfp}) turns on. The Vgs of the DUT will be pulled down to negative value ($-Vss$), which is the voltage across the capacitor (C_{store}). In the meantime, as $-V_{SS}$ fail, the IN+ of comparator ($COMP_{gfp}$)become higher than IN- ($-V_{ref,gfp}$). Consequently, the opto-coupler receives a logic 1 signal from the comparator, and it sends an inverted output (logic 0) signal to AND gate IC. Eventually, the dc-link control switch will be turned off and isolate the converter from the high voltage power supply.

4 | SIMULATION AND EXPERIMENTAL VERIFICATION

The circuit as shown in Figure 2 is constructed in Cadence Orcad, which is a SPICE-based simulation tool and used to access the performance of the proposed protection scheme. The overall simulation can be divided into the following parts,

TABLE 1 Key components in proposed protection scheme

Component	Model
$\pm Vss/\pm Vss,p$ voltage regulator	ISA2415
$+Vcc/+Vopto$ voltage regulator	ITQ2405SA
$Dcb/Ddisc/Ddesat,gate$	ES1A
$Dsense$	BY203-20S
$Cstore$	EEEFT1V561AP
$COMP_{desat}/COMP_{gfp}$	LM311
Opto-coupler	ACPL-H61L
$S_{CMOS,p}/S_{CMOS,n}$	IRF5305/IRLR2905
$S_{comp,desat}/S_{desat}/S_{gfp}$	IPD220N06L3
DC-link switch	IXBF20N360
DC-link switch gate driver	IX3120
DUT/desat gate driver	Si8271

TABLE 2 Key parameters in proposed protection scheme

Parameter/unit	Value
$Rdesat/\Omega$	100
$Rsat/\Omega$	220
$Cdesat/$F	1500p
$Rp, Rn/\Omega$	1
$Rcom, desat/\Omega$	500
$Ropto, desat/\Omega$	100
$Cstore/$F	560u
$Rgfp, ref1/Rgfp, ref2/\Omega$	600/300
$Rcom, gfp/\Omega$	500
$Ropto, gfp/\Omega$	100
$+Vcc/+Vopto/$V	+5
$\pm Vss/\pm Vss, p/$V	±15

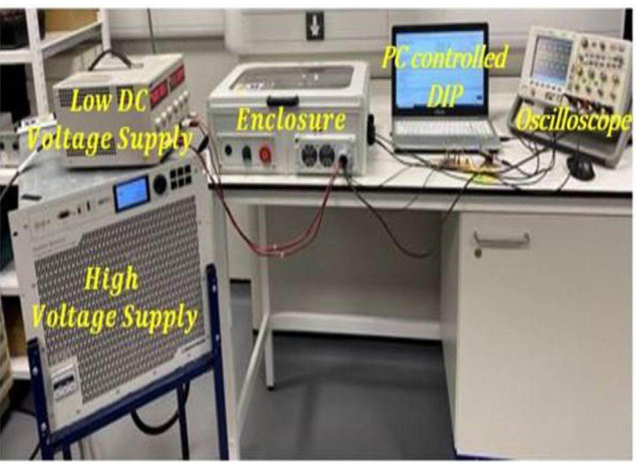

FIGURE 9 Set-up for experimental verification

TABLE 3 Critical values of desaturation circuit

Objective/unit	PSJ GaN FET	SiC JFET
$Rref1, desat/\Omega$	200	300
$Rref2, desat/\Omega$	1000	1000
$Id_limit/$A	13	60
$Vref/$V	4.167	3.846
$\Delta Vdesat/$V	2.48	2.02
Response time (t_r)/ns	321	290
Detect time (t_{detect})/ns	20	40.6

namely, desaturation circuit and negative power supply protection circuit implementation. The experimental verification set up as illustrated in Figure 6(b), which consists of a high-voltage DC source, an inductive load and two optional freewheeling SiC diodes (GB10MPS17-247). It is necessary to point out that the optional freewheeling diodes are implemented for higher current testing when SiC JFETs are used. The fault signal is triggered by C2000 Piccolo LaunchPad evaluation board with Ti F28027F as shown in Figure 6(a). Figure 7 depicts the IV characteristics and selected forward operation points of the PSJ GaN FET and SiC JFET used in this work, respectively. The gate-source voltage for both PSJ GaN FET and SiC JFET is varied from $-V_{SS}$ to 0 V, and [2 V, 13 A] and [1.4 V, 60 A] have been respectively selected as operation points based on their IV characteristics for PSJ GaN FET and SiC JFET.

4.1 | Evaluation of desaturation circuit

To evaluate the performance of the proposed desaturation circuit, a fault signal is generated by the lower switching module Sa in single-phase half bridge converter in Cadence, whereas the upper switching module Sb is operating at 50 kHz. With regards to experimental validation, this fault signal is triggered by the upper device as shown in Figure 6(a). The maximum current limit is set by two reference resistors ($R_{ref1,desat}$ and $R_{ref2,desat}$) as previously mentioned. In this work, the PSJ GaN FET based converter is operating at 600 V/5 A, and Id_limit is set at 13 A; the SiC JFET-based converter is operating at 400 V/25 A, and 60 A has been set as Id_limit, corresponding with 2 and 1.4 V drain-to-source voltage respectively according to their IV-curve as depicted in Figure 7 at room temperature. According to the Equation (1), the $Vref$ as "IN-" of the comparator is set to 4.167 V of PSJ GaN FET and 3.846 V of SiC JFET. Table 3 shows critical values in desaturation scheme, including overcurrent limit (Id_limit), reference voltage of the comparator ($Vref$), change in sensing voltage when faults occur ($\Delta Vdesat$). The CMOS configuration ensures that the comparison of the comparator between $Vdesat$ and $Vref$ only take place when DUT is ON-state. When DUT is under normal operation, $Vdesat$ is below $Vref$. The fault signal results in an increase of $Vdesat$, and therefore a logic LOW signal is yielded by desaturation circuit to turn-off the DUT. The triggering of fault signal leads to the

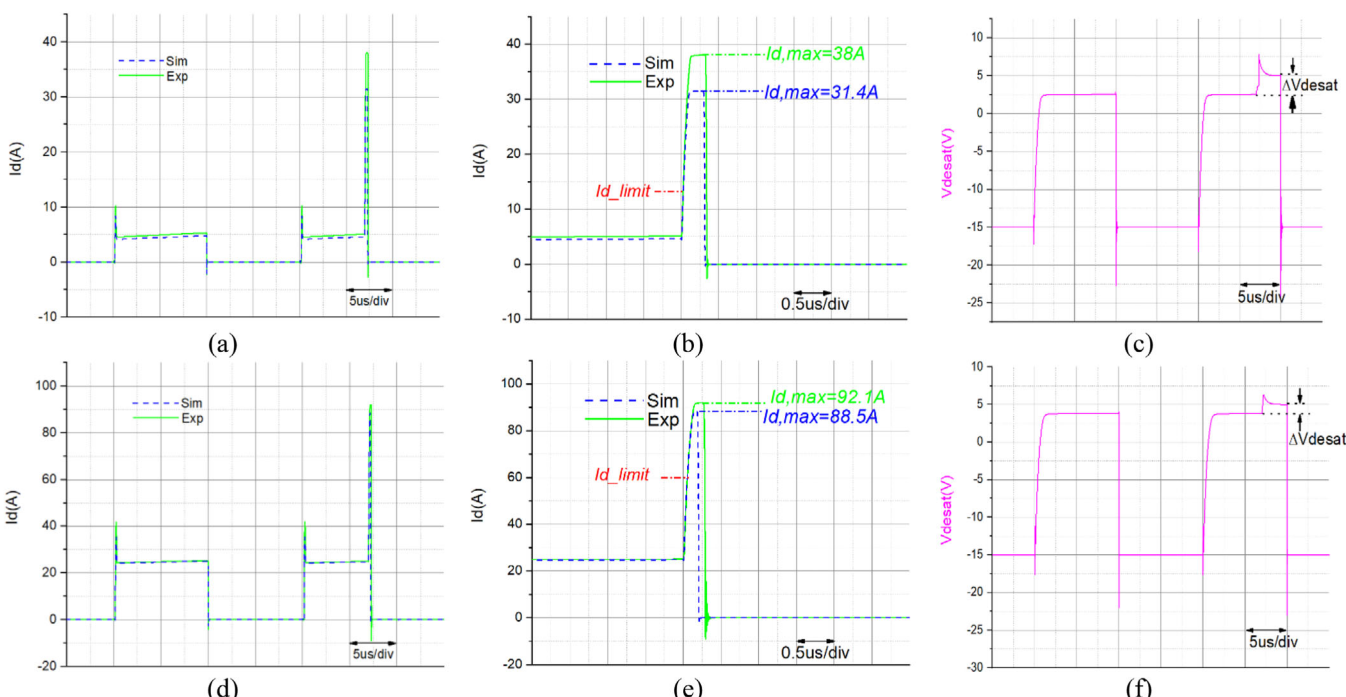

FIGURE 10 Comparison of simulation and experimental result of proposed desaturation scheme (a) PSJ GaN FET drain current; (b) zoom-in view of PSJ GaN FET drain current; (c) experimental PSJ GaN FET Vdesat; (d) SiC JFET drain current; (e) zoom-in view of SiC JFET drain current; (f) experimental SiC JFET Vdesat

desaturation circuit stops gating signal due to $-V_{SS}$ is forcefully applied to the gate-source terminal of the DUT.

The response time (t_r) of this desaturation circuit is the time from the instant of the drain current exceeds the specified limitation of the drain current (*Id_limit*) to where the fault event is cleared by the desaturation circuit. As shown in Figures 10(b) and 10(e), the overcurrent event lasts for 341 ns of PSJ GaN FET and 330.6 ns of SiC JFET. A maximum 38A drain current is observed within the desaturation period for PSJ GaN FET. With regards to SiC JFET, a maximum 92.1A drain current is reached within this period. Meanwhile, Figure 10(c) shows the proposed desaturation circuit only requires tens of nanoseconds (t_{detect}) upon the $Id, limit$ setting and devices' characteristics to detect the fault event, which saves more than 2.9 μs in comparison to the desaturation scheme proposed in [18]. Meanwhile, the response time of the proposed desaturation circuit is much lower than the 5us which is the common minimum requirement of short circuit capability for WBG device [18, 26]. As a result, the proposed desaturation circuit is able to detect and clear faults within 341 ns, which shows significant advancement in comparison with that in [18].

4.2 | Evaluation of negative power supply protection

To evaluate the performance of proposed negative supply protection circuit scheme in Figure 5, the negative power supply of the gate driver is eliminated by turning off the supporting gate driver power supply when PSJ GaNFET is operated at 50 kHz frequency. Figure 11 illustrates the response of negative power supply protection circuit. Reaction time and time frame are the two critical objectives for the proposed negative power supply protection. The reaction time is defined by how quick the DUT is switched-off by the negative power supply protection scheme. The time frame describes the allowed time for the converter to be isolated from its high-voltage source.

As shown in Figure 11(a), once negative voltage supply fail, the V_{gs_EN} of DUT will be pulled down accordingly towards $--Vss$ within 0.12 μs. It is because the reservoir capacitor (*Cstore*) is previously charged to $--Vss$ through the diode (*Ddisc*) during normal operation. An EN signal simultaneously generated by a negative power supply protection circuit which is sent to gate driver IC of the DC-link switch. This EN signal commands the dc-link switch to be turned off and isolates the converter from its main source. The proposed negative supply protection scheme keeps the converter in off-state for 60.5 ms as illustrated in Figure 11(b).

5 | CONCLUSION

A protection scheme for the bidirectional switching (BDS) module formed by two discrete normally-on GaN devices is proposed in this paper. The protection scheme consists of two parts, namely, the desaturation circuit and the negative gate voltage protection. Cadence Orcad is used to evaluate the proposed protection scheme under the simulation environment.

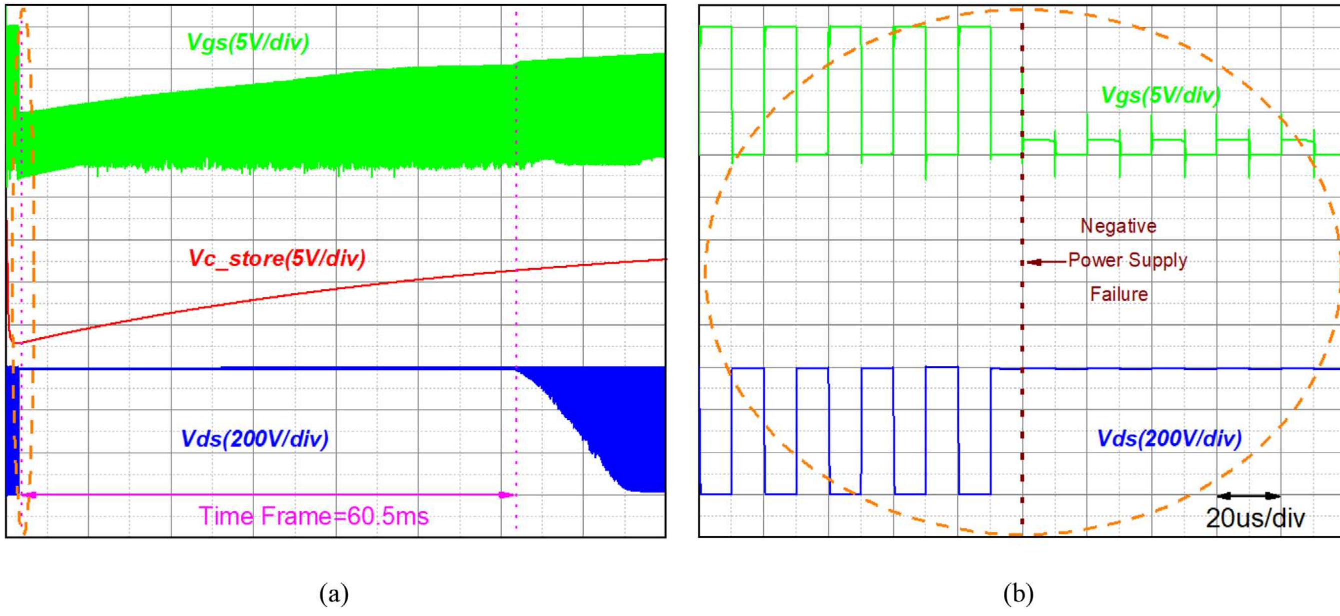

FIGURE 11 The proposed negative power supply protection experimental result (a) time frame; (b) zoom-in view of V_{gs} and V_{ds}

With respect to the performance of the proposed protection scheme, the overcurrent event can be removed in 341 ns for PSJ GaN FET at 600 V/5 A operation and 330.6 ns for SiC JFET at 400 V/25 A operation. The negative gate voltage protection circuit is able to offer 60.5 ms time frame, which can be easily adjusted by the capacitance of *Cstore* or the operation frequency. The time frame provided by the negative gate voltage protection circuit is aimed to offer a sufficient time for isolation of a single-phase half bridge converter from the high DC supply voltage.

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