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A Simple Approach to Improve the Switching Performance of Cascode GaNFETs

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Abstract –This paper analyses the switching performance of the cascode GaNFETs on Silicon substrates in three different PCBs using a double pulse test (DPT). A significant Vgs ringing is found during experiment. The source side parasitic inductance of cascade GaN with TO-247 package has been evaluated to cause significant gate voltage high frequency ringing. Moreover, reduction in Vgs high frequency ringing allows further reduction in input capacitance of the cascode structure. Which indicates a LV Si MOSFET with smaller input capacitance can be used in cascode GaNFETs. This enables faster switching transients and boosts the maximum switching frequency operation of cascode GaN devices, and thereby making use of the advantages that Gallium Nitride (GaN) brings. Method to reduce Vgs high frequency ringing is introduced in this paper. This enables stable switching transients and enhance the switching performance of cascode GaN devices, and thereby making use of the advantages that Gallium Nitride (GaN) brings. Simulation based on spice model is conducted for verification purpose.

Keywords – Cascode GaNFET, Gate Driver, Parasitics, Spice Model

I. INTRODUCTION

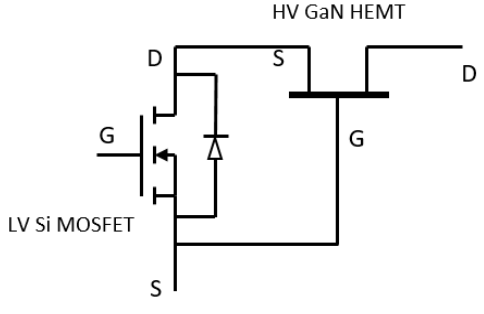
GaN has drawn international attention recently due to its superior intrinsic property in comparison with current dominant Si. This allows GaN-based device achieve smaller die size, higher power density, higher efficiency compared to that of Si for given voltage and current capability. Commercial GaN devices can be simply divided into two categories, which are pure eGaNFETs and cascode GaNFETs. Pure eGaNFETs are enhancement mode devices, which have two critical challenges in terms of low threshold voltage (about 1.5V) and narrow gate-to-source voltage operation margin (Max: 7V) [1]–[4]. This makes eGaNFET gate drive design more difficult and sophisticated, which also restricts the maximum turn-on dv/dt and di/dt [5]. Cascode GaNFET consists of one LV Si MOSFET and a HV GaN HEMT, with the detailed configuration as shown in Fig. 1(a). Unlike e-mode GaNFETs, cascode GaN devices can exhibit higher gate threshold voltages and wider Vgs operation margin compared to pure eGaNFETs [6]–[8]. A large Vgs ringing of cascode GaNFETs with TO-220/TO-247 package have been reported by Transphorm Inc. [9]. This Vgs high frequency ringing gives rise to higher driving losses and switching losses. Moreover, a larger input capacitance is required to prevent such significant Vgs high frequency ringing, which reduces the speed of switching. This leads to a reduction in switching frequency of the cascode GaN devices. One of the biggest drawbacks of cascode GaNFETs is slower switching transient in comparison with pure eGaNFETs. A detailed key parameter comparison of these two kinds of GaN devices as shown in Table 1 [10][11].

This paper aims to reduce the Vgs high frequency ringing in cascaded GaN structure, and thus improve the switching performance of overall cascode GaNFETs.

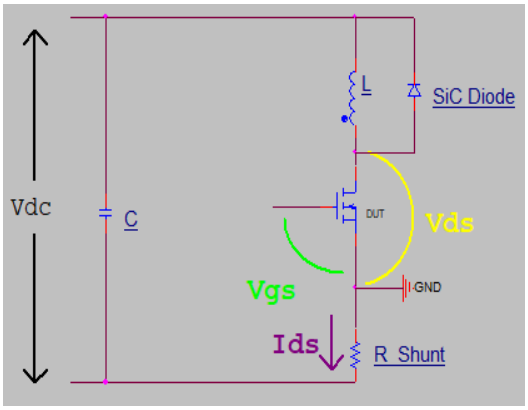
Table 1: Comparison between e-mode GaNFET and cascode GaNFET

Parameter	Cascode GaNFET (TPH3205WSB)	e-mode GaNFET (GS66508B)
Maximum transient protection/V	800	750
Gate driving voltage safety margin/V	10	1
Gate threshold voltage/V	2.4	1.7
Negative gate voltage required	No	Yes
Input capacitance (C_{ISS})/pF	2200	242

Three different PCBs with different gate loop design are used to find out the source of this Vgs high frequency ringing. The source ringing caused by parasitic inductance (from source of the device to gate driver ground) shows significant impact on the Vgs high frequency ringing. In an extreme case, this Vgs high frequency ringing can affect drain-source voltage, which results in additional unwanted switching loss. By reducing this parasitic inductance, a smaller Vgs ringing can be achieved due to reduction in source ringing, which can significantly reduce the driving loss of cascode GaNFETs. With reduced Vgs ringing, a LV Si MOSFET with smaller input capacitance can be used in cascode structure. This makes the input capacitance for overall cascode GaNFETs become smaller and therefore attain faster switching transients and higher switching frequency.



(a)



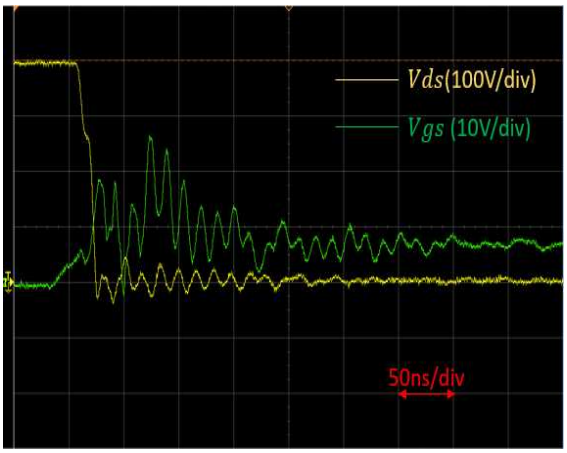
(b)

Figure 1: (a) Structure of cascode GaN device; (b) Double pulse test circuit

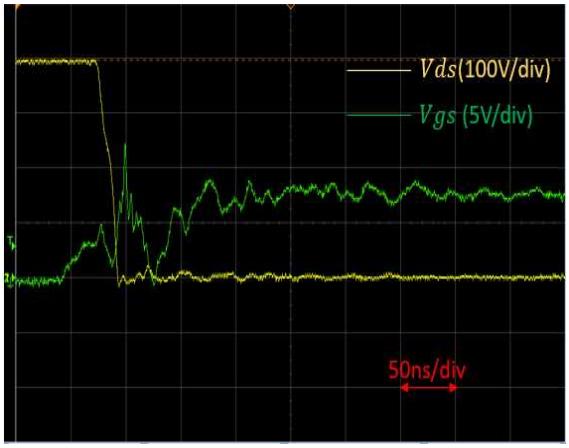
II. Experimental Evaluation of Cascode GaN Device

GaN Devices (TPH3205WSB) from Transphorm are used in this work. Double pulse test is used for the test as shown in Fig. 1 (c), which in addition to the DUT, has a free-wheeling diode (FFSH3065B-F085). Ascribed to the ground pin of gate driver is directly connected to source terminal of the device in order to minimize the common source inductance (CSI) in PCB. Hence, the majority of parasitic inductance in gate loop can be categorized into two parts, namely, gate turn-on inductance and source side parasitic inductance as depicted in Fig. 4.

With respect to gate driver, a relative faster integrated gate driver Si 8271 with high CMTI (200kV/us) is used in this work. In order to boost the turn-off speed, the gate path has been separated into turn-on and turn-off path with 10Ω ($Rgon$) and 2Ω ($Rgoff$) resistor respectively. For the comparison purpose, all three PCBs exhibit similar power loop design, and Ansys Q3D is used to extract the parasitic inductance within gate loop of three different PCBs in this work, and the value of these parasitic inductances as shown in Table 3.



(a)



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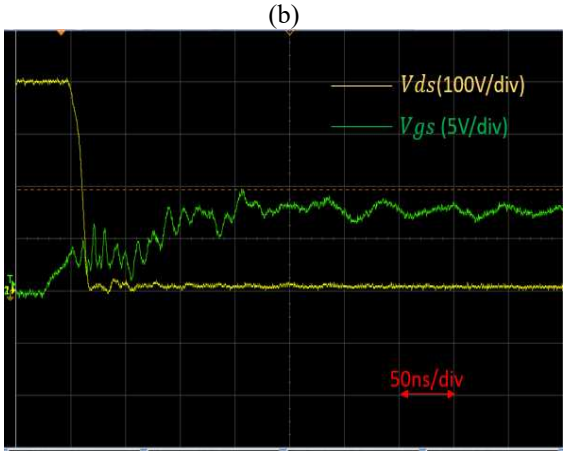
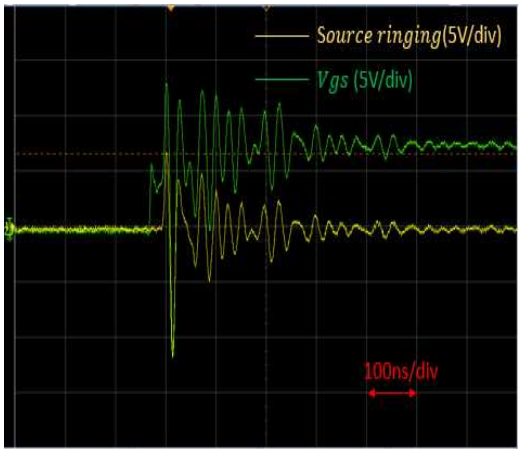
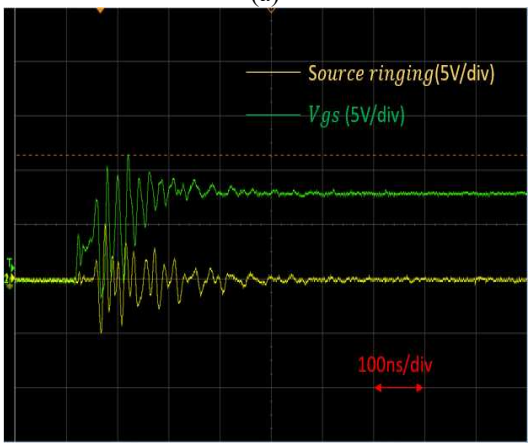


(c)

Figure 2: Turn-on event @ 400V/3A of (a) original board; (b) 1st amended board; (c) 2nd amended board



(a)



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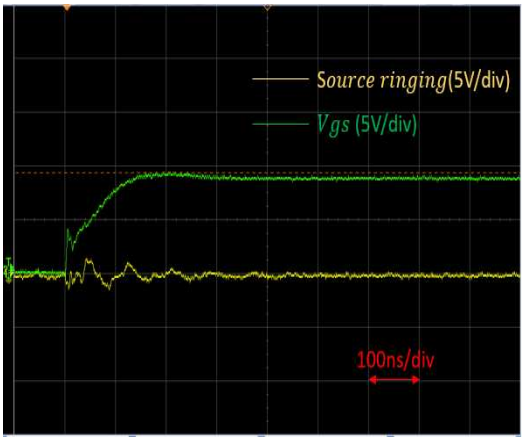

(c)

Figure 3: Source side ringing @ Vds=100V of (a) Original board; (b) 1st amended board; (c) 2nd amended board

Table 2: Three PCBs' key measurement results comparison

Parameter	Original board		1st amended (w/ external ferrite bead) board		2nd amended (w/ external ferrite bead) board	
	Turn-on	Turn-off	Turn-on	Turn-off	Turn-on	Turn-off
Vgs_{pk-pk}/V	28.4	10.3	13	10	10.3	10
Vgs_{Max}/V	26.3	7.8	12.2	8.1	9.6	8.1
Vds_{pk-pk}/V	438	403	413	406	409	400
Vds_{Max}/V	400	400	397	400	402	399
Source ringing @Vds=100 V /V	18.3		9.9		2.8	
Source ringing duration@ Vds=100V /ns	510		360		190	

Table 3: Three PCBs' parasitic inductance extraction

Objective	Original board	1st amended (w/ external ferrite bead) board	2nd amended (w/ external ferrite bead) board
Gate turn-on inductance /nH	5.6012	9.4462	4.4326
Source side parasitic inductance /nH	10.376	4.2235	1.092

The Vgs high frequency ringing is mainly caused by the source side ringing of cascode GaN device, since the shape of the Vgs ringing is like the source side ringring in terms of waveform shape and voltage oscillation frequency as depicted in Fig. 3. The source side ringing is therefore formed by source side parasitic inductance as shown in Fig. 4. The source side ringing measured is as illustrated in Fig. 4, the measurement probes are directly connected to the GND pin of gate driver and source terminal of the cascode GaN device.

Fig. 2(a) shows the original board has significant Vgs and Vds oscillation, which lead to additional driving loss and switching loss during transition. In order to find out the source that causes such voltage oscillations, another two boards with optional ferrite bead (40Ω@100MHz) were made for comparison purpose. The 1st amended board has 3.84nH higher gate turn-on inductance and 6.1525nH smaller source side parasitic inductance in comparison with original board, while the peak-to-peak value of source ringing and Vgs ringing during turn-on have reduced by 14.2V and 15.4V respectively. Even without the optional ferrite bead, the 1st amended board shows a significant reduction in Vgs_{pk-pk} from 28.4V to 14.2V during turn-on period. In the meantime, there is no significant Vds oscillation can be observed after amendment. This demonstrates the importance of this parasitic inductance. Reduction in source side parasitic inductance can effectively reduce the source side ringing, and therefore smaller and shorter gate-source voltage oscillation can be achieved. With further optimization in 2nd amended board, both Vgs oscillation and source ringing duration become even smaller and shorter. The Vgs_{pk-pk} reduced from 13V to 10.3V, and the source-side ringing become even smaller, reduced from $9.9V_{pk-pk}$ to $2.8V_{pk-pk}$. By comparing 1st and 2nd amended PCBs, the source side parasitic inductance shows more significant influence on both Vgs and Vds waveform in comparison to gate turn-on inductance as depicted in Fig. 2 and Fig. 3. Meanwhile, a smaller source side parasitic inductance give rise to shorter gate-source voltage oscillation time, which can further reduce the gate driving loss. As a result, a careful management with respect to source side parasitic inductance should be made when cascode GaN devices is used.

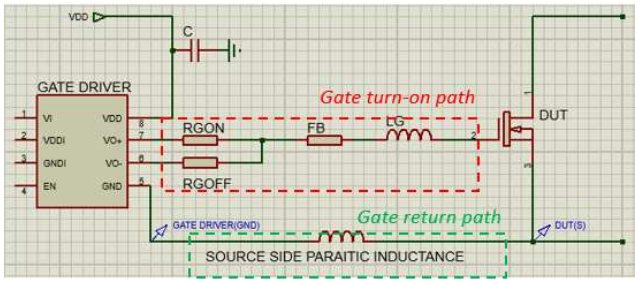

Figure 4: Source side ringing measurement

III. Simulation Verification

Cadence Orcad is used for simulation verification, and the simulation circuit is identical with PCB. The original spice model of the cascode GaNFET is provided by Transphorm Inc [12]. The spice model has been modified by author in accordance with practical measurement of the DUT for the sake of accuracy. The simulation and experimental turn-on and turn-off waveforms of TPH3205WSB are illustrated in Fig. 5. Two additional spice models with different input capacitance were made for verification purpose. Cgs/Cgd ratio of these two modified spice models remain the same.

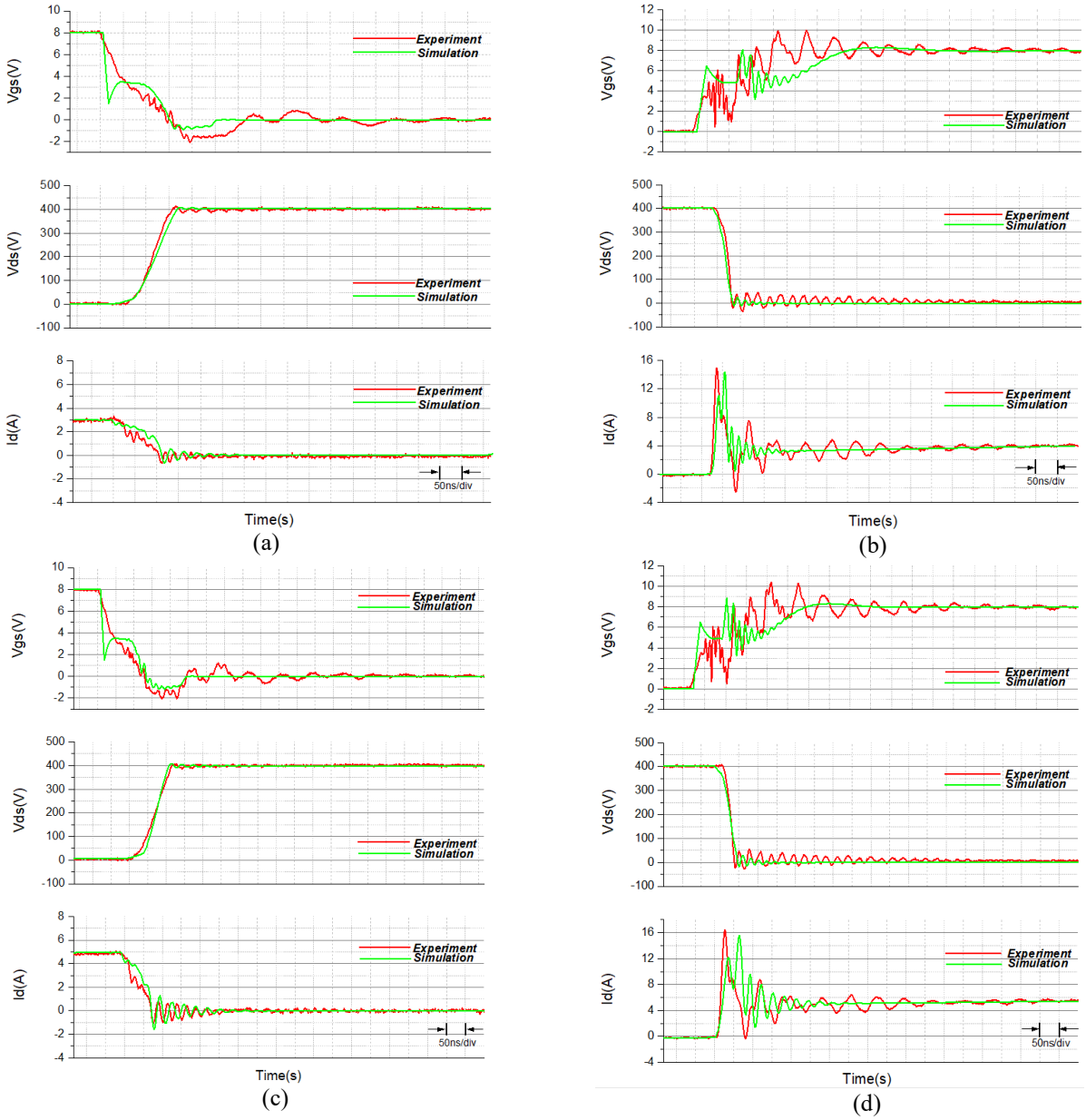

Figure 5: Waveforms of TPH3205WSB (a) 400V/3A turn-off; (b) 400V/3A turn-on; (c) 400V/5A turn-off; (d) 400V/5A turn-on

Table 4: Simulation verification @ 400V/3A

Parameter	Original Spice Model	Spice Model I	Spice Model II
C_{gs_MOSFET}/pF	2141.48	1641.48	1141.48
Ton/ns	35.34	34.2	30.899
Toff/ns	101	94.9	86.88
Switching losses/uJ	38.2	37.63	37.17

Table 4 shows simulation result of three models. According to simulation result, the reduction in gate-source capacitance of cascode GaNFET, both Ton and Toff become smaller. Typically, with 500 pF reduction of Cgs, the Ton and Toff of the cascode GaNFET can be reduced by 1.14ns and 6.1ns respectively. With 1000 pF reduction of Cgs, the Ton and Toff can respectively become 4.441ns and 14.12ns smaller. As a result, when the gate return path of cascode GaNFET is carefully designed, the LV Si MOSFET no longer require that high input capacitance to prevent source side ringing. Thus, a MOSFET with smaller gate-source capacitance can be used in cascode structure, and therefore both turn-on and turn-off transients can be shorter. This allows cascode GaNFETs operate at even higher frequency and result in higher power density higher efficiency operation for power conversion design.

IV. Conclusion

This paper evaluates the impact of source side parasitic inductance of cascode GaNFETs with TO-247 package via double pulse test (DPT). A smaller Vgs high frequency ringing can be achieved by optimizing the source side parasitic inductance, as a large source ringing is caused by this parasitic inductance. Thanks to the smaller Vgs ringing amplitude and shorter Vgs oscillation duration, the cascode GaNFETs no longer require that high input capacitance. It is therefore possible to achieve faster switching transients for cascode GaNFETs by replacing a MOSFET with smaller input capacitance. Ascribed to Si technology is relatively

mature today, there are lots of LV Si MOSFETs with lower input capacitance available in the market [13]. In order to verify the assumption proposed by author, a series of simulations based on spice model are conducted. According to the simulation result, the switching speed can be improved without the cost of gate driving loss and switching loss. Typically, when a 500pF gate-source capacitance reduction achieved, the turn-on time (Ton) and turn-off time (Toff) can be 1.14ns and 6.1ns smaller; when the gate-source capacitance reduced by 1000pF, the turn-on and turn-off time can be accordingly reduced by 4.441ns and 14.12ns. As a result, the source side inductance become one of the most critical consideration when using cascode GaNFET.

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