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Dual metal gate AlGaN/GaN high electron mobility transistors with improved transconductance and reduced short channel effects

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Abstract

AlGaN/GaN high electron mobility transistors with a range of dual metal gate (DMG) lengths have been fabricated and studied. An improvement in transconductance up to 9% has been measured in the DMG devices in comparison to the conventional single metal gate devices. This is attributed to the distribution of the electric field under the gate region as a result of two gate metals. The drain induced barrier lowering is also suppressed using the sub-μm DMG devices, with a drain induced barrier lowering decrease of around 50% due to a potential shielding effect in the two-dimensional electron gas channel.

Keywords: GaN, HEMTs, transconductance, drain induced barrier lowering

(Some figures may appear in colour only in the online journal)

1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) have been an area of increasing research particularly in high frequency and high power applications. Communications technology seem to be the most common place for these devices, due to their excellent performance in the GHz range [1–5]. To achieve high frequency operation, high transconductance is the key. However, reducing the gate length to achieve higher transconductance results in short channel effects such as drain induced barrier lowering (DIBL) where the threshold voltage (V_{TH}) changes with drain bias [6]. This limits the output power, gain and efficiency of the short gate length AlGaN/GaN HEMTs for RF applications [7]. In addition, the peak of electric field occurs at the drain-side of the gate in the lateral HEMTs results in a non-uniform electron velocity profile under the gate and low electron velocity in the channel near the source-side [8]. Modification of the electric field distribution under the gate region can improve the electron velocity profile and hence the device transconductance. One approach to improve the device transconductance and suppress DIBL of the lateral HEMTs is to employ a dual metal gate (DMG) structure with different metal work functions (WF) [9–11]. Simulations of GaN-based HEMT devices using this structure have been performed previously [12, 13] showing notable improvements in the electron velocity under the gate leading to a higher output current and transconductance as well as suppression in the DIBL in these devices [14]. Recently, an improvement in the transconductance of the GaN-based

transistors with DMG have been demonstrated experimentally [15, 16]. However, the gate lengths in those devices are larger than 1 μm and the effect of the DMG on DIBL has not been studied which is critical for high frequency RF applications [17, 18].

In this paper, we demonstrate sub-μm DMG structures on AlGaN/GaN HEMTs with two different gate metals: titanium (Ti) and palladium (Pd), and study the electrical characteristics in comparison with conventional single metal gate (SMG) devices. We also investigate the effect the gate length and the gate metal configurations can have on DMG device performance. A device simulation study was undertaken to understand the properties of the DMG HEMTs.

2. Experimental

The HEMTs epilayer structure was grown by metal-organic vapour phase epitaxy on a 6 inch diameter silicon substrate as shown in figure 1(a). A 250 nm AlN layer was first grown on the substrate as a nucleation layer. Subsequently, a 2 μm thick compositionally graded AlGaN layer which serves as a strain-relief layer to manage the strain as a result of the large lattice mismatch and large thermal expansion coefficient difference between GaN and silicon, followed by a 1 μm thick carbon-doped GaN buffer to achieve high breakdown voltage were grown A 250 nm unintentionally doped GaN channel layer was then grown and followed by a nominally 1 nm AlN spacer layer which serves as a channel mobility enhancement layer. Finally, a 25 nm unintentionally doped $Al_{0.25}Ga_{0.75}N$ barrier layer was grown and capped with a nominally 2 nm unintentionally doped GaN cap layer to give a high quality surface morphology and reduce gate leakage current. [19]

The devices were then fabricated using the following process: Initially, mesa isolation was performed using Cl_2-based inductively coupled plasma etching. Ti/Al/Ni/Au metal stacks were deposited and annealed at 850 °C to form the source and drain ohmic contacts. Following this, the first gate was defined using electron beam lithography (EBL). A metal stack of Ti/Au (20 nm/200 nm), was then deposited using thermal evaporation. The second gate regions were defined with further EBL step and Pd/Au (20 nm/200 nm) was deposited using evaporation. A Ni/Au (20 nm/200 nm) metal stack was deposited to form probe pads for gate, drain and source contacts. 80 nm of SiN_x was deposited using plasma enhanced chemical vapour deposition to act as passivation for the devices. Via etching on the probe pads was then performed using reactive ion etcher to allow electrical probing to the devices. All devices are fabricated with a source–drain separation of 5 μm, gate width of 125 μm and gate length ranging from 400 nm (200 nm/200 nm for DMG) to 200 nm (100 nm/100 nm for DMG). Figure 1(b) shows the SEM image of a DMG with a PdAu/TiAu configuration. For comparison, devices with TiAu/PdAu DMG, PdAu and TiAu SMG were also fabricated. Figure 1(c) shows the conduction band diagram of SMG HEMT with gate metal WF of 4.4 eV and 5.2 eV.

3. Results and discussions

3.1. Experimental results

Figure 2(a) shows the gate transfer of the AlGaN/GaN HEMTs with four different gate configurations, TiAu/PdAu (DMG), PdAu/TiAu (DMG), TiAu (SMG) and PdAu (SMG) with a total gate length of 400 nm. V_{TH} of the devices was acquired from the gate transfer characteristics using linear extrapolation from the peak transconductance method [20, 21]. A V_{TH} difference of 0.5 V between the TiAu and PdAu SMG devices was measured, while the PdAu SMG and PdAu/TiAu DMG devices exhibit a similar V_{TH}. On the other hand, V_{TH} of the TiAu/PdAu DMG devices is 0.35 V higher than that of the PdAu SMG devices. The peak transconductance shows an increase, from 200 mS mm^{-1} in the PdAu SMG devices, to 212 mS mm^{-1} in the PdAu/TiAu DMG devices, averaged from measurements on five devices for each gate metal configuration and covering three separate fabrication batches. The output characteristics of the PdAu SMG and PdAu/TiAu DMG devices are shown in figure 2(b).

In addition to the transconductance increase, the DMG structure suppresses the DIBL effect in the AlGaN/GaN HEMTs. DIBL is defined as $(V_{TH(LIN)} - V_{TH(SAT)})/(V_{DS(SAT)} - V_{DS(LIN)})$, where $V_{TH(LIN)}$ and $V_{TH(SAT)}$ are V_{TH} for the drain bias $= V_{DS(LIN)}$ and $V_{DS(SAT)}$, respectively [22]. $V_{DS(LIN)}$ and $V_{DS(SAT)}$ are set as 0.1 V and 10 V, respectively. This DIBL manifests as a negative shift in V_{TH} at higher drain biases as the channel region requires a higher gate voltage to pinch off. The PdAu SMG devices exhibit a DIBL of 37 mV V^{-1} with a drain bias voltage between 0.1 V and 10 V. In comparison, V_{TH} of the PdAu/TiAu DMG devices was less sensitive to the drain bias changes with a DIBL of 19 mV V^{-1} when subjected to the same drain bias range as shown in figure 3. It is noted that the off-state leakage current is dominated by the gate leakage in the DMG devices while the higher off-state leakage current observed in the SMG devices can be attributed to the DIBL effect which leads to poor channel pinch-off.

Figure 4 shows the gate transfer characteristics of the 100 nm/100 nm PdAu/TiAu DMG and 200 nm PdAu SMG HEMTs. The DMG structure is also effective in improving peak transconductance and reducing DIBL effect as the total gate length reduces to 200 nm. Table 1 summarises the peak transconductance and DIBL with varying gate length in PdAu SMG and PdAu/TiAu DMG devices. While the peak transconductance increases with decreasing gate length in both SMG and DMG devices, the DMG devices exhibit a higher peak transconductance of 229 mS mm^{-1} with 100 nm/100 nm gate length compared to 216 mS mm^{-1} with 200 nm SMG devices. On the other hand, DIBL reduces from 55 mV V^{-1} in the SMG devices with a 200 nm gate length to 27 mV V^{-1} in the 100 nm/100 nm DMG devices.

3.2. Device simulations and discussion

The SMG and DMG AlGaN/GaN HEMT structures were simulated using Sentaurus TCAD software to understand their

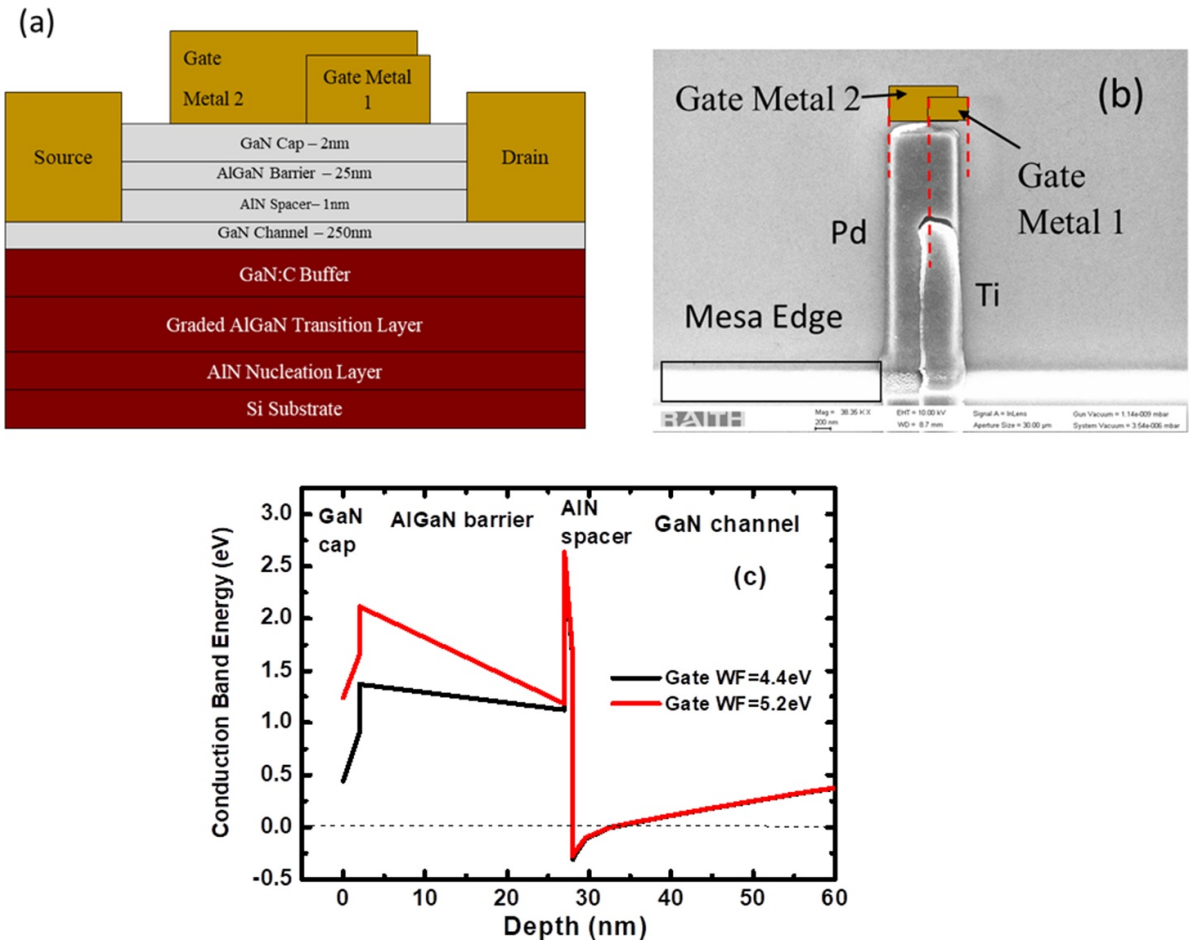

Figure 1. (a) A profile view of the epilayer structure in this study. (b) An SEM image taken showing the device with DMG, gate metal 1 being deposited first then metal 2 on top. (c) Conduction band diagram of the HEMT structure in this study with varying gate metal work function.

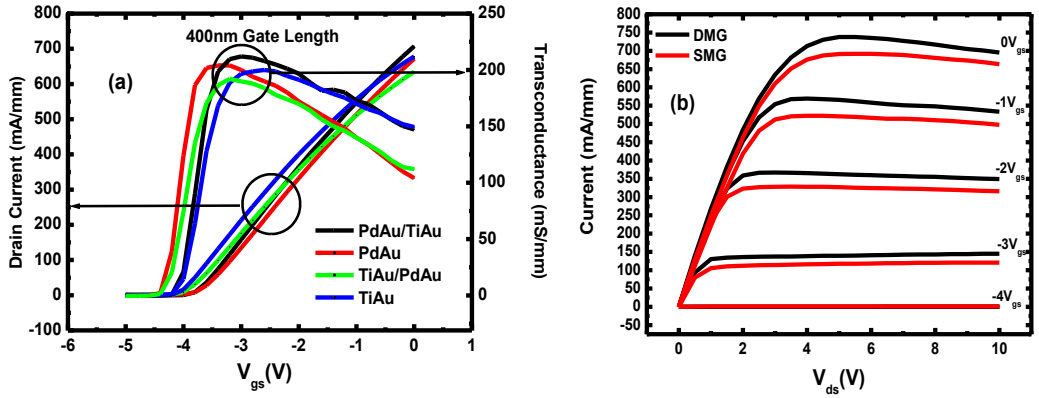

Figure 2. (a) The gate transfer characteristics of the 400 nm TiAu SMG, 400 nm PdAu SMG, 200 nm/200 nm PdAu/TiAu DMG and 200 nm/200 nm TiAu/PdAu DMG HEMTs. (b) The output characteristics of 200 nm/200 nm PdAu/TiAu DMG and 400 nm PdAu SMG HEMTs.

electrical properties. The epi-structure and device structure used in the simulations are the same as the experimental structures described above. The WF of the Pd and Ti in the simulations is set as 5.2 eV and 4.4 eV, respectively [23, 24]. A 0.6 V difference in V_{TH} between the TiAu and PdAu SMG devices is observed from the TCAD simulation which is consistent with experimental results. V_{TH} of AlGaN/GaN HEMTs can be expressed as [25, 26]

$$V_{TH} = \frac{\emptyset_B - \Delta E_C}{q} - q\frac{d_B}{\varepsilon_B}\sigma_{pol} + \frac{E_B}{q}, \qquad (1)$$

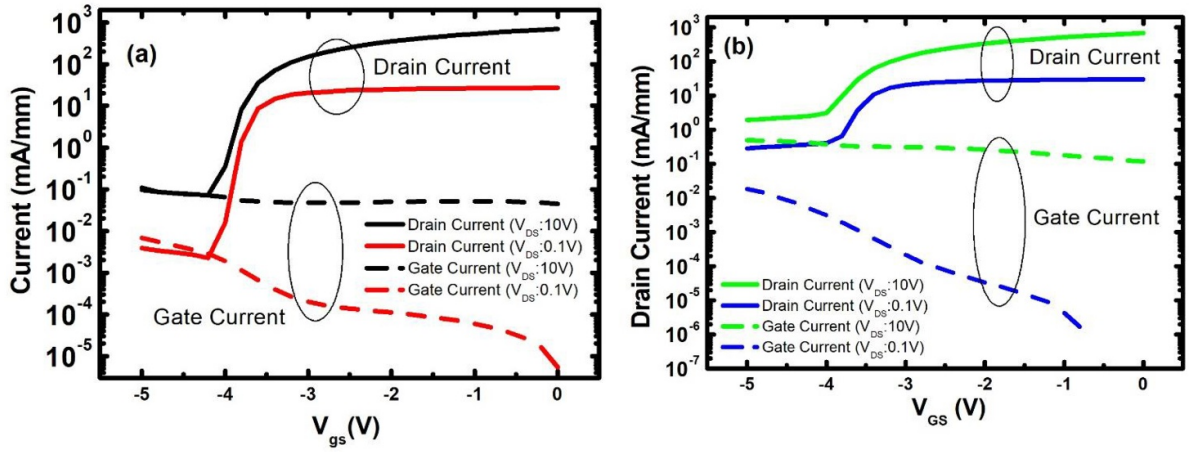

Figure 3. Comparison of gate transfer characteristics of (a) 200 nm/200 nm PdAu/TiAu DMG and (b) 400 nm PdAu SMG HEMTs with drain bias of 0.1 V and 10 V.

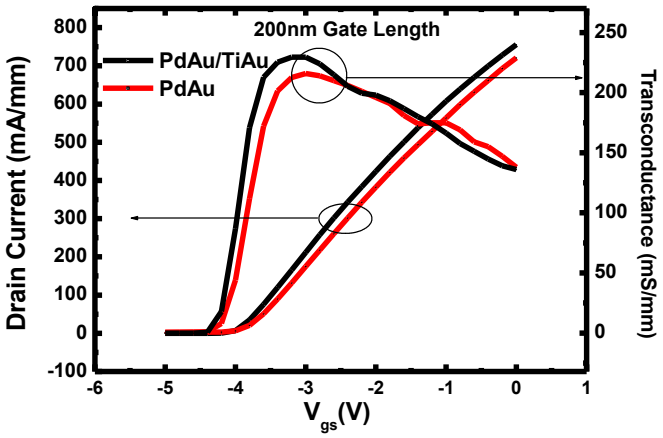

Figure 4. Comparison of the gate transfer characteristics of 100 nm/100 nm PdAu/TiAu DMG and 200 nm PdAu SMG HEMTs.

Table 1. Peak transconductance and DIBL of the PdAu/TiAu DMG and PdAu SMG AlGaN/GaN HEMTs with varying gate length.

Gate configuration	Peak transconductance (mS mm^{-1})	DIBL (mV V^{-1})
200 nm/200 nm DMG	212	19
400 nm SMG	200	37
100 nm/100 nm DMG	229	27
200 nm SMG	216	55

where σ_{pol} represents the polarisation charge density at hetero-interface, q is the charge on an electron, ϕ_{B} is the metal-semiconductor Schottky barrier height, ΔE_{C} is the conduction band discontinuity, ε_{B} and d_{B} are the permittivity and thickness of the barrier layer, respectively, E_{F} is the difference between the intrinsic Fermi level and the conduction band edge of the GaN channel.

From equation (1), since all devices in this study are fabricated on the same epi-wafers, the difference in V_{TH} observed between TiAu and PdAu SMG devices is due to the difference in the gate metal WF and hence the metal-semiconductor Schottky barrier height [27, 28]. The forward bias of I–V characteristics can be described by:

$$I = I_O\left(\exp\left(\frac{qV - IR_{\mathrm{s}}}{nkT}\right) - 1\right), \tag{2}$$

$$I_O = AA^{**}T^2\exp\left(\frac{-q\Phi_{\mathrm{B}}}{kT}\right), \tag{3}$$

where I_0 is the saturation current, q is the electron charge, n is the ideality factor, R_{s} is the series resistance, k is Boltzmann constant, T is the temperature, A is the Schottky diode area, A^{**} is the effective Richardson constant of 35 A cm^{-2} K^{-2} [28] and Φ_{B} is the Schottky barrier height.

Figure 5 shows the I–V characteristics of the Ti and Pd Schottky diodes with 150 μm diameter. The Schottky barrier height extracted from the Schottky diodes using equations (2) and (3) is found to be 0.57 eV for Ti and 1.18 eV for Pd, which gives a difference of 0.61 eV, consistent with the difference in V_{TH} measured from TiAu and PdAu SMG HEMTs.

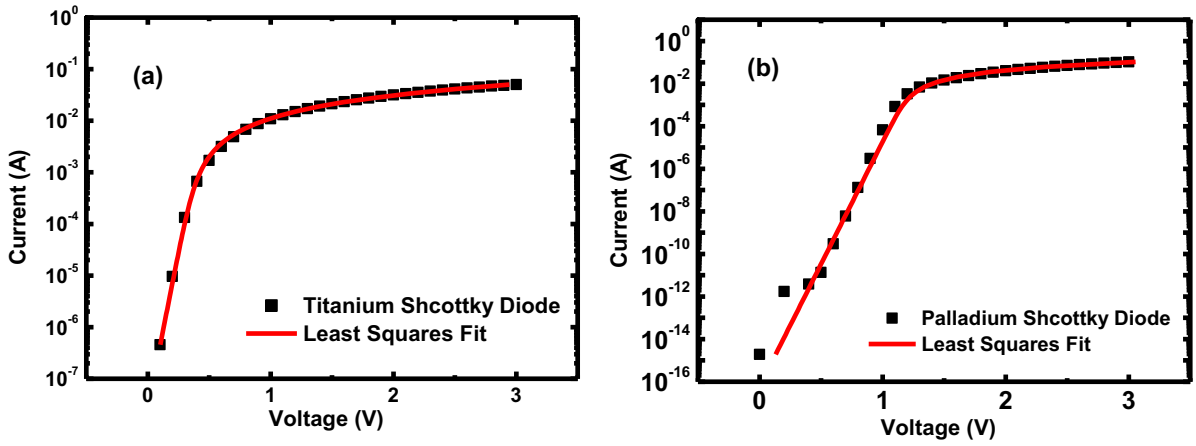

Figure 5. Experimental I–V characteristics of Schottky diode with (a) Ti and (b) Pd Schottky contact. The red lines are the least square fit to the I–V characteristics using equation (2).

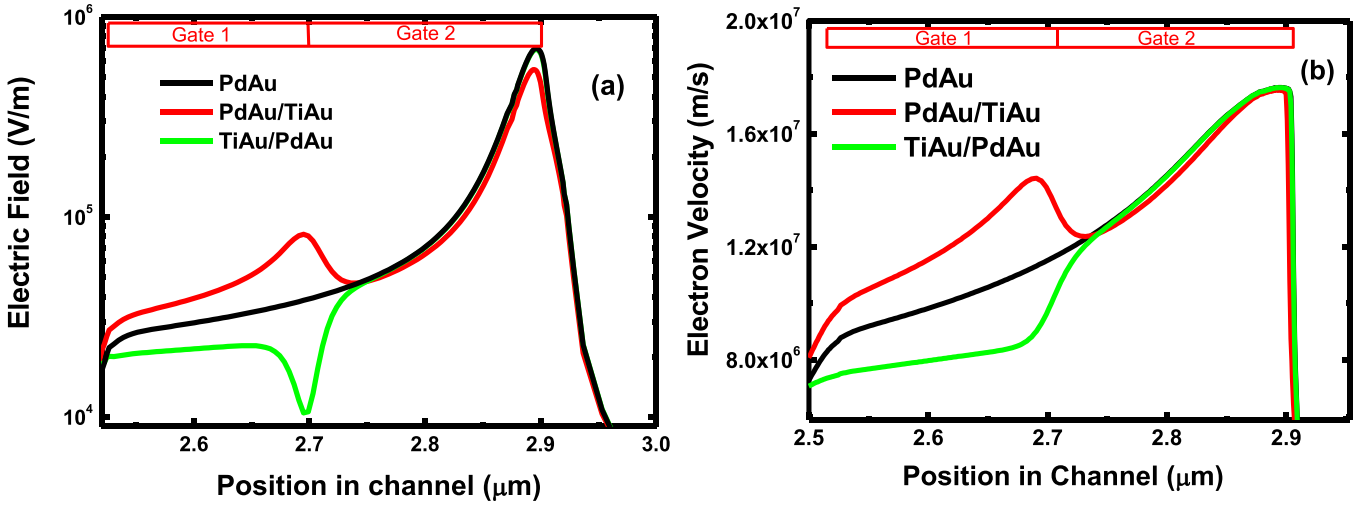

Figure 6. Simulated (a) electric field and (b) electron velocity under the gate region along the channel for different gate configurations with total gate length of 400 nm at $V_{DS} = 10$ V and $V_{GS} = 0$ V.

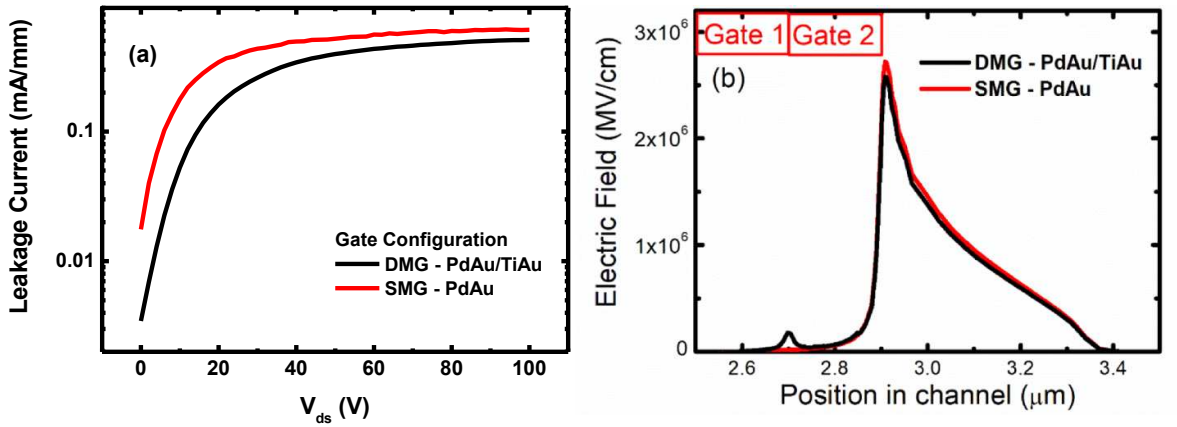

Figure 7. (a) Off-state gate leakage current of 400 nm SMG and 200 nm/200 nm DMG HEMTs. (b) Simulated off-state electric field profile along the 2DEG under the gate region of PdAu SMG and PdAu/TiAu DMG HEMTs at V_{DS}: 100 V.

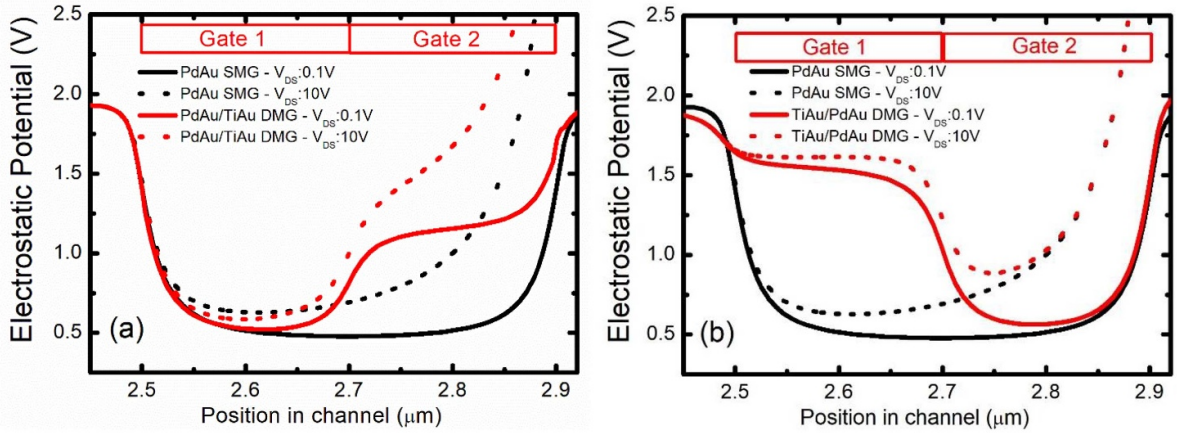

Figure 8. The comparison of the simulated electrostatic potential along the channel under the 400 nm gate region (a) between PdAu SMG and PdAu/TiAu DMG and (b) between PdAu SMG and TiAu/PdAu DMG at $V_{GS} = -3.5$ V with varying drain bias.

This indicates that the V_{TH} of the SMG devices is governed by the Schottky barrier height between the gate metal and the semiconductor. Due to a higher Schottky barrier height, depletion of the 2DEG channel under the Pd gate metal occurs at lower gate voltage compared to that of the Ti gate metal in the devices.

Two peaks in the electric field are observed along the 2DEG channel for the PdAu/TiAu DMG devices, in contrast to the single peak at the drain-side gate edge in the electric field for the SMG devices as shown in figure 6(a). The DMG devices with a higher gate metal WF (Pd) on the source side and the lower WF on the drain side (Ti) moderates the electric field at the drain-side gate edge and induces an additional peak in the electric field between the two gate metals. This acts in a similar manner as field plates spreading out the peak field seen along the device channel [29–31]. The presence of the additional electric field peak under the gate effectively increases the average velocity under the gate region as shown in figure 6(b). Hence, an improved transconductance is observed in the DMG device with PdAu/TiAu. On the other hand, placing a lower WF (Ti) on the source-side of the TiAu/PdAu DMG induces an opposite effect and reduces the electric field between the gate metals. This results in a reduced average electron velocity in the channel and a peak transconductance of 192 mS mm^{-1} is measured as shown in figure 2(a), lower than that of both PdAu/TiAu DMG and SMG devices.

Despite the presence of lower WF and hence lower Schottky barrier height gate metal (Ti) on the drain side for the PdAu/TiAu DMG, a similar level of off-state gate leakage current was measured for both PdAu SMG and PdAu/TiAu DMG HEMTs at drain bias of 100 V as shown in figure 7(a). This is attributable to the electric field moderation effect induced by PdAu/TiAu DMG as observed in figure 7(b). The lower electric field in the drain-side gate edge of DMG compensates the effect of lower Schottky barrier height on the gate leakage current.

Figure 8(a) shows the simulated electrostatic potential profile of the PdAu SMG and PdAu/TiAu DMG devices. A two-step profile in the electrostatic potential along the channel is observed with the Pd gate metal with a higher WF on the source side is shielded from the varying drain bias by the lower WF metal, Ti, on the drain-side for the PdAu/TiAu DMG device. This acts to spread out the depletion region in the channel and the screening effect reduces the sensitivity of DIBL with the drain bias variation when compared to the PdAu SMG device. As the DIBL effect increases with the reduction of gate length for higher frequency operations, unique screening effect in the DMG devices is advantageous in suppressing the DIBL in the sub-μm gate length devices. It is noted that the shielding effect is not observed in the TiAu/PdAu DMG and the channel is effectively controlled by the Pd part of the gate metal which is only 200 nm in length as observed in figure 8(b). This is consistent with a DIBL of 47 mV V^{-1} measured experimentally on the 200 nm/200 nm TiAu/PdAu DMG devices, which is higher than that of all other configurations. This effect in the TiAu/PdAu DMG devices also explains why V_{TH} measured at V_{DS}:10 V from figure 2(a) is higher (more negative) than that of the PdAu SMG device.

4. Conclusion

An increase in the transconductance has been demonstrated in the DMG structure AlGaN/GaN transistors compared to that of the conventional SMG structure with gate length of 400 nm and 200 nm. The transconductance improvement with the higher WF gate metal placed on the source-side and lower WF on the drain-side results from an additional peak in the electric field under the gate which improves the average electron velocity in the channel. In addition, the dual gate metal structure is effective in reducing the DIBL effect with a sub-μm gate length. This is attributable to the screening effect induced by the lower WF metal at the drain side of the gate screening the higher WF gate from the varying drain bias.

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