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Epitaxial GeSn/Ge Vertical Nanowires for p-Type Field-Effect Transistors with Enhanced Performance

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Abstract: Harvesting the full potential of single crystal semiconductor nanowires (NWs) for advanced nanoscale field-effect transistors (FETs) requires a smart combination of charge control architecture and functional semiconductors. In this article, high performance vertical gate-all-

around nanowire p-type pFETs are presented. The device concept is based on advanced $Ge_{0.92}Sn_{0.08}$/Ge group IV epitaxial heterostructures, employing quasi-one-dimensional semiconductor nanowires fabricated with a top-down approach. The advantage of using a heterostructure is the possibility of electronic band engineering with band offsets tunable by changing the semiconductor stoichiometry and elastic strain. The use of a $Ge_{0.92}Sn_{0.08}$ layer as the source in GeSn/Ge NW pFETs results in a small subthreshold slope of 72 mV/dec and a high I_{ON}/I_{OFF} ratio of 3×10^6. A ~32% drive current enhancement is obtained compared to vertical Ge homojunction NW control devices. More interestingly, the drain-induced-barrier lowering is much smaller with GeSn instead of Ge as the source. The general improvement of the transistor's key figures of merits originates from the valence band offset at the $Ge_{0.92}Sn_{0.08}$/Ge heterojunction, as well as from a smaller NiGeSn/GeSn contact resistivity.

Keywords: nanowire, gate-all around, field-effect transistors, GeSn alloys, heterostructure, Group IV nanoelectronics

INTRODUCTION

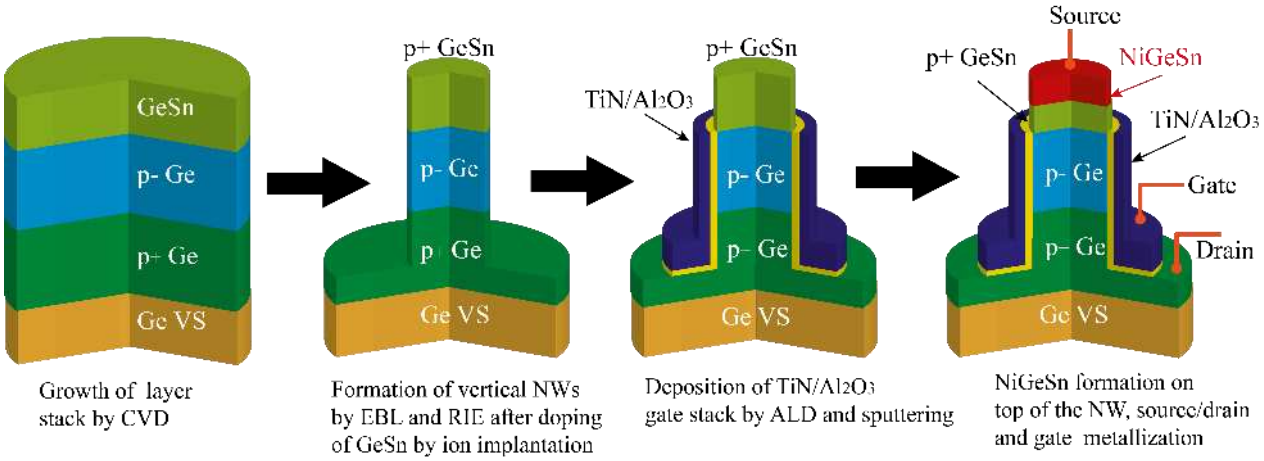
New materials, novel device concepts and architectures have been continuously evaluated to improve the metal oxide semiconductor field-effect transistor (MOSFET) performance.[1-4] Besides the social and economic impact of low power electronics in the field of Internet of Things (IoT) and Artificial Intelligence of Things (AIoT) applications, and in spite of remarkable technological progress, the scaling of silicon complementary metal-oxide-semiconductor (CMOS) still faces multiple challenges. The most critically important limitation in MOSFET size scaling is caused by the gate controllability of electrical charges. Multiple-gate MOSFETs, like FinFETs, provide improved gate control, and have been used for technology nodes beyond 22nm.[5] Gate-all-

around (GAA) NW transistors are strong candidates for ultra-scaled sub-5 nm technology nodes offering excellent gate control and immunity against short-channel effects.[2,6] Regarding the ultimate CMOS architecture, vertical GAA NW transistors provide further scalability, enhanced layout efficiency, and smaller power consumption compared to FinFETs and even to horizontal GAA NW devices.[7] In addition, a vertical NW design decouples footprint scaling from gate length and contact placement scaling.

In addition to the evolution of device architecture from planar MOSFETs to FinFETs and GAA nanowire FETs, the performance of Si-based FET is further improved by *i)* integrating group IV semiconductors and alloys like SiGe, Ge and GeSn, and *ii)* electronic band engineering with heterostructures and lattice strain. All these lead to an increased carrier mobility by reducing the effective mass of carriers. Germanium with its high hole mobility and injection velocity has yielded superior pMOSFETs electrical performance.[6,8] Very recently, vertical Ge GAA NW pFETs with excellent subthreshold properties were reported.[10-12] However, vertical NW devices suffer from an inherently large contact resistance on top of nanowires due to the very small contact area, limiting the maximum achievable device performance. Technological approaches such as laser annealing, to increase the doping concentration,[13,14] or gate-last process to increase the top contact area,[15] have been investigated to reduce the contact resistivity. The introduction of small bandgap semiconductor materials as a top layer is a promising option for the realization of a low contact resistivity. In this context, the newly developed GeSn group IV semiconductors with tunable bandgap by Sn content adjustment and the strain in the layer, largely investigated for Si photonics applications,[16,17] are taking a leading position. The breakthrough in the growth of high quality epitaxial (Si)GeSn alloys enables a new degree of freedom in group IV heterostructure

engineering.[18-20] Vertical NW structures allow designing devices that fully benefit from the band engineering with a perfect epitaxial interface and *in-situ* doping.

In this work, we present vertical $Ge_{0.92}Sn_{0.08}$/Ge heterojunction GAA NW p-type MOSFETs fabricated with a fully CMOS compatible top-down approach (**Scheme 1**). Emphasis is here put on the performance enhancement by adopting GeSn alloy as the top source of a Ge channel device. The smaller bandgap of GeSn and the GeSn/Ge band offset, together with intrinsic strain in the heterostructure, yield superior NW p-FET properties. The dependence of the key electrical figures of merits (FOMs) on the scaling of the NW diameters is studied. Devices presented here prove the advantages of band engineering with group IV heterostructures in vertical 3D nanowire devices.



Scheme 1. Schematic illustration of the GeSn/Ge heterostructure growth and vertical NW p-FET fabrication process.

RESULTS AND DISCUSSION

Heterostructure design and growth: The heterostructure is designed after considerations of the band alignment and strain engineering, in order to obtain high-performance FETs with Si-CMOS

compatible processing. Firstly, Ge virtual substrates (Ge-VS) were grown on 200 mm Si(001) wafers in an industrial reduced pressure chemical vapor deposition (RP-CVD) reactor. Then, device layers started with the growth of 200 nm thick p-type *in-situ* boron doped (~ 2.5×10^{19} cm^{-3}) Ge, followed by the growth of 150 nm thick slightly boron-doped Ge layer that defined the channel length. The heterostructure ended with the growth of a 60 nm thick $Ge_{0.92}Sn_{0.08}$ alloy layer. The high crystalline quality of the epitaxy with a defect-free $Ge_{0.92}Sn_{0.08}$/Ge interface is shown in the high-resolution (HR) transmission electron microscopy (TEM) micrographs in **Figure 1a-c**. The X-Ray Diffraction - Reciprocal Space Mapping (XRD-RSM) (**Figure 1d**) shows that the $Ge_{0.92}Sn_{0.08}$ layer has the same in-plane lattice constant as Ge, confirming the pseudomorphic growth. From the XRD-RSM, a compressive biaxial strain of -1.06% is extracted for the GeSn layer and 0.16% biaxial tensile strain for the Ge layer. Strain values are important for the calculation of the strain relaxation and, consequently, the electronic band structure in the fabricated NWs. The bulk heterostructure was completed by doping the GeSn layer with boron by ion implantation at an energy of 10 keV and a dose of 2×10^{14} cm^{-2}. A low thermal budget annealing at 400 °C resulted in an activated boron concentration of ~ 5×10^{19} cm^{-3} as indicated by the Electrochemical Capacitance-Voltage (ECV) measurements in **Figure 1e**.

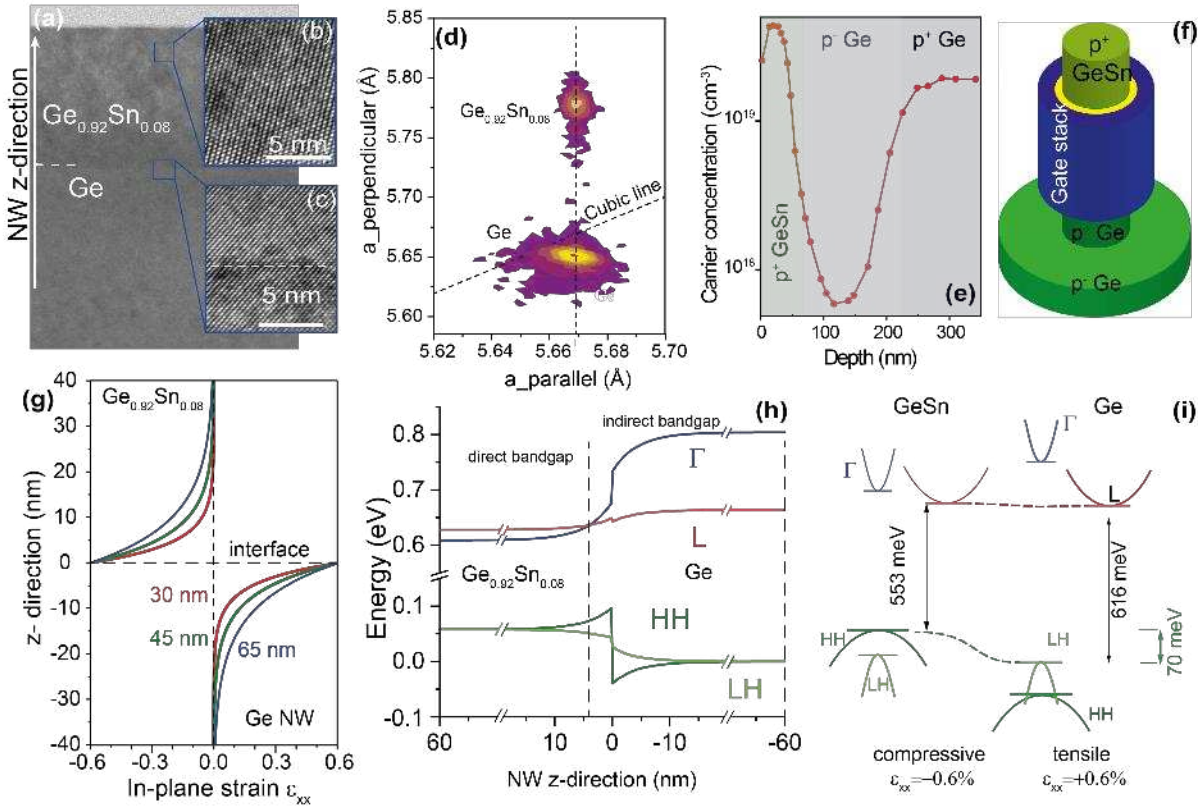


Figure 1. *(a) Cross-sectional TEM image of the 60 nm thick $Ge_{0.92}Sn_{0.08}$ layer grown on Ge. The arrow shows the direction of the NW. HR-TEM micrograph for (b) the $Ge_{0.92}Sn_{0.08}$ layer, and (c) the $Ge_{0.92}Sn_{0.08}$/Ge interface, showing the high crystalline quality and the defect-free interface. (d) XRD-RSM of the heterostructure. The peaks of $Ge_{0.92}Sn_{0.08}$ and Ge lie along the same in-plane lattice vector, indicating the layer is fully strained. (e) Activated dopant distribution in the layers measured by ECV. (f) Schematic view of a vertical GeSn/Ge NW p-FET. (g) In-plane strain ε_{xx} variation along the NW z-direction for different NW diameters. The calculated band energies along z-axis (h) and at the interface (i) for a 30 nm diameter GeSn / Ge NW heterostructure after accounting for the strain relaxation in the nanowire.*

Calculations of the electronic band structure and its strain dependence were performed using the 8-band k·p method, with expressions and material parameters as given in Ref.[21]. L-valley was considered within the simple effective mass method and deformation potentials, since the full k·p

calculation would require a larger number of bands to be included. The band edges of the $Ge_{0.92}Sn_{0.08}$ layers in the initial as-grown state are given in the supplementary information (SI) in **Table S1** and the band alignment of the $Ge_{0.92}Sn_{0.08}$/Ge heterostructure is plotted in **Figure S1**. The bandgaps for fully strained as-grown $Ge_{0.92}Sn_{0.08}$ layer are $E_{gap-\Gamma} = 0.604$ eV, and $E_{gap-L} = 0.538$ eV.

The reduced dimensionality of a NW yields an anisotropic strain relaxation. The variation of the in-plane strain, ε_{xx} along the NW axis (z-direction), for 3 NW diameters is plotted in **Figure 1g**. According to finite-element calculations,[22] and also from atomistic modelling,[23] the in-plane strain decays along the NW axis exponentially from the interface (z=0), as $\varepsilon_{xx} = \varepsilon_{yy} = \varepsilon_{xx0}\exp(-\alpha|z|)$, where, to a very good approximation, $\alpha = 7/D$ (D is the NW diameter). The strain at the interface is calculated from the relaxed lattice constants (a_1, a_2) of the two materials, as $\varepsilon_{xx0} = (a_1 - a_2)/(a_1 + a_2)$. The calculated in-plane strain is positive (tensile) in Ge and negative (compressive) in GeSn. With no external force applied to the NWs, the strain in the axial direction is given by $\varepsilon_{zz} = -(2C_{12}/C_{11})\varepsilon_{xx}$, where C_{11} and C_{12} are the stiffness constants. These values of strain are calculated along the NW axis. Off the axis, the strain approximately varies as $\propto \cos(\frac{\pi r}{D})$, where r is the radial distance from the NW axis. The strain has an impact on band energies, changing from indirect at the interface to a direct bandgap at the top of the NWs, as shown in **Figure 1h**. At the top of the NW where the strain is negligible, the $Ge_{0.92}Sn_{0.08}$ alloy has a direct bandgap of $E_{gap-\Gamma} = 0.551$ eV, and $E_{gap-L} = 0.570$ eV. At about 5 nm away from the $Ge_{0.92}Sn_{0.08}$/Ge interface, under increased compressive strain, the $Ge_{0.92}Sn_{0.08}$ becomes an indirect semiconductor, with $E_{gap-\Gamma} = 0.580$ eV and $E_{gap-L} = 0.553$ eV at the interface. The band structure at the GeSn/Ge interface in the center of a 30 nm diameter NW is schematically shown in **Figure 1i**. More results regarding the variation of band energies along the NW length, following the strain evolution in the

heterostructure for 30 nm diameter NWs, are given in SI (**Figure S1**). Quantization, present in NWs of finite length and diameter, is calculated using the effective mass method, assuming the decoupling of the axial and radial directions. The effective masses of Γ-, HH, and LH bands are obtained from the 8-band k.p Hamiltonian with strain. For the L electrons, the projections of longitudinal and transverse masses of the L-valley in the corresponding directions are used. In finding the axial quantization states the band-edge energies along the NW center are used in the 1D Schrödinger equation, as a reasonable approximation. These energies depend on the NW diameter, because of different strain profiles in the axial direction. Important for p-FETs discussed here are the valence band offsets ΔEv_{HH} = 140 meV, ΔEv_{LH} = 20 meV. The "effective band offset" ΔEv, taken as the spacing between the highest valence band states of GeSn and Ge, is 70 meV.

To realize vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA NW pMOSFETs, schematically displayed in **Figure 1f**, the fabrication processes (**Scheme 1**) have to be carried out at a low thermal budget, in order to maintain the structural stability of the GeSn alloy.[24] The details of the fabrication processes are given in SI, and only the main features are described here. GeSn/Ge NWs with diameters from 32 nm to 65 nm were produced (see **Figure S2** in SI). Exemplarily, overlapped SEM images of vertical GeSn/Ge NW with various diameters and a height of 220 nm are shown in **Figure 2a**.

The high-κ dielectric is formed by multi-step deposition using an optimized post-oxidation passivation process by means of atomic layer deposition (ALD).[9,25] It starts with an ultra-thin 1 nm Al_2O_3 at 250°C in the ALD chamber, followed by a post-oxidation process with O_2 plasma. Next, 8 nm Al_2O_3 and 40 nm TiN are deposited to conformally wrap around the vertical NWs (**Figure S3**). After gate patterning, two steps of spin-on-glass (SOG) planarization and back-etching were used to position the top gate stack and the isotropic etching was applied to remove the gate stack on the top of NWs (**Figure 2b**), and to form the top NiGeSn contact with Ni sputtering and

annealing (**Figure 2c**). The cross-section of the fabricated device structure is shown in a TEM image in **Figure 2d.** The high resolution (HR)-TEM micrograph in **Figure 2e** reveals the excellent crystallinity of the Ge channel and its high quality interface with the gate stack.

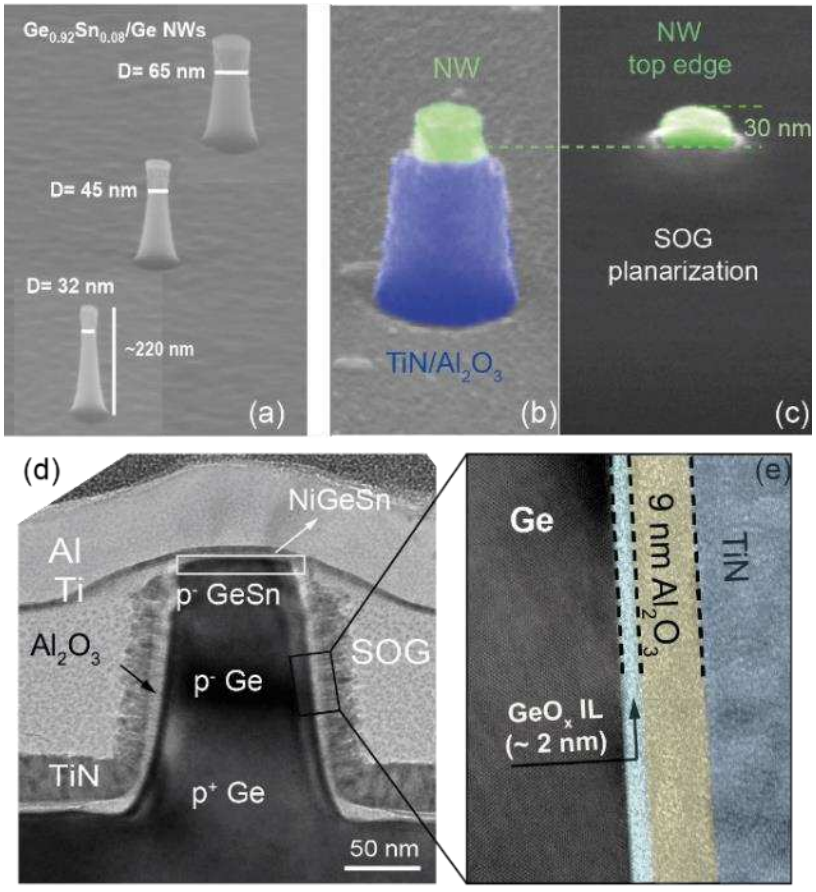


Figure 2. *(a) Overlapped tilted SEM images of GeSn/Ge NW of different diameters and a height of 220 nm. (b) Gate stack all-around NW channel and free source region. (SOG is removed by HF) (c) SOG planarization before NiGeSn metallization. (d) Cross-sectional TEM image of a fabricated vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA NW pMOSFET. (e) HR-TEM micrograph showing high crystallinity of the Ge channel and excellent interface with the gate stack consisting of ~2 nm GeO_x interfacial layer (IL) and 9 nm Al_2O_3.*

For purpose of comparison, homojunction Ge devices were also fabricated with similar feature dimensions and layout. The main differences between the Ge and the GeSn/Ge

heterostructure FETs are: i) the top Ge layer was *in-situ* doped, instead of by ion implantation, and ii) the post-oxidation was done by thermal oxidation at 500°C for a better dielectric/Ge interface passivation, which cannot be used for GeSn devices because of the thermal budget limitation.

Electrical characterization

The superior gate electrostatic integrity is evidenced by the drain current (I_D) versus gate-source voltage (I_D-V_{GS}) transfer characteristics (**Figure 3a**). Note that in this work the current is normalized to the NW perimeter and the measurements are conducted with the top-contact as the source. The threshold voltage, V_{TH}, is defined to be the gate voltage for a constant I_D=100nA/μm. The vertical GeSn/Ge NW FET with a diameter of 32 nm and a gate length of 150 nm delivers steep subthreshold swing (*SS*) of 72 mV/dec and a large on-/off current ratio I_{ON}/I_{OFF} ~3×10^6 at V_{DS} = -0.1 V (**Figure 3a** blue lines). *SS* and I_{ON}/I_{OFF} ratio become inferior with increasing the NW diameters, reaching 84 mV/dec and ~8.4×10^5, respectively, for devices with a NW diameter of 65 nm. More device characteristics are given in SI. The I_D-V_{GS} characteristics of a 65 nm diameter Ge NW pFET show a slightly lower *SS* of 68 mV/dec (see SI **Figure S4**). The performance improvement achieved with the use of GeSn as a top source is clearly evidenced by comparing the output characteristics (i.e. drain current versus drain voltage, I_D-V_{DS}), of the corresponding devices (**Figure 3b**). At low voltages of V_{GS}-V_{TH} = -0.5V and V_{DS} = -1V the GeSn/Ge device shows a ~32% I_{ON} enhancement in comparison with the Ge pFET for a NW diameter of 65nm. The device performance improvement, obtained by using GeSn as the source, is also confirmed by the transconductance, as indicated in **Figure 4a**. The maximum transconductance, G_{max}, decreases with the nanowire diameter. However, all GeSn/Ge devices show much larger G_{max} than homojunction Ge FETs. Consequently, the total resistance (R_{tot}) of the GeSn/Ge devices is much smaller than that of the Ge NW pFET. Due to the smaller bandgap of GeSn and the band offset to the Ge channel,

as illustrated in **Figure 1** and **Figure 4**, a smaller Schottky barrier height (SBH) is indeed obtained with $NiGe_{0.92}Sn_{0.08}/Ge_{0.92}Sn_{0.08}$ than with NiGe/Ge junctions, which results in a lower contact resistivity, and thus a lower R_{tot}, improving both G_m and I_D. For both types of devices, the total resistance shows a decreasing trend with increasing NW diameters, which reflects the decreasing contact resistance with increasing geometrical contact areas. Compared to the Ge device, the GeSn/Ge p-FET shows a smaller R_{tot} increase rate as the NW diameter reduces. The contact resistance depends on the contact area, the SBH and the doping in the semiconductor layer. For the Ge NW device, possible boron deactivation[26] in the top Ge for smaller NWs and less B segregation during NiGe formation[27] cause rapid contact resistance increase as the NW diameter decreases. For GeSn/Ge NW p-FETs, a higher density of boron segregated at the NiGeSn/GeSn interface [28] and the smaller SBH of NiGeSn/GeSn result in lower contact resistance increasing rate with decreasing NW diameter, compared to the Ge p-FET.

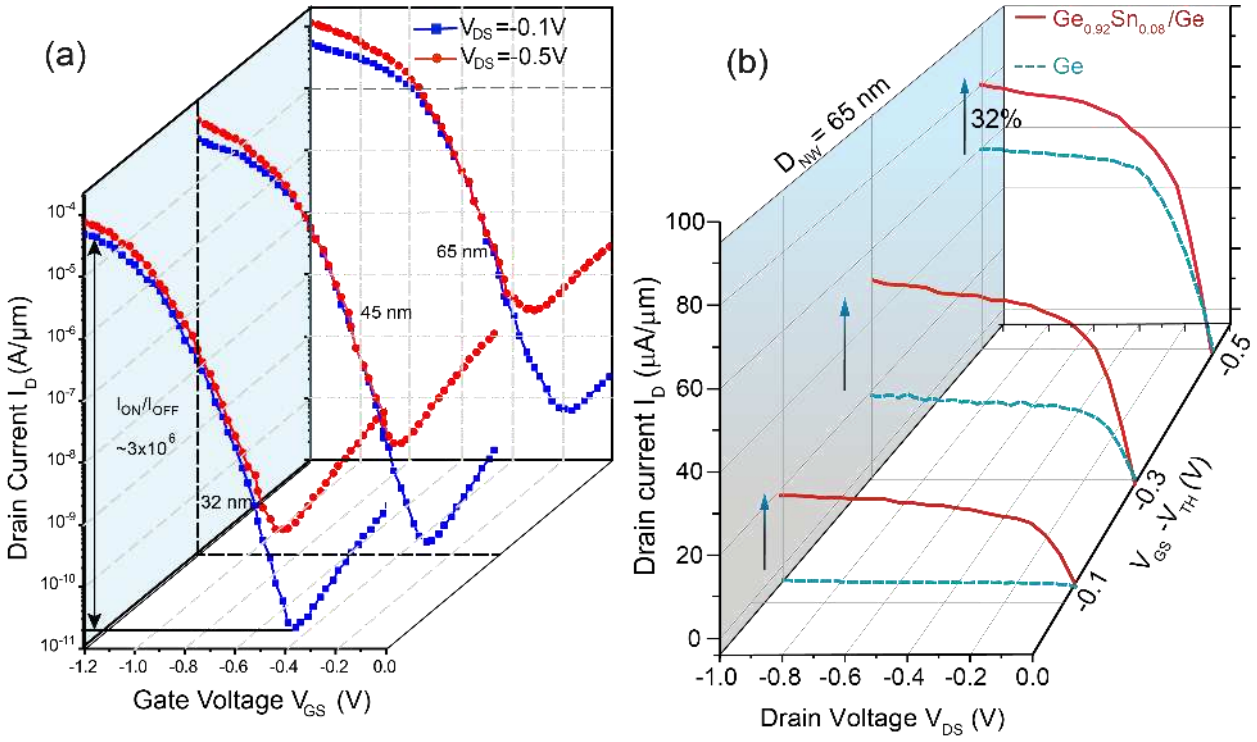


Figure 3. *(a) I_D-V_{GS} transfer characteristics for vertical GeSn/Ge NW GAA pFETs with various NW diameters, showing high I_{ON}/I_{OFF} ratio and small SS. (b) Comparison of the I_D-V_{DS} output characteristics of a GeSn/Ge heterostructure pFET with that of a reference Ge homojunction device, for a NW diameter of 65nm in both cases. The GeSn/Ge pFET shows much larger currents than its Ge counterpart for any gate driving voltage V_{GS}-V_{TH}.*

Next, the influence of the NW diameter scaling on the electrical characteristics of GeSn/Ge and Ge pFETs is studied by analyzing the dependence of *SS* and drain-induced-barrier-lowering (DIBL) on the NW diameters. **Figure 5** shows data points extracted from the electrical characteristics of GeSn/Ge and Ge pFETs. Here, each data point represents the average value based on > 20 devices with the same NW diameter and processing conditions. Generally, GeSn/Ge NW devices exhibit larger *SS* than their Ge counterparts (**Figure 5a**). The reason for this is the low thermal budget limitation of GeSn/Ge devices, which requires the use of an O_2 plasma post-oxidation, thus yielding a higher density of interface traps (D_{it}) compared to the thermal oxidation as used for Ge devices. However, while the *SS* of Ge pFETs slowly decreases as the NW diameter decreases, a steep decrease is observed for GeSn/Ge pFETs, reaching almost the same small values as the Ge pFETs. This effect stems from the increased gate control when the NW diameter is reduced. In fact, by representing the device as a series and parallel combination of capacitors in a top-of-the-barrier model, *SS* is approximately given by

$$SS = \frac{k_B T}{q} \ln(10) \left[1 + \frac{C_d}{C_{ox}} + \frac{C_{it}}{C_{ox}}\right] \qquad (1)$$

where $C_{ox,d,it}$ are the oxide, the depletion, and the interface state capacitances as described in the following.

$$C_{ox} = 2\pi\varepsilon_0\varepsilon_{ox}\frac{L}{ln\left(1+2\frac{d_{ox}}{D}\right)} \qquad (2)$$

$$C_d \approx \varepsilon_0\varepsilon_{nw}\frac{\pi d_{nw}^2}{4L} \qquad (3)$$

$$C_{it} \approx e^2 D_{it}\pi DL \qquad (4)$$

It is clear that an overall larger *SS* and a reduction of *SS* with decreasing NW diameter *D* are expected for the GeSn device, because of the larger C_{it} compared to that of the Ge device.

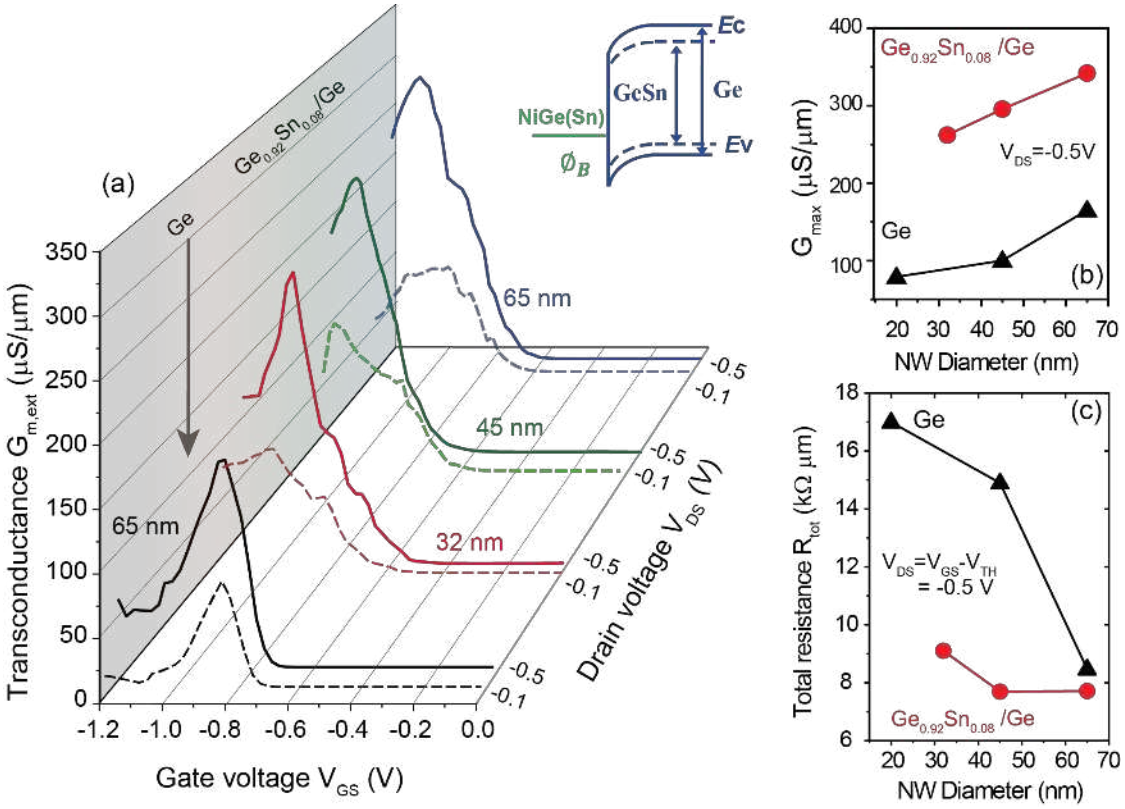


Figure 4. *(a) Transconductance profiles for different NW diameter GeSn/Ge and Ge pFETs at V_{DS}=-0.1V and -0.5V. All the GeSn/Ge devices show much higher transconductance than the reference Ge homojunction devices with a NW diameter of 65nm. (b) The maximum transconductance G_{max} increases with the NW diameter. GeSn/Ge FETs show much higher G_{max} than Ge homojunction devices. (c) Total resistance R_{tot} of the device as a function of NW diameter,*

showing a decreasing R_{tot} with increasing NW diameters. GeSn devices have reduced R_{tot} due to the lower Schottky barrier of NiGeSn/GeSn than NiGe/Ge contacts, as illustrated by the band energy.

Next, the behavior of DIBL in GeSn/Ge devices is compared to that in Ge pFETs. Instead of an increase of the DIBL with the nanowire diameter, as observed in the case of Ge pFETs, DIBL for the GeSn/Ge pFETs remains almost constant. This behavior may appear counterintuitive at first sight. However, using again the capacitor representation based on a top-of-the-barrier model, the DIBL can be written as a change of the top-of-the-barrier with changing drain potential and hence DIBL $= \frac{C_d}{C_{ox}+C_d+C_{it}}$, which means that DIBL is suppressed if C_{it} is sufficiently large. As a result, the expected increase of DIBL is observed only in the Ge devices with low D_{it}. In GeSn/Ge devices, C_{it} is expected to be substantially larger (due to the low thermal budget processing) and consequently, a smaller DIBL is observed, as displayed in **Figure 5b**. However, while the simple capacitor relation can explain partially the DIBL reduction in GeSn/Ge devices, it does not reproduce well the fact that DIBL in the GeSn/Ge device is almost constant. We, therefore, suggest that the reason for the rather constant DIBL is the valence band offset ΔE_v at the $Ge_{0.92}Sn_{0.08}$/Ge heterojunction. As indicated in **Figure 1h**, the strain at the GeSn/Ge hetero-interface has a different impact on the light- and heavy-hole valence bands: while the heavy hole band shows a rather large valence band offset, the light holes have only a very small offset. As a result, a dipole layer builds up at the hetero-interface in the heavy-hole band, which reduces the impact of drain since it is screened by the large carrier density within this dipole layer. The latter due to the large band offset, would lead to a substantial reduction of the drain current. However, due to the strain-induced,

different behavior of the light-hole band, there is almost no potential barrier for the light holes. This means, that the heavy holes lead to a rather stationary charge that reduces DIBL while the light holes contribute mostly to the current. This effect together with high D_{it} as we discussed above result in much lower DIBL for the GeSn/Ge p-FETs. Therefore, the particular GeSn/Ge heterostructure, in combination with an appropriate strain field, yields a major scaling benefit compared to homojunction devices.

In order to verify our considerations regarding the impact of the GeSn/Ge heterostructure and the suppression of DIBL, we performed self-consistent device simulations based on the non-equilibrium Green's function formalism (NEGF). The effective mass approximation, with multiple independent subbands, was used. The heterostructure offsets and the impact of strain on the light- and heavy-hole bands were extracted from the calculations above (cf. **Figure 1**). Scattering in the device was accounted for with Büttiker probes.[29] The electrostatics of the wrap-gate architecture was taken into consideration with a one-dimensional modified Poisson equation.[30] More detail about the device simulations is presented in **SI**. **Figure 5c** shows DIBL values as extracted from the self-consistently calculated valence band profiles at V_{gs}=0V. Note that in order to decrease the computational burden, substantially shorter devices of 20nm with smaller NW diameter from 15 nm to 25 nm were considered here, compared to the experimental devices. As a result, the absolute value of DIBL is significantly larger than in the experiments. The qualitative behavior, however, is well reproduced.

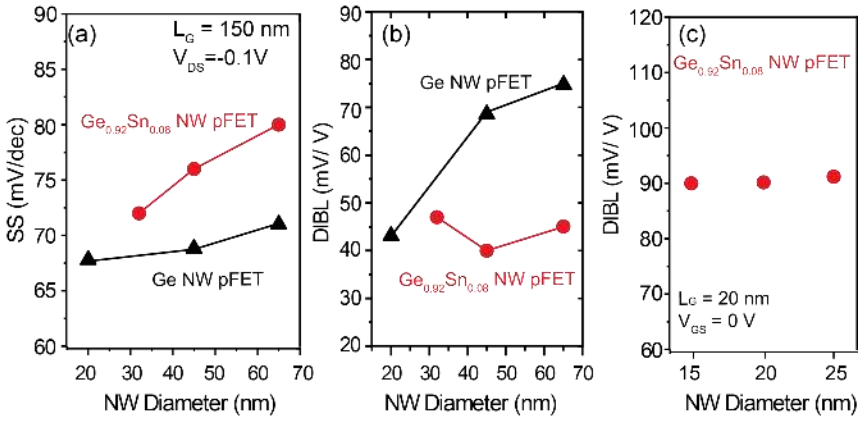


Figure 5. *(a) Measured SS as a function of NW diameters (b) Measured DIBL as a function of NW diameters. The Ge homojunction device shows a decreasing DIBL with decreasing NW diameters due to improved gate control. The GeSn/Ge pFET shows almost a constant DIBL. (c) DIBL extracted from self-consistent NEGF simulations in the case of a GeSn/Ge device, showing a constant DIBL, in agreement with the experimental results in (b).*

CONCLUSIONS

High-performance hetero-epitaxial GeSn/Ge GAA NW p-FETs were presented. Vertical NW architecture enables us to fully benefit from (i) band engineering in such group IV heterostructures, (ii) an excellent charge electrostatic control with such GAA devices and (iii) high quality of an epitaxial GeSn/Ge interface. We thus succeeded in improving GeSn/Ge transistor's figures of merits such as G_m, DIBL and I_{on}/I_{off} ratios over Ge control devices. The use of low and direct bandgap GeSn alloys as the source strongly decreases the total resistance, resulting in 32% higher drive currents. The band engineering with strain in the GeSn/Ge heterostructure gives a big advantage by reducing the DIBL. The full potential of GeSn semiconductor for CMOS functionality is still to be revealed through n-GeSn FETs devices with high electron mobility GeSn channels. Last but not least, strain engineering together with bandgap tunable GeSn/SiGeSn

advanced heterostructures, as used in photonics research, offer future perspective for the monolithic integration of group IV-based microelectronic and photonic applications.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

ASSOCIATED CONTENT

Supporting Information. Additional information on band structure calculation for GeSn/Ge, device fabrication and characterization are given in SI file.

Supporting Information (word file)

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– Supporting Information –

Epitaxial GeSn/Ge Vertical Nanowires for p-Type Field-Effect Transistors with Enhanced Performance

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1. Material growth and characterization

Ge and GeSn/Ge heterostructures are grown by reduced pressure chemical vapor deposition (RP-CVD) in an industrial reactor. Germane, GeH_4, is used as precursor gas for the Ge-epitaxy and,

digermane, Ge_2H_6, and tin-tetrachloride $SnCl_4$ precursors for GeSn epitaxy. Diborane, B_2H_6, precursor was used for p-type (B) *in-situ* doping. The stoichiometry extracted from Rutherford backscattering spectrometry (RBS) is used as an input parameter in the XRD to determine the lattice strain in both Ge and GeSn layers.

2. *Band structures*

The band edges for strained $Ge_{0.92}Sn_{0.08}$ and Ge in "bulk form" (as-grown case) are given in the **Table S1** below. The "effective bandgaps" taken as spacing between the lowest conduction band state and the highest valance band state for as-grown $Ge_{0.92}Sn_{0.08}$ are $E_{gap\text{-}\Gamma}$=0.604 eV, and $E_{gap\text{-}L}$=0.538 eV. The band alignment of the GeSn/Ge heterostructure is given in **Figure S1**. For the relaxed case, cubic GeSn is a direct bandgap alloy with the bandgaps $E_{gap\text{-}\Gamma}$ = 0.551 eV, and $E_{gap\text{-}L}$=0.570 eV.

Table S1. *Calculated band energies for as grown strained GeSn and Ge layers.*

Sn content (at.%)	Ev_{HH} (eV)	Ev_{LH} (eV)	E_Γ(eV)	E_L(eV)	Biaxial strain (%)
0	0.000	0.000	0.664	0.804	0
0	-0.017	-0.001	0.779	0.651	0.16
0.080	0.058	0.058	0.609	0.628	0
0.080	0.121	0.029	0.725	0.659	-1.06

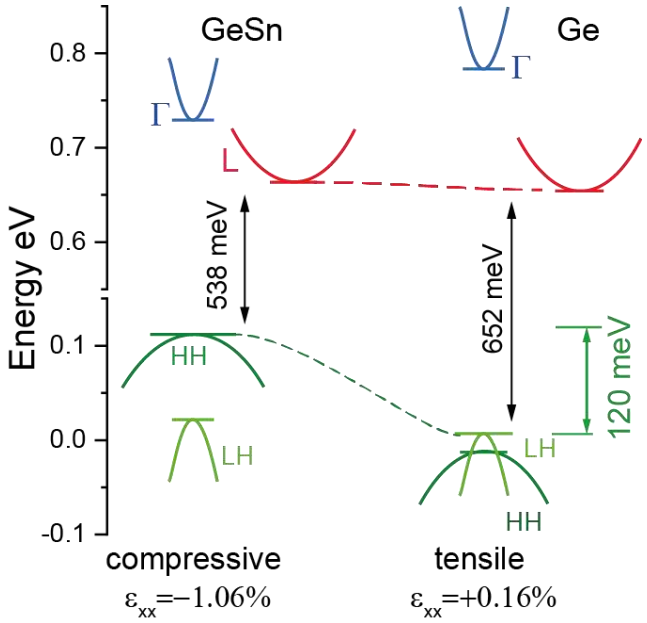

Figure S1. *Electronic bands alignment for the as-grown GeSn/Ge heterostructure.*

The quantised states of electrons and holes in a quantum wire were calculated within the effective-mass approximation. Mixing of bands near Γ point was neglected. The heavy-hole, light-hole, and the Γ and L conduction bands were described by appropriate effective masses. In the presence of strain these masses are different in different directions. We have used the approximation that the in-plane mass ($m_{\|}$) is the same in any direction in the wire cross section, but is different from the mass in the axial, z-direction (m_z). The values of $m_{\|}$ and m_z are very different for both heavy and light holes, and also slightly depend on strain, while they are very similar for electrons, as given in **Table S2** for $Ge_{0.92}Sn_{0.08}$, calculated by the *k.p* method. The potential (band edge energy *V(z)*) for the particular carrier type, depends on the material composition and local strain (calculated from the strain value and deformation potentials), as given in **Table S3** for $Ge_{0.92}Sn_{0.08}$. But is here approximately taken to be constant across the wire cross-section, and becomes infinite at the wire surface. It may only depend on *z* in heterostructure wires. Within these approximations the Hamiltonian / Schrödinger equation in cylindrical coordinate system (with *r* the radial coordinate, *z* the axial, and ϕ the azimuthal angle) is

$$-\frac{\hbar^2}{2m_0}\left[\frac{1}{m_{\|}}\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\right)+\frac{1}{r^2}\frac{\partial^2}{\partial\phi^2}+\frac{\partial}{\partial z}\frac{1}{m_z}\frac{\partial}{\partial z}\right]\Psi+V(z)\Psi=E\Psi \qquad \text{(S1)}$$

The wave function can then be factorised as

$$\Psi=\mathrm{R(r)Z(z)\Phi(\phi)} \qquad \text{(S2)}$$

with $\Phi=e^{im\phi}$ (*m* is the azimuthal quantum number) the radial component of energy is given by

$$E_{l,m}=\frac{\hbar^2}{2m_0}\left(\frac{q_{l,m}}{r_0}\right)^2 \qquad \text{(S3)}$$

where $q_{l,m}$ is *l*-th root of *m*-th order Bessel function $J_m(q)=0$, r_0 is the wire radius, and *l* the radial quantum number. The axial component of energy is found by solving the 1D Schrödinger equation by finite-difference method. For single-composition wire of length *L* the axial component of energy would simply be $E_n=\left(\frac{\hbar^2}{2m_0m_z}\right)\left(\frac{n\pi}{L}\right)^2$, where *n* is the axial quantum number.

***Table S2**. Calculated effective masses in $Ge_{0.92}Sn_{0.08}$ with biaxial compressive strain.*

ε_{xx}	m_{HHz}	$m_{HH\parallel}$	m_{LHz}	$m_{LH\parallel}$	$m_{\Gamma z}$	$m_{\Gamma\parallel}$	m_{Lz}	$m_{L\parallel}$
0.000	0.222	0.029	0.020	0.050	0.032	0.032	0.117	0.293
-0.002	0.222	0.029	0.022	0.052	0.034	0.032	0.117	0.293
-0.004	0.222	0.028	0.024	0.052	0.036	0.032	0.117	0.293
-0.006	0.222	0.027	0.026	0.050	0.038	0.033	0.117	0.293

***Table S3**. Calculated band edges in $Ge_{0.92}Sn_{0.08}$ layer with biaxial compressive strain (reference zero is the v.b. top in unstrained Ge).*

ε_{xx}	E_{HH} (eV)	E_{LH} (eV)	E_{Γ} (eV)	E_{L} (eV)
0.000	0.058	0.058	0.609	0.628
-0.002	0.071	0.052	0.632	0.635
-0.004	0.085	0.047	0.656	0.642
-0.006	0.098	0.043	0.679	0.650

3. Device fabrication

The fabrication process of vertical GeSn/Ge NW p-MOSFETs is presented in **Figure S2**. After e-beam lithography and etching, vertical NWs are formed. Digital etching consisting of multiple cycles of self-limiting O_2 plasma oxidation and diluted HCl stripping is applied to shrink the NW diameters. Note that the planar surface is not perfectly smooth due to Cl_2 –based dry etching. It

was reported that $SnCl_x$ by-products are non-volatile at low temperatures. Therefore during our etching at 0°C, these by-products are redeposited as hard masks, which roughen the planar surface.

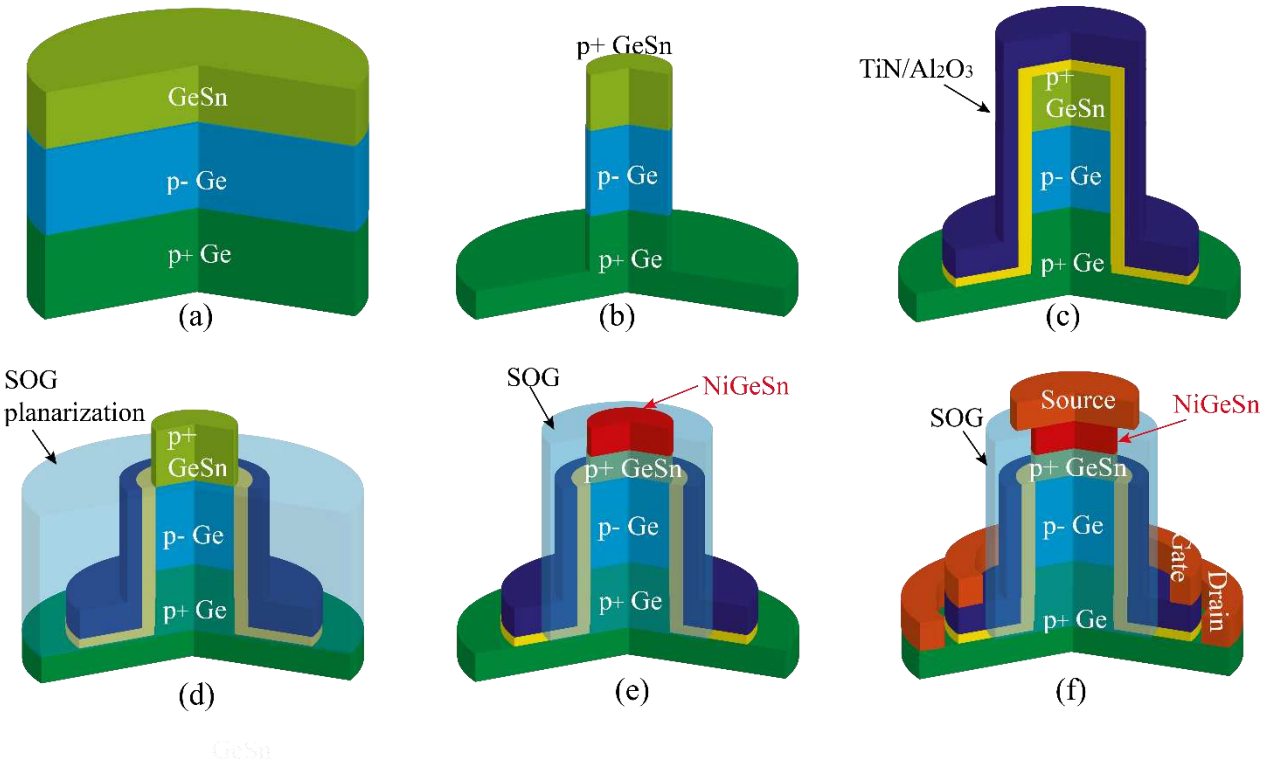

Figure S2*: Schematic of vertical GeSn NW p-MOSFETs fabrication process. (a) layer stack grown by CVD, (b)Vertical GeSn/Ge NW fabrication by top-down process; (c) TiN/Al_2O_3 gate stack deposition; (d) SOG planarization and etch back following by gate stack removal from the top of the NW; (e) NiGeSn formation after SOG planarization to isolate the gate to the top of the NW; (f) metallization of the S/D and gate.*

Subsequently high–κ dielectric deposition starts with an ultra-thin 1 nm ALD Al_2O_3 followed by a post-oxidation process treatment in O_2 plasma. The oxidation passivates the Ge dangling bonds, forming a ~2 nm GeO_x interfacial layer (IL), and saturates oxygen vacancies in the Al_2O_3 layer. The gate stack is completed by 8 nm ALD Al_2O_3 and 40 nm TiN conformal deposition around the vertical NWs. EDX elemental distribution across the Ge/gate stack interface is plotted in Fig SI3.

After gate patterning, planarization is performed by spin-coated spin-on-glass (SOG) and cured at 350 ºC followed by isotropic back-etching with CHF_3. The exposed top gate stack is

removed by an optimized Cl_2/SF_6 etching recipe. Subsequently, a second SOG spin-coating and planarization are performed to isolate the gate stack and top contact. Via openings through the SOG layer are formed and finally Ti/Al contact metallization is conducted to finish the device fabrication. For comparison, Ge control devices with p+-p$^-$-p+ doping scheme are also fabricated at the same experimental conditions except the post-oxidation passivation. Thermal oxidation method at 500°C instead of O_2 plasma is applied to passivate the Ge NWs after 1nm Al_2O_3 ALD. The equivalent oxide thickness (EOT) is kept similar, ~ 5 nm for both GeSn/Ge and Ge NW pMOSFETs.

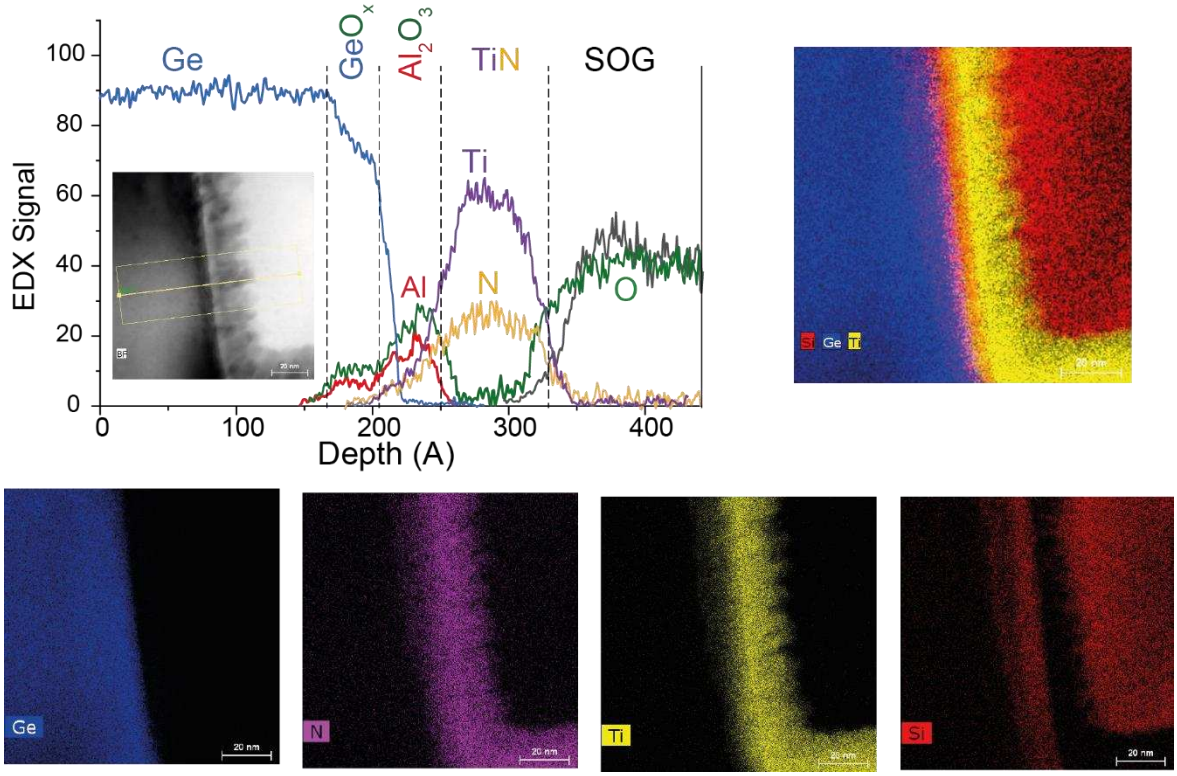

***Figure S3**: EDX elemental distributions at the lateral Ge/gate stack interface.*

4. Comparison of Ge and GeSn devices

The transfer characteristics for vertical GAA GeSn/Ge and Ge NW pFETs with 65 nm diameter NWs are presented in **Figure S4 (a)**. The shift of V_{TH} for GeSn/Ge device could be caused by different D_{it} and other process variations. Higher on-currents for the GeSn/Ge device than the

Ge pFET are demonstrated under normalized overdrive gate voltage $V_{OV} = V_{GS} - V_{TH}^{'}$, where the threshold voltage $V_{TH}^{'}$ is determined from the linear I_D vs V_{GS} curve (**Figure S4(b)**). The linear I_D~V_{GS} plot in the inset of **Figure S4(b)** shows more clearly the current increase. Much larger drain current improvement is found for 45 nm diameter p-FETs by comparison the GeSn/Ge and Ge NW devices, as shown in **Figure S4 (c).**

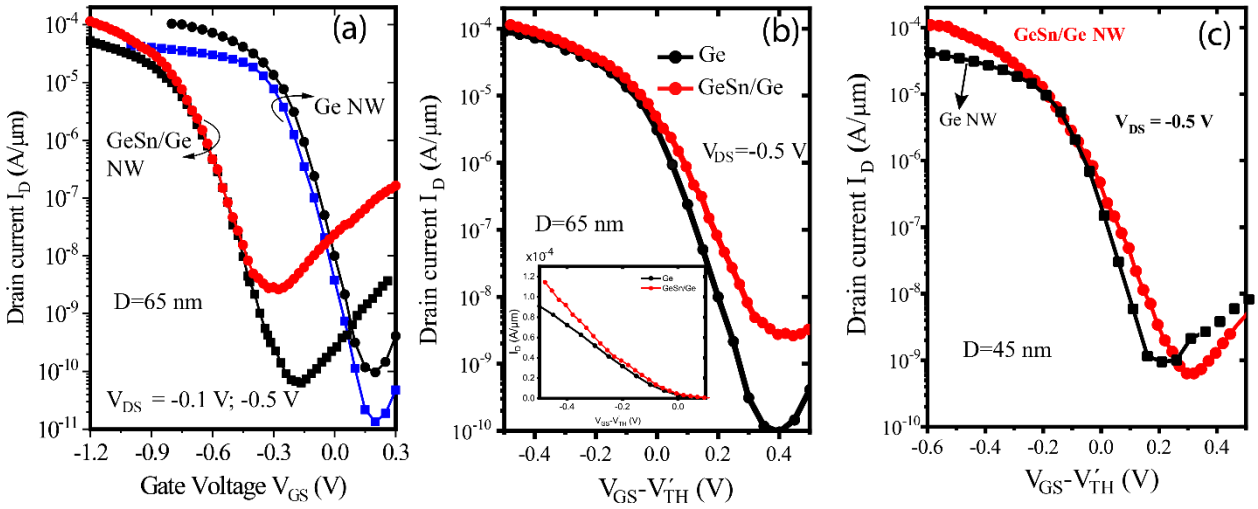

Figure S4*. Comparison of electrical characteristics between GeSn/Ge and Ge GAA pFETs with a NW diameter of 65 nm. (a) Transfer characteristics, showing a subthreshold swing SS of 68mV/dec for Ge and 84mV/dec for GeSn/Ge NW devices at V_{DS}=-0.1V, (b) Transfer characteristics in logarithmic scale of I_D and linear I_D (inset) for the 65 nm diameter devices under normalized V_{GS}-$V^{'}_{TH}$, showing the on-current increase. (c) Transfer characteristics for p-FETs with a NW diameter of 45 nm further demonstrate the current improvement by using GeSn as source.*

5. Device Simulations

For simulations of the device we used a home-made self-consistent Poisson-Schrödinger solver that is based on the non-equilibrium Green's function formalism (NEGF). To simplify the computation, an one-dimensional modified Poisson equation was used that is very well suited to describe the electrostatics of ultrathin-body FETs such as fully-depleted silicon-on-insulator,

nanowire and nanotube devices.[1-3] In the case of the NEGF, an effective mass approximation is employed on a finite difference grid with lattice spacing $a = 0.5\,nm$ and energy-dependent effective masses to account for the complex band structure (Flietner's dispersion relation[4]). The following effective mass tensor is used:

$\begin{pmatrix} m^*_{lh,\parallel} & 0 & 0 \\ 0 & m^*_{lh,\perp} & 0 \\ 0 & 0 & m^*_{lh,\perp} \end{pmatrix}$ for the light hole band with $m^*_{lh,\parallel} = 0.023$ in the direction of current transport (nanowire axis) and $m^*_{lh,\perp} = 0.05$ perpendicular (leading to the formation of 1D subbands due to carrier confinement). For the heavy hole band the used effective mass tensor is:

$\begin{pmatrix} m^*_{hh,\parallel} & 0 & 0 \\ 0 & m^*_{hh,\perp} & 0 \\ 0 & 0 & m^*_{hh,\perp} \end{pmatrix}$ with $m^*_{hh,\parallel} = 0.222$ in the direction of current transport and $m^*_{lh,\parallel} = 0.026$ in the perpendicular direction. For simplicity, these effective mass tensors were used throughout the device structure. The error made with this assumption plays a substantially smaller role compared to the modification of the band structure due to the strain at the heterointerface that has been incorporated as described further below.

Multiple independent one-dimensional modes for heavy and light hole bands have been included in the simulations. Moreover, ballistic transport and room temperature conditions are assumed. This tool has been successfully used to simulate the device characteristics of UTB SOI MOSFET, nanowire/nanotube transistors, Schottky-barrier FETs as well as band-to-band tunneling FETs.[5-8]

The device structure considered in the manuscript is a wrap-gate nanowire FET with a diameter D=15nm, 20nm, and 25nm, a SiO_2 gate dielectric of thickness d_{ox}=3nm (gate leakage is neglected for simplicity) and a channel length of L=20nm. The top and bottom sections (L_{source}=40nm, L_{drain}=40nm) of the nanowire are considered to be p-type doped (a homogeneous doping is assumed). At the source side, a contact to a metallic source electrode is implemented (as is the case

in the experimental transistor), yielding a Schottky-barrier height of $\emptyset_{SB} = 0.2\,eV$ due to the assumed Fermi level pinning.

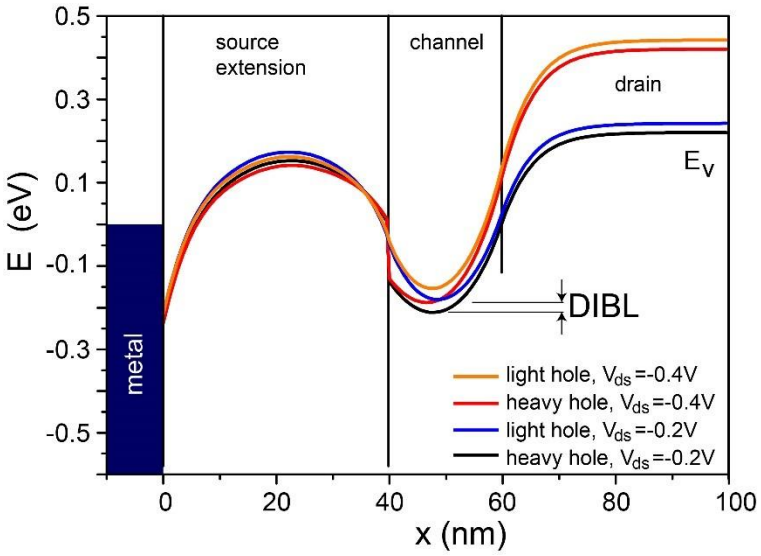

***Figure S5**. Valence bands of the first 1D subband of the heavy and light hole band including the impact of strain on the band line-up at the heterointerface (cf. **Figure 1h** in the manuscript). V_{DS}=-0.2V and -0.4V, L=20nm, D=25nm, d_{ox}=3nm; the effective mass tensors as given above are used.*

The impact of strain on the band structure has been incorporated using **Figure 1h** of the manuscript. This leads to a valence band offset of the band at the heterointerface with a gradual separation between the light and heavy hole bands (that are degenerate away from the heterointerface, see **Figure 1h**). This results in a valence band (surface potential at the nanowire/gate dielectric interface) along current transport direction as plotted in **Figure S5**.

Figure S6 displays a gray-scale plot of the local density of states along the direction of current transport showing the heavy hole band (black straight line) after convergence is achieved (Convergence is considered to be reached, when the maximum potential change along the nanowire

is less than 2 meV). The horizontal lines at the right indicate the energetic positions of the multiple light and heavy bands (the shown local density of states display the sum of the contributions from the various subbands) that are considered in the calculation.

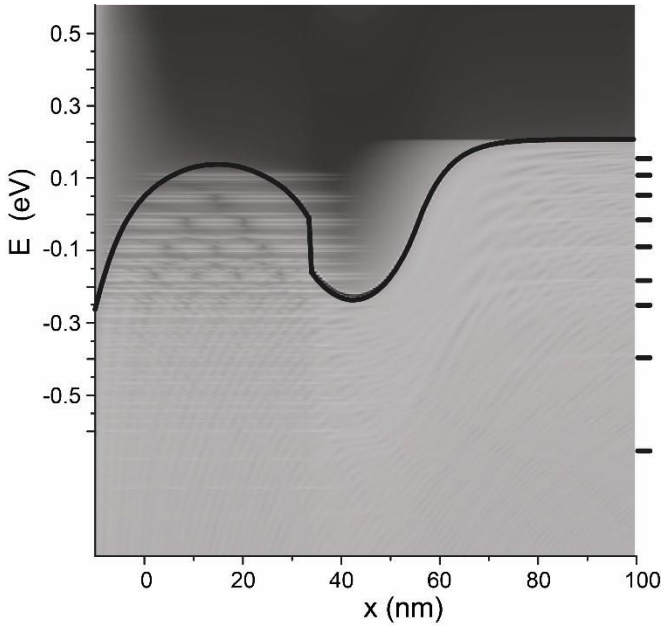

Figure S6. *Gray-scale plot of the local density of states along the direction of current transport showing the heavy hole band (black straight line).*

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