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Gunsal, I., Stone, D. and Foster, M. orcid.org/0000-0002-8565-0541 (2021) Suppressing leakage current for cascaded H-bridge inverters in renewable energy and storage systems. IEEE Transactions on Industrial Electronics, 68 (11). pp. 11035-11043. ISSN 0278-0046

https://doi.org/10.1109/tie.2020.3031524

Suppressing Leakage Current for Cascaded H-Bridge Inverters in Renewable Energy and Storage Systems

I. Gunsal, D. A. Stone, and M. P. Foster

***Abstract*—Leakage current in a transformerless cascaded H-bridge inverter is a problem that deteriorates the system performance and causes safety concerns. In this paper, a common-mode equivalent circuit is established for analyzing the occurrence of leakage current in an *m*-level cascaded H-bridge inverter with either asymmetrical or symmetrical inductance output filter configurations. The analysis provides a comparison between traditional phase shifted pulse width modulation, phase disposition pulse width modulation and the proposed leakage current reduction pulse width modulation. It is reported that grid leakage current cannot be suppressed in an asymmetrical inductance filter configuration solely based on modulation methods. The proposed LCRPWM pulse width modulation can effectively reduce the grid leakage current in a symmetrical filter configuration nine-level cascaded H-bridge inverter. Simulation and experimental studies for aforementioned methods are provided and their performances are evaluated.**

***Index Terms*—Cascaded H-bridge (CHB) inverter, leakage current, pulse width modulation, transformerless.**

I. INTRODUCTION

RENEWABLE energy systems (RES) share in the current electricity generation mix is increasing due to environmental concerns, requirement of sustainability and enforced policies [1]. With the help of policies and feed-in tariffs, photovoltaics (PV) have become more common in the form of domestic rooftop systems. Increased penetration of PVs in low voltage distribution networks causes problems for grid operators and these include voltage fluctuations [2]. Battery energy storage systems (BESS) are one of the options to reduce the stress on utility grids by acting as a buffer between supply and demand. There is a move to utilize second life electric vehicle (EV) batteries in grid support, as automotive manufacturers tend to replace them when their State of Health (SOH) reaches around 70-80% [3]. However, batteries in their second life application need to be maintained with extra care, as diminished SOH may bring many problems such as compromised performance and reliability. The cascaded H-bridge (CHB) inverter is a favorable multilevel converter (MLC) topology for hybrid PV and battery system as it inherently requires isolated power supplies, which could be produced by battery modules. The use of isolated battery modules reduces DC link voltages, offering more flexibility by allowing greater diversity in the battery's origin (age, technology and provenance). Furthermore, employing MLCs enables the implementation of modular maximum power point tracking in PV arrays, where a large PV array is divided into sections, with each section assigned to separate level in the MLC system. Additionally, a hybrid PV-battery system also enables a controllable real and reactive power (P, Q respectively) injection system into the grid, which may be beneficial for the stability of the network [4]-[5].

Grid connected systems featuring a transformer at the point of grid coupling, provides galvanic isolation and so avoids issues associated with the circulation of leakage currents. However, transformers tend to be heavy, costly, and they reduce system efficiency [6]. In transformerless topologies, a common-mode circuit occurs that results in leakage current flowing through parasitic capacitances to the ground [7]-[9]. Parasitic capacitances are mostly dominated by PV panels due to their large surface area. When the voltage across these parasitic capacitances changes, leakage current flow to ground occurs, which deteriorates the output waveforms, reduces the system efficiency and is a safety concern. The German standard VDE-0126-1-1 obligates to disconnect PV systems from the grid within 0.3s when the rms value of the leakage current or its peak value increases beyond 30mA and 300mA respectively [10].

Methods for suppressing leakage current are categorized by: 1) decoupling or clamping the parasitic capacitance [11]-[20]; 2) inclusion of common-mode chokes or filters to provide attenuation [21]-[24]; 3) applying appropriate modulation strategies to ameliorate the issue [25]-[28]. In addition, decoupling the parasitic PV capacitances from the AC side of the circuit during the freewheeling period may suppress the leakage current such as in HERIC [12] and H5 [19] topologies. In the H6 topology [18], the parasitic capacitances are clamped to the half of the DC link voltage, which restricts the voltage swing on the capacitor, therefore providing some

Manuscript received May 11, 2020; revised July 30, 2020 and September 21, 2020; accepted October 05, 2020. This work was supported in part by the UK Eng. and Physical Sciences Research Council under Grant EP/L016818/1. (Corresponding author: Izgun Gunsal)

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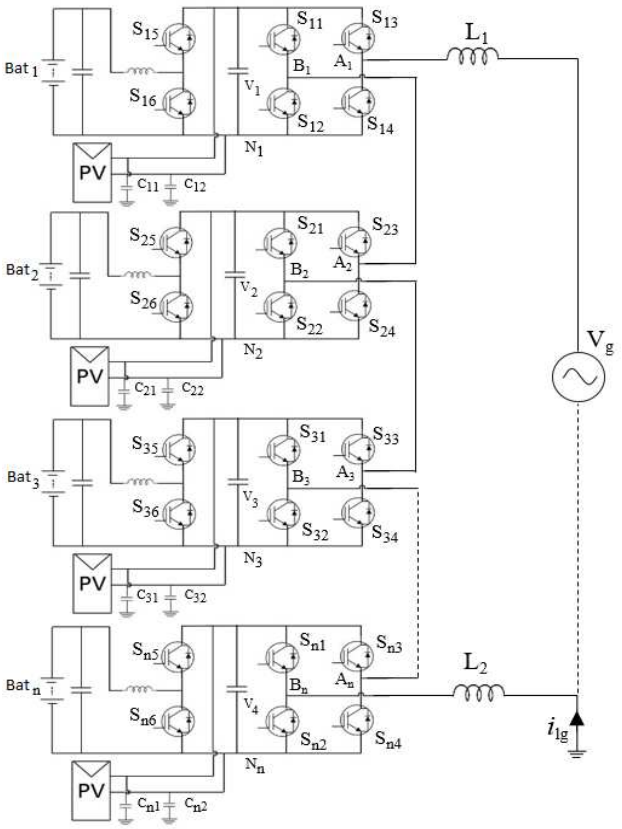

Fig. 1. Single-phase *m*-level CHB hybrid inverter.

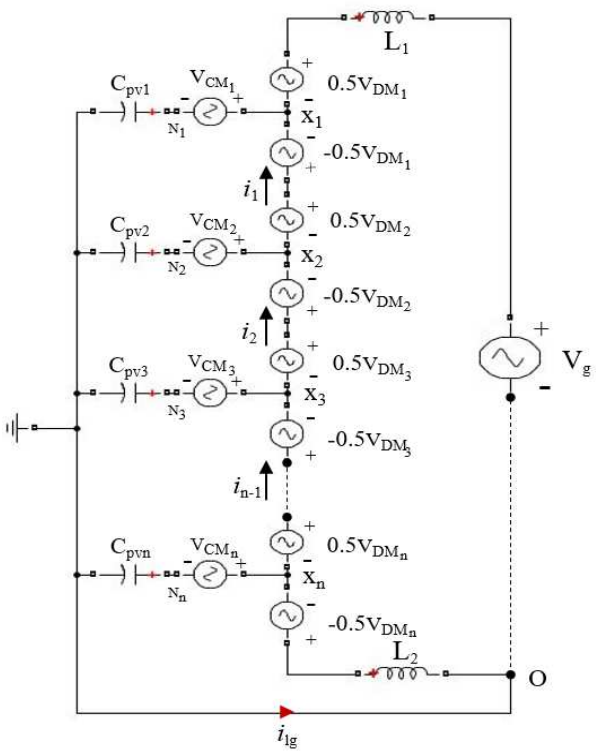

Fig. 2. Equivalent circuit of an *m*-level CHB inverter.

suppression of the leakage current. It should be noted these topologies require additional switching devices and this increases the system cost and complexity. In addition, these topologies fail to suppress the leakage current when H-bridge modules are cascaded, as there is an inter-module leakage path to the ground formed by the cascading of the converters. It is possible to reduce leakage current by adding filters to the leakage paths. In [21] and [23], authors designed and placed passive filters in the output of individual modules of a CHB. This helped in reducing the leakage current however deteriorated the voltage output of the converter. Filter circuit dramatically increase the cost, volume and weight of the CHB which unfortunately scales with an increasing number of modules. They also entail a complex design process and cannot be applied directly to different system topologies. Applying appropriate modulation methods to stabilize the common-mode voltage during the whole switching cycle does not require extra circuitry and provides the cheapest and often the most energy efficient solution. In [26]-[28], sinusoidal pulse width modulation (SPWM) methods are presented for a five-level CHB, however the converter is observed to leak current to ground while transitioning through zero state of the switching cycle and therefore reported modulation scheme fails to conform to VDE-0126-1-1. In [25], a modified phase disposition pulse width modulation (MPDPWM) scheme is reported that successfully suppresses the grid leakage current for a five-level CHB. However, these modulation based leakage suppression methods are limited to five-level CHB and there is no solution given for a generalized *m*-level CHB.

In this paper, common-mode analysis for an *m*-level *n*-module (where n=2,3,4,… and m=2n+1) single-phase CHB inverter is established. Subsequently, this analysis is used to present a novel modulation method that can suppress leakage current for a nine-level CHB. A four-module CHB is used to offer higher accessibility to EV battery modules in a second life application. A simulation study and experimental results are provided demonstrating improvements over previous studies and verifies the effectiveness of the proposed solution.

II. Common-mode Analysis of CHB Inverter

Fig. 1 shows an *m*-level CHB utilizing hybrid sources such as PV arrays and batteries (Bat_n) at the same DC link. There are n H-bridge modules cascaded one after another, whose total output is tied to the grid, V_g, via two symmetrical filter inductors $L_{1,2}$. Each H-bridge is connected to a battery via a buck and boost stage to allow bi-directional energy transfer and has a PV panel connected directly across the DC link. Capacitances C_{j1} and C_{j2} (module index: j=1,2,…,n) are included in the circuit and represent the parasitic capacitance between PV terminals and ground. The values of these capacitances vary due to the panel surface area and also the weather conditions [30]. In Fig. 1, the negative terminal of each H-bridge and PV panel, termed "N_j", is taken as the reference point for that module, midpoints of each H-bridge leg are labelled "A_j" and "B_j" forming the output terminals for that module. The voltages imposed by switching actions between the output terminals and reference point of H-bridges are named as "V_{AN_j}" and "V_{BN_j}". Common-mode and differential-mode voltages for module j can be expressed in terms of the imposed voltages in equations (1) and (2), respectively.

$$V_{CM_j} = \frac{V_{AN_j} + V_{BN_j}}{2} \quad (1)$$

$$V_{DM_j} = V_{AN_j} - V_{BN_j} \quad (2)$$

Rearranging (1) and (2), leg voltages V_{AN_j} and V_{BN_j} can be expressed in terms of common-mode and differential-mode voltages:

$$V_{AN_j} = V_{CM_j} + \frac{V_{DM_j}}{2} \quad (3)$$

$$V_{BN_j} = V_{CM_j} - \frac{V_{DM_j}}{2} \quad (4)$$

By using (3) and (4), an equivalent circuit representing common-mode and differential-mode voltages can be derived. Fig. 2 shows the equivalent circuit for Fig. 1, and is similar to that as described in [23], where the ground point ($\stackrel{\perp}{=}$), grid voltage, filter inductances and grid leakage current are named as "O", "V_g", "L_1" and "L_2" and "i_{lg}" respectively.

From the perspective of the leakage current, the parasitic capacitances C_{j1} and C_{j2} seen in Fig. 1 are connected in parallel to the ground, therefore the equivalent parasitic capacitance of the j^{th} module is $C_{pvj} = C_{j1} \parallel C_{j2}$. If $C_{j1} = C_{j2}$, $C_{pvj} = 2C_{j1} = 2C_{j2}$, which is shown in Fig. 2. A fictious node connected between the common-mode and differential-mode voltages labelled as "X_j" is an imaginary point used for convenience of the circuit analysis. The output filter configuration is generally either asymmetrical ($L_1 \neq 0$, $L_2 = 0$) or symmetrical ($L_1 = L_2 \neq 0$) when the inverter is tied to the utility grid. These configurations have different leakage current characteristics, therefore have to be analyzed separately. The aim of the following sections is to derive an expression for the total grid leakage current "i_{lg}" in terms of the common-mode and differential-mode voltages. The resulting expression will be subsequently analyzed to determine the viability of leakage current suppression through the action of the common-mode or differential-mode voltages achieved by through appropriate modulation of each module.

A. Asymmetrical Filter Configuration

Assume inductor two is omitted, $L_1 \neq 0$, $L_2 = 0$. The derivation commences by determining the voltage across the parasitic capacitance (termed PCV) of the j^{th} module as shown below:

$$V_{N_jO} = 0.5V_{DM_j} - V_{CM_j} + \sum_{k=j+1}^{n} V_{DM_k} \quad (5)$$

Assuming all PV panels have identical parasitic capacitances, $C_{pv} = C_{pvj}$, the total grid leakage current i_{lg}, which is the summation of the individual leakage currents becomes

$$i_{lg} = C_{pv}\frac{d}{dt}\sum_{j=1}^{n} V_{N_jO} = C_{pv}\frac{dV_{N_TO}}{dt} \quad (6)$$

where V_{N_TO} is the sum of parasitic capacitance voltages (SPCV) and is defined as:

$$V_{N_TO} = -V_{CMT} + \sum_{j=1}^{n}(j - 0.5)\, V_{DM_j} \quad (7)$$

and $V_{CMT} = \sum_{j=1}^{n} V_{CM_j}$.

Grid leakage current in an asymmetrical circuit is defined in (6). It can be seen that if V_{N_TO} is not constant, leakage current will be present in the circuit. Moreover, the SPCV of an m-level inverter is determined by differential-mode and common-mode voltages of the modules, as expressed in (7). Although the contribution of each module common-mode voltage is equal (unity coefficient), the differential-mode voltages have increasing contributions and separating this effect poses difficulties for modulation based leakage cancelation approaches.

B. Symmetrical Filter Configuration

Starting with the aforementioned condition ($L_1 = L_2 \neq 0$), it is possible to apply Kirchhoff's law to equate current flowing the nodes X_j in Fig. 2 to obtain the following equation that applies to a n-module m-level CHB (where $f=1,2,\ldots,n-1$). Equation (8a-c) represent sum of currents for the 1st node, $j \in \{2, n-1\}$ nodes and the final node $j=n$, respectively. Equation (8d) provides the sum of parasitic capacitor voltages V_{N_TO}.

$$\frac{V_{X_1O} - V_{CM_1}}{Z_{PV_1}} + \frac{V_{X_1O} + 0.5V_{DM_1} - V_g}{Z_{L_1}} - i_1 = 0 \quad (8a)$$

$$\frac{V_{X_jO} - V_{CM_j}}{Z_{PV_j}} + i_{(j-1)} - i_j = 0 \; (j \in \{2, \mathrm{n}-1\}) \quad (8b)$$

$$\frac{V_{X_nO} - V_{CM_n}}{Z_{PV_n}} + \frac{V_{X_nO} - 0.5V_{DM_n}}{Z_{L_2}} + i_{(n-1)} = 0 \quad (8c)$$

$$\begin{gathered} V_{X_fO} - V_{X_{(f+1)}O} = 0.5(V_{DM_f} + V_{DM_{(f+1)}}) \\ V_{N_jO} = V_{X_jO} - V_{CM_j} \\ V_{N_TO} = \sum_{j=1}^{n} V_{N_jO} \end{gathered} \quad (8d)$$

The current flow to two adjacent modules are termed i_f, $i_{(j+1)},\ldots,i_{(n-1)}$, as illustrated by arrows i_1, i_2 & i_{n-1} in Fig. 2. In a symmetrical filter configuration, we can assume the impedance of filter inductors are equal so $Z_L = Z_{L_1} = Z_{L_2}$, where in this case $Z_L = sL_1 = sL_2$ with s being Laplace operator. One may also assume the impedance of the parasitic capacitances are $Z_{pvj} = 1/(sC_{pvj})$ in order to simplify the analysis. Using (8), the sum of parasitic capacitance voltage for an n-module CHB can be expressed as:

$$V_{N_TO} = \frac{Z_{pv}\left(-2V_{CMT} + nV_g + \sum_{j=1}^{n}(2j - n - 1)\, V_{DM_j}\right)}{2Z_{pv} + nZ_L} \quad (9)$$

From [30], the parasitic capacitance of a PV panel is taken as a maximum of ~150nF/kW. As the utility grid is dominated

by low frequency harmonics [25], it is therefore possible to say that $Z_{pv} \gg Z_L$. Thus, it is possible to further simplify (9) and express SPCV as

$$V_{N_TO} \cong -V_{CMT} + \frac{n}{2}V_g + \sum_{j=1}^{n}\left(\frac{2j-n-1}{2}\right)V_{DM_j} \quad (10)$$

Equation (10) reveals that if the number of modules is odd in a CHB (n=1,3,5…), the differential-mode voltage of middle H-bridge module does not contribute to SPCV, therefore it is not possible to keep the SPCV constant during a complete switching cycle. Conversely, there may be a solution when the number of modules is even (n=2,4,6…). For a four-module (n=4) CHB, the SPCV can be calculated using equation (10).

$$V_{N_TO} \cong -1.5V_{DM_1} - 0.5V_{DM_2} + 0.5V_{DM_3} + 1.5V_{DM_4} - V_{CMT} + 2V_g \quad (11)$$

Equation (11) provides an approximate expression for the SPCV for a four-module, nine-level CHB. It is influenced by common-mode and differential-mode voltages. Importantly, the differential-mode voltages in modules 1 and 4 and modules 2 and 3 have similar but opposing sign coefficients and so this provides a mechanism for reducing the leakage current through cancellation of the voltage terms.

C. Modulation Strategy and Leakage Current

The common-mode and differential-mode voltages are imposed by the unique switching states of the individual modules. Firstly, the switching function S_{jsw} for a nine-level CHB needs to be defined as:

$$S_{jk} = \begin{cases} 1, S_{jsw} \;\; ON \\ 0, S_{jsw} \;\; OFF \end{cases} \begin{pmatrix} \text{switch index,} \\ sw = 1,2,3,4 \end{pmatrix} \quad (12)$$

If the dc link voltage is same for all the modules, the imposed output voltages V_{AN_j} and V_{BN_j} for j^{th} module is as follows:

$$V_{AN_j} = V_{dc}S_{j3} \quad (13)$$

$$V_{BN_j} = V_{dc}S_{j1} \quad (14)$$

The common-mode and differential-mode voltages for the module can be calculated using (1) and (2). Since a single H-bridge has four valid unique switching states, a system containing four modules has 256 valid unique switching states. Using (7) and (9) with (13) and (14) it is possible to calculate the V_{N_TO} (SPCV) of each unique switching state. Unfortunately, there is no combination of switching states that has constant SPCV throughout the complete switching cycle for an asymmetrical filter configuration in an m-level CHB. This can be shown for the states, generated in a four module CHB by examining voltage levels between $+4V_{dc}$ and $-4V_{dc}$ in Table I. Having a varying SPCV during a switching cycle will cause leakage current in the system. Conversely, it is possible to keep SPCV at $-2V_{dc}$ while generating a nine-level output voltage waveform in a symmetrical filter configuration.

TABLE I
SWITCHING STATES OF LCRPWM
(LEAKAGE CURRENT REDUCTION PULSE WIDTH MODULATION)

Output Voltage	$S_{11}, S_{13}, S_{21}, S_{23}, S_{31}, S_{33}, S_{41}, S_{43}$	V_{N_TO} (Asym)	V_{N_TO} (Sym)
$+4V_{dc}$	10101010	$6V_{dc}$	$-2V_{dc}$
$+3V_{dc}$	10100010	$4V_{dc}$	$-2V_{dc}$
$+2V_{dc}$	10110010	$2V_{dc}$	$-2V_{dc}$
$+1V_{dc}$	11111000	0	$-2V_{dc}$
0	11110000	$-2V_{dc}$	$-2V_{dc}$
0	00001111	$-2V_{dc}$	$-2V_{dc}$
$-1V_{dc}$	00011111	$-4V_{dc}$	$-2V_{dc}$
$-2V_{dc}$	01001101	$-6V_{dc}$	$-2V_{dc}$
$-3V_{dc}$	01000101	$-8V_{dc}$	$-2V_{dc}$
$-4V_{dc}$	01010101	$-10V_{dc}$	$-2V_{dc}$

If the inverter is modulated using one of the combinations of selected switching states, SPCV would be constant and the grid leakage current would be suppressed. Examination of phase disposition pulse width modulation (PDPWM) and phase shifted pulse width modulation (PSPWM) show these techniques lead to switching combinations that generate varying SPCV, leading to system leakage currents through parasitic capacitances to the ground.

III. LEAKAGE CURRENT REDUCTION PULSE WIDTH MODULATION STRATEGY

Traditional PDPWM and PSPWM techniques can be implemented easily and do not require significant computational power. As discussed in Section II-C, these modulation strategies cannot produce a stable SPCV throughout a complete switching cycle and, therefore, are unable to suppress leakage current. In order to overcome this issue, a leakage current reduction pulse width modulation (LCRPWM) scheme is proposed. There exists more than one switching state combination available for each of $+3V_{dc}$, $+2V_{dc}$, $+1V_{dc}$ 0, $-1V_{dc}$, $-2V_{dc}$, $-3V_{dc}$ output voltage levels, which generate $-2V_{dc}$ SPCV. The switching states for LCRPWM, seen in right hand column of Table I, is selected by minimizing the number of switching events to reduce switching losses. This modulation method requires only four carrier waveforms that are in phase, unlike to PDPWM and PSPWM techniques, which requires eight carriers in order to generate gate signals for switches.

The triangular carrier waveforms V_{c1-4} are in phase and all have an amplitude of 0.25, which can be seen in Fig. 3. These carriers are defined as $0 \le V_{c1} \le 0.25 \le V_{c2}$ $0.5 \le V_{c3}$ $0.75 \le V_{c4} \le 1$. Several new grid reference signals are introduced $V_{r1\text{-}7}$ which are compared with the different carrier waveforms to generate the switching functions S_{jk} for each switching device. The reference waveform is a unity amplitude sinewave operating at the grid frequency and is defined as:

$$V_{ref} = \sin(\omega t) \quad (15)$$

The sign (signum) of the reference waveform is defined to provide a Boolean signal:

$$\text{sgn}(V_{ref}) = \begin{cases} 1 & V_{ref} > 0 \\ 0 & V_{ref} \le 0 \end{cases} \quad (16)$$

The helper reference waveforms are defined as:

$$
\begin{aligned}
V_{r1} &= \begin{cases} V_{ref} & V_{ref} > 0 \\ V_{ref} + 1 & V_{ref} \le 0 \end{cases} \\
V_{r2} &= \begin{cases} V_{ref} & V_{ref} > 0 \\ 1 & V_{ref} \le 0 \end{cases} \\
V_{r3} &= \begin{cases} |V_{ref}| & -0.25 \le V_{ref} < 0 \\ 0 & \text{otherwise} \end{cases} \\
V_{r4} &= -V_{ref} \times \overline{\text{sgn}(V_{ref})} \\
V_{r5} &= \begin{cases} 1 & V_{ref} > 0 \\ |V_{ref}| & V_{ref} \le 0 \end{cases} \\
V_{r6} &= V_{ref} \times \text{sgn}(V_{ref}) \\
V_{r7} &= \begin{cases} V_{ref} & 0 \le V_{ref} < 0.25 \\ 0 & \text{otherwise} \end{cases}
\end{aligned}
\tag{17}
$$

where the overhead bar symbol denotes a logical 'not' operator.

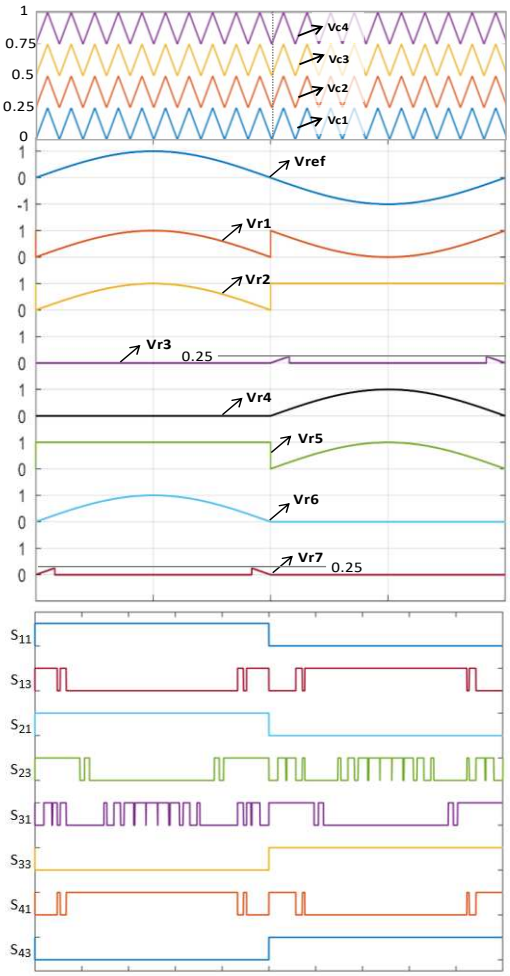

Fig. 3. Switching properties of LCRPWM technique.

The helper reference signals are generated by using switching states determined in Table 1. The switches in the same leg of the H-bridge operates in complementary manner (i.e. S_{j1} and S_{j2}). Gate pulses for each switching device can be calculated by following equations for LCRPWM.

$$
S_{11} = S_{21} = S_{34} = S_{44} = \overline{S_{12}} = \overline{S_{22}} = \overline{S_{33}} = \overline{S_{43}} = \text{sgn}(V_{ref}) \tag{18a}
$$

$$
\begin{aligned}
S_{13} = S_{42} = \overline{S_{14}} = \overline{S_{41}} = {} & \text{sgn}(V_{ref}) \cdot [V_{r1} < V_{c2}] + \\
& \overline{\text{sgn}(V_{ref})} \cdot [V_{r1} < V_{c3}]
\end{aligned}
\tag{18b}
$$

$$
\begin{aligned}
S_{23} = \overline{S_{24}} = {} & \text{sgn}(V_{ref}) \cdot [V_{r2} < V_{c3}] + \overline{\text{sgn}(V_{ref})} \cdot [V_{r3} > V_{c1}] \\
& \cdot [0 < V_{r4} < 0.25] + \overline{\text{sgn}(V_{ref})} \\
& \cdot [V_{r1} > V_{c3}] \cdot [0.25 < |V_{ref}| < 0.75] \\
& + \overline{\text{sgn}(V_{ref})} \cdot [V_{r4} > V_{c4}] \cdot [0.75 < V_{r4} < 1]
\end{aligned}
\tag{18c}
$$

$$
\begin{aligned}
S_{31} = \overline{S_{32}} = {} & \text{sgn}(V_{ref}) \cdot [V_{r7} > V_{c1}] \cdot [0 < V_{r7} < 0.25] \\
& + \text{sgn}(V_{ref}) \cdot [V_{r1} < V_{c2}] \\
& \cdot [0.25 < V_{ref} < 0.75] + \text{sgn}(V_{ref}) \\
& \cdot [V_{r6} > V_{c4}] \cdot [0.75 < V_{ref} < 1] \\
& + \overline{\text{sgn}(V_{ref})} \cdot [V_{r5} < V_{c3}]
\end{aligned}
\tag{18d}
$$

where the inequalities in the square brackets are equivalent to comparisons (i.e. if statements), the '+' symbols denote logical 'or' operators and the '·' symbols represent logical 'and' operators.

From Table I, there are two switching states for a zero voltage output. During zero crossing of reference wave, these states switch from one to the other dependent on polarity of the reference. There are ten unique switching states that generate nine voltage levels for the proposed leakage current reduction operation of the CHB inverter. The relevant gate pulses for individual switches can be seen in Fig. 3.

IV. Simulation Study

The proposed modulation technique was implemented in MATLAB/Simulink to demonstrate the effectiveness of LCRPWM on suppressing the parasitic leakage current. Traditional PSPWM and PDPWM techniques are also implemented to compare the results.

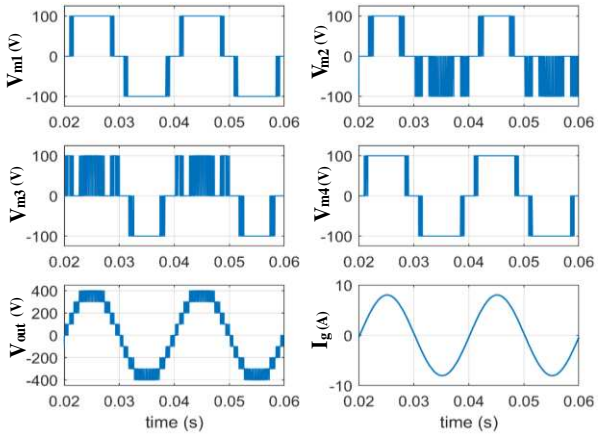

Fig. 4. LCRPWM simulation results of modules 1-4 output voltage waveforms, total output voltage and the grid current.

Some of the parameters of simulation include: DC link voltage (V_j) of 115V at each H-bridge module, a parasitic capacitance (C_{pvj}) of 100nF, grid voltage (V_g) at 240V and 50Hz, a grid filter of 3.51mH and 9μF in an LCL configuration (which has a resonant frequency < half of switching frequency) and finally a switching frequency of 4 kHz. Fig. 4 illustrates the individual module output voltages V_{m1}, V_{m2}, V_{m3} and V_{m4}, total output voltage V_{out} and finally the grid current I_g of LCRPWM technique.

Each module generates a three-level voltage waveform, creating a total of nine-level voltage waveform at the output.

After the filtering, the grid current waveform is purely sinusoidal and is of high quality, having 1.69% THD. It is clear that LCRPWM method can be applied to a nine-level CHB and demonstrates an acceptable operation quality.

In Fig. 5, PCV waveforms for individual modules (mod 1-4) of CHB, the SPCV, the leakage current of module 1 (I_{lm1}), and the parasitic grid leakage current for PSPWM, PDPWM and the proposed LCRPWM, are illustrated in parts a-c respectively. The PCV at each module contains pulsating voltages at switching frequency of the inverter. As a result of this, these noisy waveforms are reflected to the SPCV in both PSPWM and PDPWM.

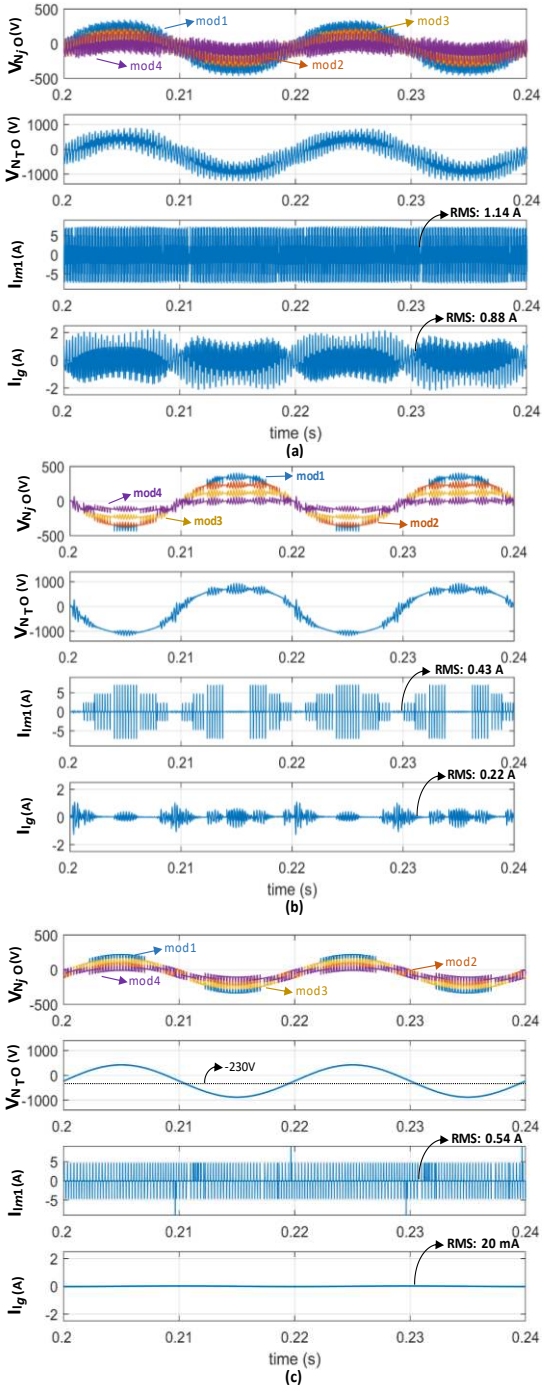

Fig. 5. Simulation results of PCV of modules 1-4, SPCV, leakage current of module 1, and the grid leakage current. (a) PSPWM. (b) PDPWM, (c) LCRPWM

As stated in Section-I, the allowed leakage current is maximum 30mA however PSPWM and PDPWM results in a root-mean-square (RMS) leakage current of 0.88A and 0.22A respectively, both values are above the acceptable limit. LCRPWM is illustrated in Fig. 5(c), and although its PCV waveform also contains pulsating voltage, the SPCV waveform has an RMS leakage current of 20mA that conforms to the regulation. The SPCV is sinusoidal and has an offset of -230V as expected. The simulation study is carried out with highest possible grid voltage of 240V_{rms} at distribution level as in [25] it is reported that higher grid voltages cause higher leakage current. Following this, the worst case condition for leakage current is simulated.

V. Experimental Validation

The experimental prototype shown in Fig. 6 was constructed to validate the aforementioned modulation techniques. The circuitry has four identical H-bridge power boards that were constructed using FNB34060T power modules from ON Semiconductor that can withstand up to 40A collector-emitter current, and auxiliary circuitry for voltage and current measurement. The master controller is an NI cRIO-9063 with an FPGA for the implementation of modulation methodologies and closed loop PI current controller. Isolated DC sources are achieved by using a combination of step-down transformer, bridge rectifiers and smoothing DC link capacitors. DC link capacitors selected to keep peak-to-peak DC link voltage ripple < 6%. The power rating for the system is 3.3 kVA, which is the total VA rating of the step-down transformers. The parameters of the inverter are illustrated in Table II.

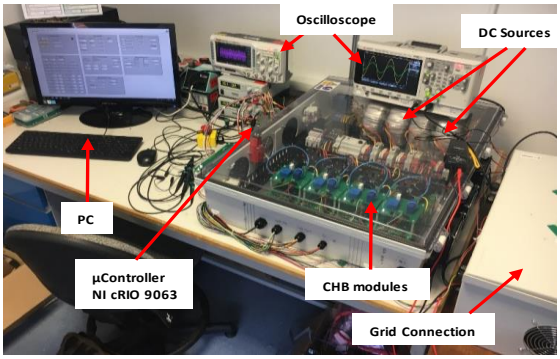

Fig. 6. Four-module nine-level CHB laboratory prototype.

TABLE II
CHB Inverter Parameters

Parameters	Values
DC voltage	115V/module
Grid voltage	240V_{AC} at 50 Hz
Power rating	3.3 kW
Switching frequency	4 kHz
DC-link Capacitance	6.6mF/module
Inverter side inductance	2x2.34 mH
Grid side inductance	2x1.17 mH
Filter capacitance	9 µF
Parasitic Capacitance	100 nF/module

Experimental results include comparisons between PSPWM, PDPWM and the proposed LCRPWM consisting of the unfiltered output voltage V_{out}, grid current I_g, grid voltage V_g, FFT analysis (THD) of grid current, leakage current of modules 1-4 I_{lm1}, I_{lm2}, I_{lm3}, and I_{lm4}, and the grid leakage current I_{lg}, which can be seen in Fig. 7-9.

Figures 7-9 show experimental results for PSPWM, PDPWM and LCRPWM respectively. Subplot (a) illustrate the nine-level unfiltered voltage steps and the sinusoidal grid voltage and currents. The THD of PSPWM is 2.26%, THD of PDPWM is 2.02%, and the THD of LCRPWM is 1.72% as shown in subplots (b). The THD of PSPWM is highest as the (S)PCV waveforms undergo the most variation and this causes highest amount of leakage current, which degrades grid current. All modulation methods create a grid current THD that conform to the IEEE 1547 standard. Moreover, subplot (c) of Fig. 7-9 provides details about the leakage current of modules 1-4 and the grid leakage current for all studied modulation methods. It is interesting to note that for PSPWM the envelope of the module leakage current and the respective RMS values varies considerably between each module. For PDPWM the modules have more consistent RMS values but, again, the waveform envelopes vary. LCRPWM provides very similar waveform envelopes and although the RMS module currents are higher, their combination has a nulling effect. The measured values for grid leakage current in PSPWM, PDPWM and LCRPWM are $893mA_{rms}$, $213mA_{rms}$ and $24mA_{rms}$ respectively. It is verified that the proposed LCRPWM method can suppress the leakage current flowing through the parasitic capacitances, also conforming to VDE-0126-1-1.

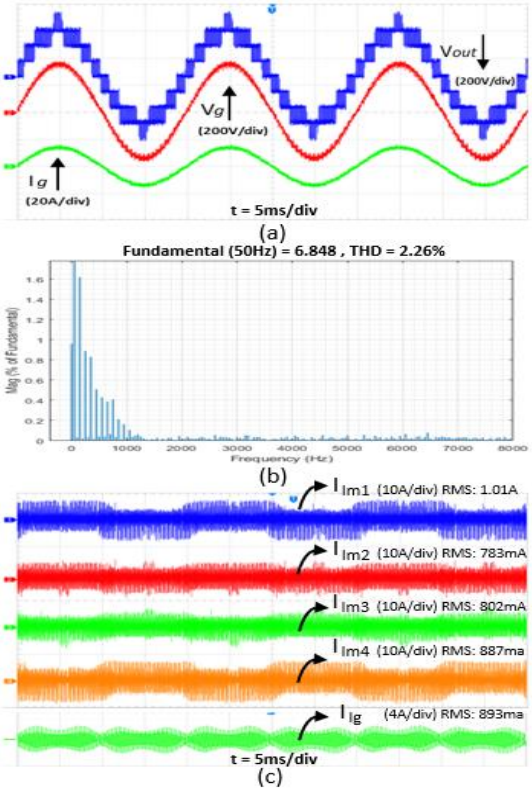

Fig. 7. Experimental results of the PSPWM. (a) Unfiltered output voltage, grid voltage, and the grid current; (b) FFT of the grid current; and (c) leakage current of modules 1-4, and the grid leakage current

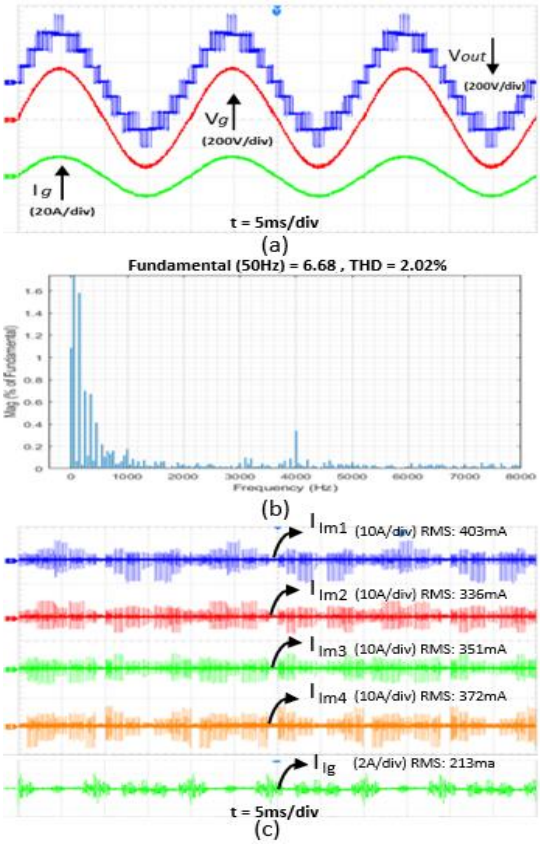

Fig. 8. Experimental results of the PDPWM. (a) Unfiltered output voltage, grid voltage, and the grid current; (b) FFT of the grid current; and (c) leakage current of modules 1-4, and the grid leakage current

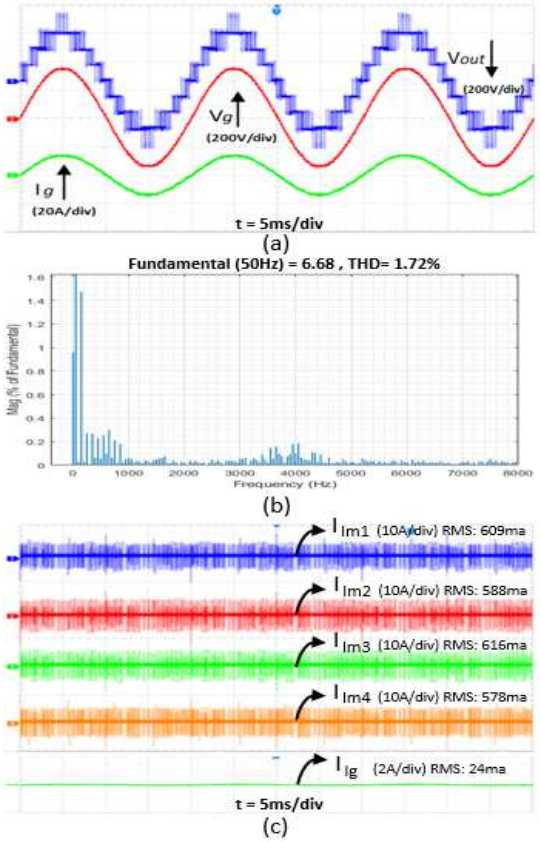

Fig. 9. Experimental results of the LCRPWM. (a) Unfiltered output voltage, grid voltage, and the grid current; (b) FFT of the grid current; and (c) leakage current of modules 1-4, and the grid leakage current

This enables one to address the leakage current problem without adding to cost, weight and size of a nine-level grid-tie CHB. The individual module leakage current values are higher than grid leakage current for PDPWM and LCRPWM. In PSPWM, only module 1 has higher module leakage current compared with the grid leakage current.

Experimental results for RMS grid leakage current with respect to switching frequency and modulation index (m_a) are illustrated in Fig. 10 for PSPWM and PDPWM respectively. It should be noted the results are limited to modulation indices > 0.75 because if m_a goes below this value, one module becomes idle and does not contribute to power sharing in PDPWM.

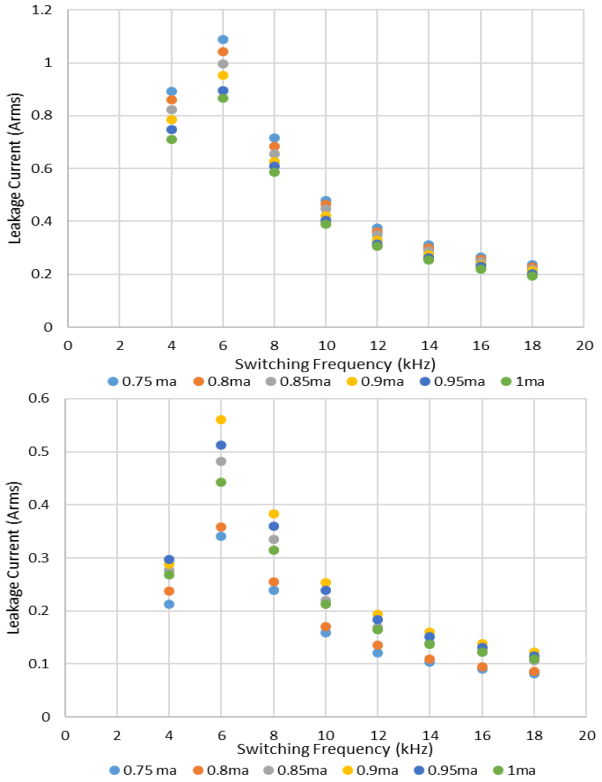

Fig. 10. Experimental results of grid leakage current with respect to different modulation indexes and switching frequencies, (a) PSPWM, (b) PDPWM.

In Fig. 10(a), it can be seen that both PSPWM and PDPWM tend to have higher grid leakage current with reduced switching frequency. This may be the effect of output filter as its filtering capability increases at higher frequencies. It should be noted that the parasitic capacitances and inductances create a resonant circuit and this should be borne in mind when selecting the switching frequency. In Fig. 10(a), it is obvious that PSPWM performs better when modulation index is closer to unity. In Fig. 10(b), PDPWM has highest grid leakage values when operated at 0.9 modulation index. 0.75-0.8 modulation index range provides lower grid leakage current in PDPWM, as the time of maximum and minimum voltage levels ($+4V_{dc}$ and $-4V_{dc}$) during a fundamental switching cycle become shorter. Furthermore, LCRPWM is not affected by switching frequency and/or modulation index variations, making it effective in suppressing grid leakage current over different operating points. PSPWM and PDPWM may conform to VDE-0126-1-1 standard at higher frequencies but this may be disadvantageous as operating conditions needs to be predefined and switching losses becomes significant in a cascaded H-bridge. Additionally, it may be possible to effectively suppress leakage current in an unbalanced DC link voltage scenario and this is the subject of ongoing work.

Finally, the experimental results are in line with simulation study and shows good agreement with the aforementioned theory in Section-II.

VI. Conclusion

In this paper, a common-mode equivalent circuit is provided for an *m*-level CHB inverter in order to analyze the leakage current problem. The occurrence of leakage current in an asymmetrical and symmetrical output filter configuration is studied. It is reported that grid leakage current cannot be minimized for an asymmetrical configuration, and also symmetrical configuration with odd module numbers of solely on modulation methods as SPCV is not constant during a fundamental switching cycle. In a symmetrical filter configuration with an even number of H-bridges, although PSPWM and PDPWM methods cannot reduce grid leakage current to allowed limits, the proposed LCRPWM technique can suppress it for a nine-level CHB. Simulation and experimental studies validate that grid leakage current can be minimized.

Despite suppressing grid leakage current using the LCRPWM technique, inter-module leakage currents are still present and can be seen in both simulation and experimental analysis. This raises some safety concerns and forms the basis of the ongoing work.

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