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THE USE OF HYBRID MODULAR MULTILEVEL CASCADED CONVERTER FOR UNBALANCED VOLTAGE CONDITION

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Abstract

This paper presents a control scheme for the hybrid MMCC using the 5-level flying capacitor converter as sub-module under grid unbalanced voltage condition. The hybrid MMCC is compared with the single star-connected MMCC under voltage sag condition to determine its superiority, in addition to its lower dc capacitor and power semiconductor switch count. The simulation results are provided to validate the hybrid MMCC control scheme and its comparison with the star connected MMCC.

1 Introduction

Single star bridge converter modular multilevel cascaded converter (SSBC-MMCC) using either two-level H-bridge or five-level Flying capacitor converter [1] as sub-modules have been applied for Static Synchronous Compensator (STATCOM) and other grid applications [2]-[7]. With the tremendous advantages of modularity, scalability and low switching losses provided by SSBC-MMCC, the dc capacitor voltage balancing of its sub-modules is a key challenge [2]. Especially under unbalance grid voltage and load condition. This has been addressed by injecting zero-sequence voltage in redistributing the unbalance average active power flowing in the MMCC phase clusters [4]-[7].

The implication of using this MMCC as STATCOM for grid unbalanced condition is that the voltage rating requirement has a direct relationship with the level of either voltage unbalance or current imbalance. Thus more power semiconductor devices are required resulting from more sub-modules serially connected to meet the desired voltage requirements for proper dc capacitor balancing. This further increases the cost of the converter by requiring more gate drivers. This limitation can be addressed by connecting single-phase sub-module converters or cells with a three-phase two-level converter. This hybrid MMCC lowers the semiconductor device and sub-module capacitor count. The topology of hybrid MMCC using three-level H-bridge cell as sub-module has been investigated in [8]-[10].The hybrid MMCC when applied for grid applications, has used floating capacitors as dcsources for HVDC transmission [9] and rectification [11] where the capacitors are regulated using *PI* controllers and hysteresis control respectively. Authors in [9], [11] has applied this for balance grid voltage STATCOM application.

In this paper, a control scheme is presented for the hybrid MMCC operating under both balanced and unbalanced grid voltage condition. The hybrid MMCC considered comprises of the five-level FC converter as sub-module and three-phase two-level converter. The control strategy begins with a power flow analysis. The dc capacitor voltage control is implemented based on [2] comprising of overall, inter-cluster and intra-cluster dc capacitor voltage control with the inclusion of a new control strategy known as the hybrid controller. The unbalance active power flowing in the converter phase clusters is addressed using the zero-sequence voltage injection technique. The hybrid MMCC is also compared against the SSBC under unbalanced grid voltage fault ride through conditions. This hybrid MMCC STATCOM is validated using MATLAB SIMULINK.

2. System Configuration

The system configuration of the hybrid MMCC is shown in Fig. 1, this consist of $(k-1)$sub-module cells per phase and a two-level converter. The sub-module dc capacitor voltages are represented as v_{dcmn}, $m = a,b,c$ and $n = 1,\dots,k-1$ and the two-level converter is v_{dcK}, where the dc capacitor voltage ratio of the sub-module to the two-level converter is $1:Q$ thus, $v_{dcK} = Qv_{dcmn}$. The grid voltages v_a, v_b, v_c and phase currents i_a, i_b, i_c are represented in dq transformation for both positive and negative sequence components as;

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{2/3}\,[T_{\alpha\beta}]\left([T_{dq}^{+}]\begin{bmatrix} V_d^{+} \\ V_q^{+} \end{bmatrix} + [T_{dq}^{-}]\begin{bmatrix} V_d^{-} \\ V_q^{-} \end{bmatrix}\right) \quad (1)$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{2/3}\,[T_{\alpha\beta}]\left([T_{dq}^{+}]\begin{bmatrix} I_d^{+} \\ I_q^{+} \end{bmatrix} + [T_{dq}^{-}]\begin{bmatrix} \mathrm{I}_d^{-} \\ I_q^{-} \end{bmatrix}\right) \quad (2)$$

Where $[T_{\alpha\beta}] = \begin{bmatrix} 1 & 0 \\ -1/2 & -\sqrt{3}/2 \\ -1/2 & \sqrt{3}/2 \end{bmatrix}$, $[T_{dq}^{+}] = \begin{bmatrix} sin\omega t & -cos\omega t \\ cos\omega t & sin\omega t \end{bmatrix}$ and $[T_{dq}^{-}] = \begin{bmatrix} sin\omega t & cos\omega t \\ -cos\omega t & sin\omega t \end{bmatrix}$.

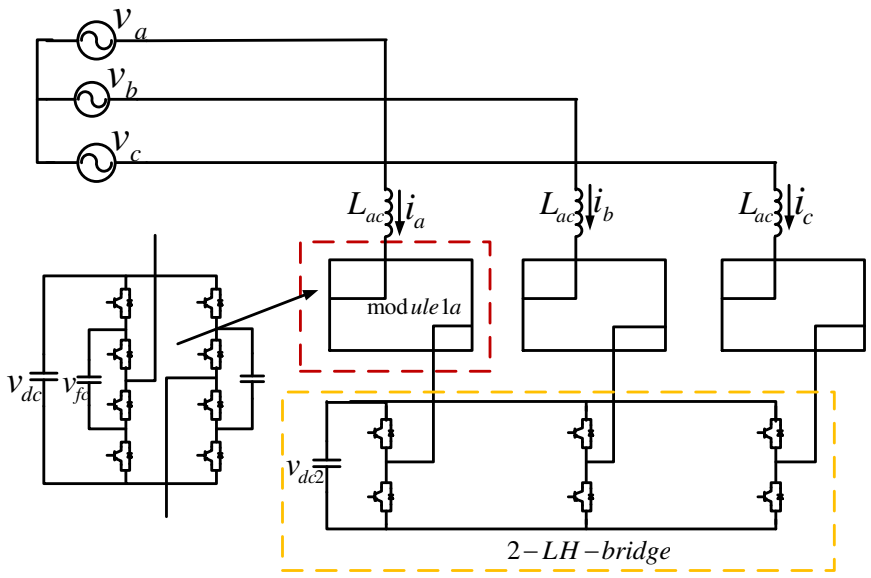

Fig.1: MMCC-Hybrid STATCOM system

Where + and – represent the positive and negative sequence, *d* and *q* represent active and reactive axis respectively and ωt is the grid angular frequency.

3. Power Flow Investigation

This is important for the implementation of the control strategy of the hybrid MMCC. This power flow investigation is solely dependent on (1), (2) and the zero-sequence voltage for the sub-modules v_S^0 and two-level converterv_2^0, which are given as;

$v_S^0 = V_S^0 \sin(\omega t + \psi_S^0)$ (3a)

$v_2^0 = V_2^0 \sin(\omega t + \psi_2^0)$ (3b)

Where V_S^0, V_2^0, ψ_S^0, ψ_2^0 are the magnitude and phase angles of the zero-sequence voltage of the sub-modules and two-level converter. The voltage references of the hybrid MMCC are shared between the sub-modules and two-level converters depending on their dc capacitor voltage utilizations of v_{dcmn} and $0.5v_{dcK}$ respectively.

The cluster power flow in the sub-modules P_{Sm} and two-level converter P_{2m} are given as;

$P_{Sm} = P_{Sm(1)} + \cdots + P_{Sm(k-1)} = {}^{P_S}/_3 + P_{CSm}$ (4a)

$P_{2m} = P_{2m(1)} + \cdots + P_{2m(k-1)} = {}^{P_2}/_3 + P_{C2m}$ (4b)

Where $P_S = P_{Sa} + P_{Sb} + P_{Sc}$, $P_{CSm} = P_{Sm} - {}^{P_S}/_3$ and $P_2 = P_{2a} + P_{2b} + P_{2c}$, $P_{C2m} = P_{2m} - {}^{P_2}/_3$. Thus for the sub-module clusters, their phase powerP_{Sm}, consist of the balance overall power(${}^{P_S}/_3$), the unbalance active phase power (P_{CSm}) likewise for the two-level converter, the phase powerP_{2m}, consist of the balance overall power (${}^{P_2}/_3$) and the unbalance active phase power(P_{C2m}). The unbalanced phase power in a two-level converter is zero because of the power flow is from one capacitor. Thus the zero-sequence voltage of the two-level converter is zero.

4. Hybrid MMCC Control Scheme

The hybrid MMCC control scheme is shown in Fig. 2. This comprises of the current controller and dc capacitor voltage controller. The dc capacitor voltage controller consists of the overall, cluster, hybrid and individual dc capacitor voltage control.

4.1 Overall control

This controller determines the reference currents needed for the hybrid MMCC current control. These reference currents are given based on balanced positive sequence current (BPSC) as [12];

$I_d^{+*} = \left(k_p + {}^{k_i}/_s\right)(V_{dc}^* - V_{dc})$ (5a)

$I_q^{+*} = {}^{-2V_d^+ Q_{ref}}/_{3\left((V_d^+)^2 + \left(V_q^+\right)^2\right)}$ (5b)

$I_d^{-*} = I_q^{-*} = 0$ (5c)

$V_{dc} = \left[\frac{\sum_{n=1}^{k-1}(V_{dcan}+V_{dcbn}+V_{dccn})}{3(k-1)} + {}^{V_{dcN}}/_Q\right]$ (5d)

I_d^{+*}compensates the total power losses of the hybrid MMCC, which is produced by using a PI regulator controlling the error between the dc capacitor voltage reference (V_{dc}^*) and the average dc capacitor voltage (V_{dc}). Fig. 3 shows the block diagram of the overall dc voltage control. I_q^{+*} Controls the required reactive power Q_{ref}. $I_d^{-*}$and I_q^{-*} are regulated to be zero. These current references are supplied to the current controller to generate the reference voltages (v_m) which are divided between the sub-modules (v_{Sm}) and two-level converters (v_{2m}).

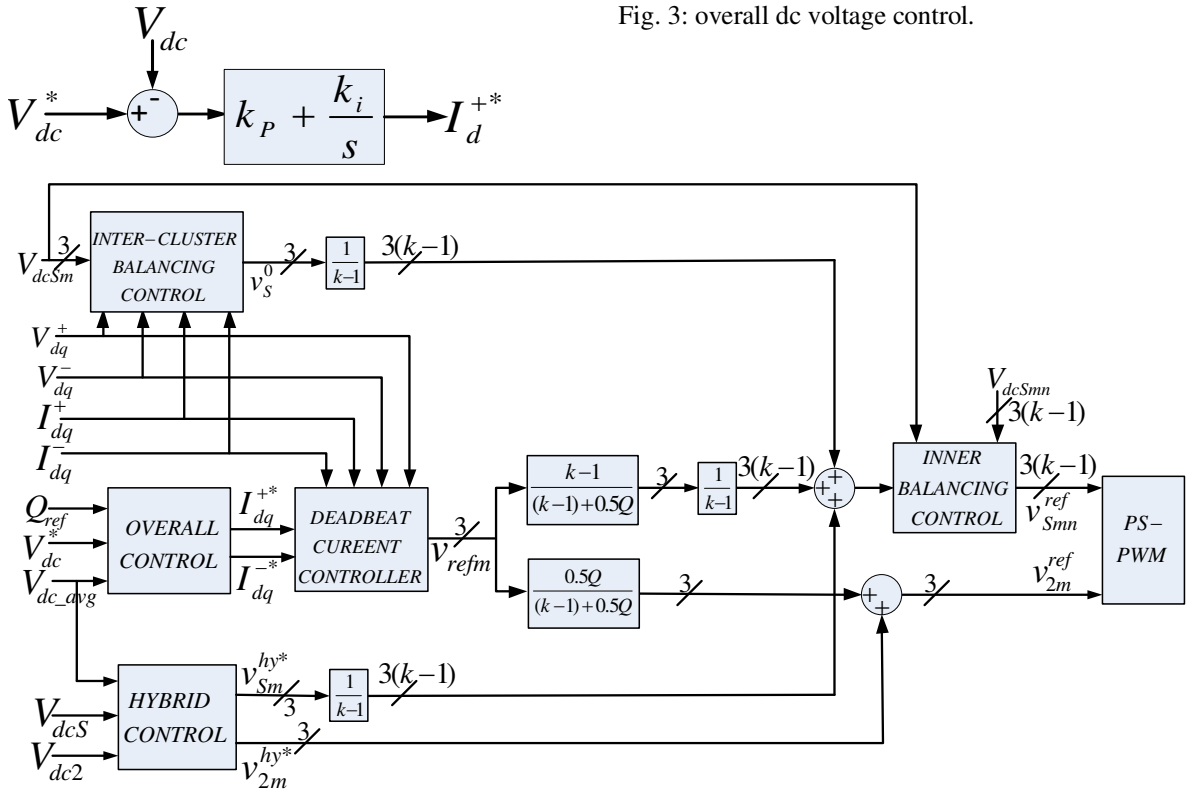

Fig. 3: overall dc voltage control.

Fig.4: MMCC-Hybrid STATCOM control scheme

4.2Hybrid controller

This is used to control the active power between the sub-modules and two-level converter for proper balancing of their dc capacitor voltages. The sub-modules and two-level converter hybrid controller reference voltages are given as;

$$v_{Sm}^{hy*} = \left(k_p^{hy*} + {k_i^{hy*}}/{s}\right)(V_{dc} - V_{dcS}).\, i_m \quad (6a)$$

$$v_{2m}^{hy*} = \left(k_p^{hy*} + {k_i^{hy*}}/{s}\right)(V_{dc} - V_{dc2}).\, i_m \quad (6b)$$

$$V_{dcS} = {\sum_{n=1}^{k-1}(V_{dcan} + V_{dcbn} + V_{dccn})}/{3(k-1)} \quad (6c)$$

$$V_{dc2} = {V_{dcN}}/{Q} \quad (6d)$$

PI regulators are applied to the error between the average dc capacitor voltage (V_{dc}) and the average dc capacitor voltage of the sub-modules (V_{dcS}), two-level converter (V_{dc2}) and multiplied by phase currents (i_m) to provide (v_{Sm}^{hy*}) and (v_{2m}^{hy*}) respectively.

4.3Cluster power controller

The unbalance active power flow is addressed by the zero-sequence voltage. From the hybrid MMCC power investigation, unbalanced active power flow only occurs for sub-modules, not for the two-level converter. Thus, only the sub-modules of the hybrid MMCC require inter-cluster dc capacitor voltage control. Therefore, only the zero-sequence voltage of the sub-modules are determined. The zero-sequence voltage for the sub-modules is derived based on [2] below.

The zero-sequence power is expressed as;

$$P_{Csm}^{0} = P_{Csm} - P_{Csm}^{+-} = P_{Csm}^{FB} - P_{Csm}^{FF} \quad (7)$$

whereP_{Csm} is known as the unbalanced phase active power in the sub-modules are also defined as the feedback terms (P_{Csm}^{FB}) while P_{Csm}^{+-} comprises positive and negative sequence voltages are referred to as the feed-forward terms (P_{Csm}^{FF}). Both P_{Csm}^{FB} and P_{Csm}^{FF} are given as;

$$P_{Csm}^{FB} = \left(k_p^{C} + {k_i^{C}}/{s}\right)(V_{dcS} - V_{dcSm}) \quad (8a)$$

$$P_{Csa}^{FF} = \frac{0.5(k-1)}{(k-1)+0.5Q}\left(V_d^- I_d^+ - V_q^- I_q^+ + V_d^+ I_d^- - V_q^+ I_q^-\right) \quad (8b)$$

$$P_{Csb}^{FF} = \frac{0.25(k-1)}{(k-1)+0.5Q}\begin{pmatrix}\left(-V_d^- + \sqrt{3}V_q^-\right)I_d^+ + \left(\sqrt{3}V_d^- + V_q^-\right)I_q^+ \\ +\left(-V_d^+ + \sqrt{3}V_q^+\right)I_d^- + \left(\sqrt{3}V_d^+ + V_q^+\right)I_q^-\end{pmatrix} \quad (8c)$$

$$P_{Csc}^{FF} = \frac{0.25(k-1)}{(k-1)+0.5Q}\begin{pmatrix}\left(-V_d^- - \sqrt{3}V_q^-\right)I_d^+ + \left(-\sqrt{3}V_d^- + V_q^-\right)I_q^+ \\ +\left(-V_d^+ - \sqrt{3}V_q^+\right)I_d^- + \left(-\sqrt{3}V_d^+ + V_q^+\right)I_q^-\end{pmatrix} \quad (8d)$$

$$V_{dcSm} = {\sum_{n=1}^{k-1} V_{dcmn}}/{k-1} \quad (8e)$$

Fig. 4 shows the inter-cluster power balancing controller. $P_{Csm}^{0}$are transformed into $\alpha - \beta$ to determine the zero-sequence voltage as;

$$\begin{bmatrix} V_S^0 sin\psi_S^0 \\ V_S^0 cos\psi_S^0 \end{bmatrix} = \frac{1}{(I_d^+)^2 + (I_q^+)^2 - (I_d^-)^2 - (I_q^-)^2}\begin{bmatrix} I_d^+ - I_d^- & I_q^+ - I_q^- \\ -I_q^+ - I_q^- & I_d^+ + I_d^- \end{bmatrix}\begin{bmatrix} P_{CS\alpha}^0 \\ P_{CS\beta}^0 \end{bmatrix} \quad (9)$$

4.4Intra-cluster controller

This is implemented to regulate the active power across each sub-module across a particular phase to actualize dc capacitor voltage balancing of each sub-module at that phase cluster. The intra-cluster control for each sub-module at a particular phase (v_{Smn}^{in}) is;

$$v_{Smn}^{in} = \left(k_p^{in} + {k_i^{in}}/{s}\right)(V_{dcSm} - V_{dcmn}).\, i_m \quad (10)$$

$v_{Smn}^{in}$is generated by passing the difference between the average dc capacitor voltage of the sub-modules in a particular phase cluster and dc capacitor voltage of each sub-module in a similar phase through a *PI* regulator. The output of the *PI* regulator is multiplied by the phase current i_m in other to keep both the voltage command and current in phase. In adding the command references from all the four controllers, the voltage references for the sub-modules (v_{Smn}^{ref}) and two-level converter (v_{2m}^{ref}) is expressed as;

$$v_{Smn}^{ref} = {v_{Sm}}/{k-1} + {v_{Sm}^{hy*}}/{k-1} + {v_S^0}/{k-1} + v_{Smn}^{in} \quad (11a)$$

$$v_{2m}^{ref} = v_{2m} + v_{2m}^{hy*} \quad (11b)$$

Both voltage references are modulated using the phase-shifted PWM (PS-PWM) [1] to generate the gate pulses for both sub-modules and two-level converter.

5. Power Flow Investigation Comparison between Hybrid and Single Star Connected MMCC under Unbalance Voltage Condition

To compare between hybrid and SSBC MMCC, the zero-sequence voltage magnitude is used as the benchmark. Assuming balance positive sequence currents are injected into the grid, the zero-sequence voltage magnitude for the hybrid (v_S^0) and SSBC [1] (v_0) is calculated using the feed-forward terms. The feed-forward terms of the hybrid and SSBC MMCC are related by;

$$P_{Csm}^{+-} = \frac{(k-1)}{(k-1)+0.5Q} P_{Cm}^{+-} \quad (12)$$

From equation (12), it is seen that as the dc capacitor voltage rating of the two-level converter *Q*increases, the zero-sequence voltage required to achieve inter-cluster power balancing of the sub-modules dc capacitor decreases. Also, for a given sub-module dc capacitor voltage rating, increase in the number of sub-modules for a fixed rating of a 2-level converter dc capacitor voltage, the required zero-sequence voltage also increases.

This implies two things;

1. The zero-sequence voltage v_S^0 of the hybrid MMCC reduces as Q increases.
2. The zero-sequence voltage v_S^0 of the hybrid MMCC increases as the number of sub-modules increases.
3. The zero-sequence voltage v_S^0 of the hybrid MMCC is less than the zero-sequence voltage v_0 of the SSBC MMCC under unbalanced grid conditions.

6. Simulation Results

To validate the control strategy for the hybrid MMCC, the system configuration shown in Fig. 1 is simulated in MATLAB SIMULINK. The number of sub-modules per phase are $k = 1$ and dc voltage ratio$Q = 2$. The system parameters are shown in Table 1. A Phase *a* 30% voltage sag is implemented as the unbalanced voltage condition. Also, the grid is supported by the injection of $Q_{ref} = -50KVar$ reactive power.

Table 1: System Parameters

Quantity	Symbol	Value
Grid voltage	v	1250V
Grid frequency	f	50Hz
Ac filter inductor	L_{ac}	6mH
Sub-module dc voltage	V_{dc}	800V
Inner capacitor voltage	V_{fc}	400V
2L H-bridge dc voltage	$2V_{dc}$	1600V
dc link capacitor (sub-module)	C_{dc}	1120µF
Inner capacitor	$0.5C_{dc}$	560 µF
dc link capacitor (2L H-bridge)	$2C_{dc}$	2240µF
Carrier frequency (sub-module)	f_s	750Hz
Carrier frequency (2L H-bridge)	$4f_s$	3000Hz

Fig. 5 shows the waveforms of the hybrid MMCC STATCOM, Fig. 5(a) shows the hybrid STATCOM phase currents injected into the grid. Fig. 5(b) shows the sub-modules and two-level converter dc capacitor voltages of the hybrid MMCC. Fig. 5(c) shows the inner capacitor voltages of the five-level flying capacitor voltages. The zero-sequence voltage (v_S^0) for maintaining sub-module dc capacitor voltages are shown in Fig. 5(d).

From Fig. 5(a) the STATCOM currents increases from 24A to 28A during the transition from balanced to unbalanced voltage condition. The current injected to the grid from the hybrid MMCC STATCOM is balanced because the negative sequence currents are kept to be zero. Both sub-modules and two-level converter dc capacitor voltages are maintained at their nominal values as shown in Fig 5(b). Likewise, the inner flying capacitors of the sub-module five-level flying capacitor converters are also maintained within their nominal values as seen in Fig. 5(c). The zero-sequence voltage during the 30% phase ***a*** unbalance voltage sag condition increases from 0 to 60V which aids the inter-cluster dc capacitor voltage balancing.

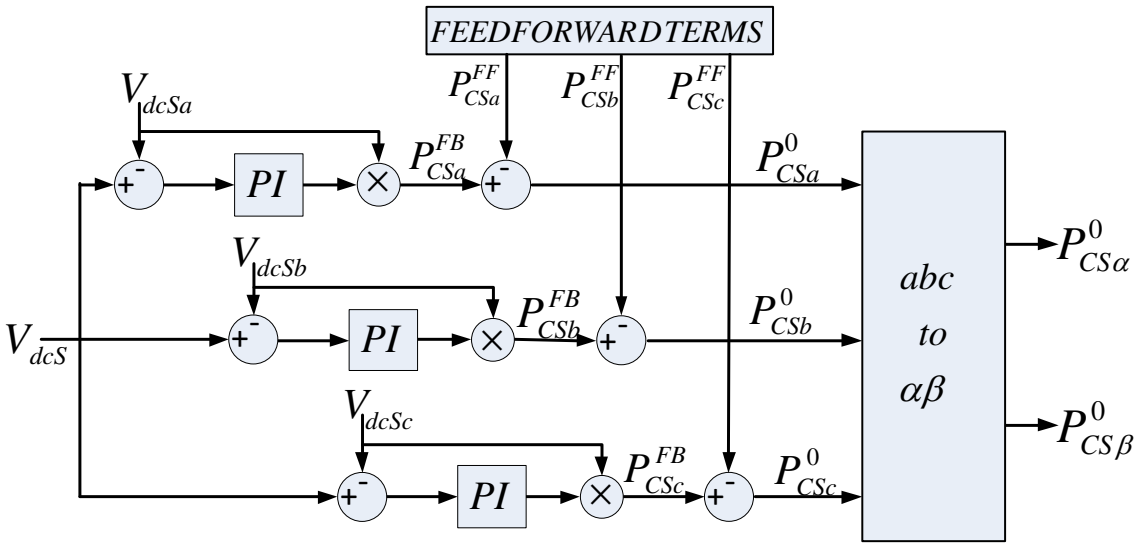

Fig. 4: Inter-cluster power balancing control

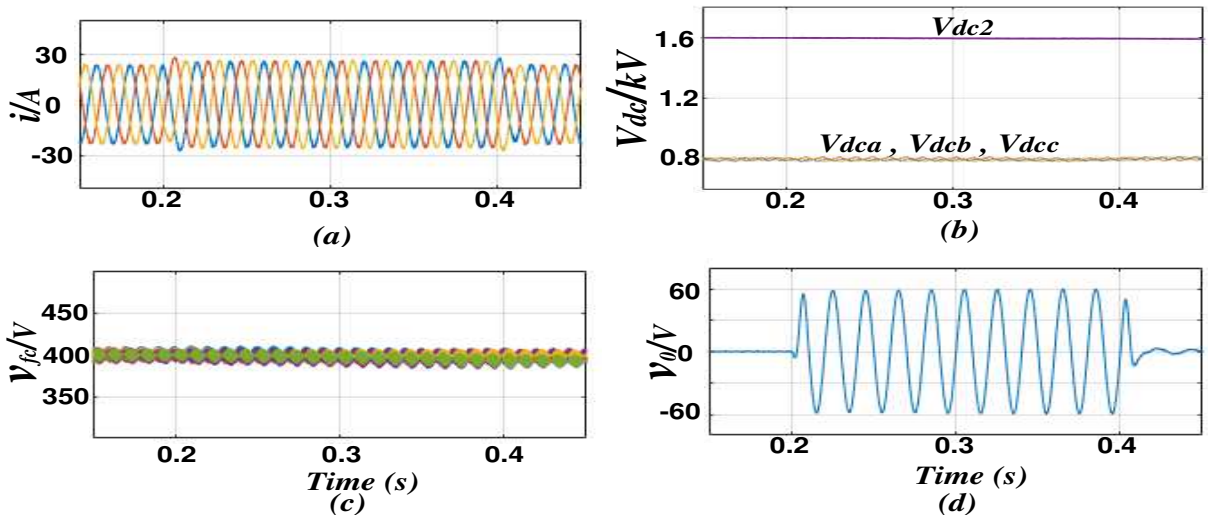

Fig. 5: Simulation results of Hybrid-MMCC STATCOM; (a) STATCOM phase currents (b) Capacitor voltages, (c) inner flying capacitor voltages and (d) Zero sequence voltage.

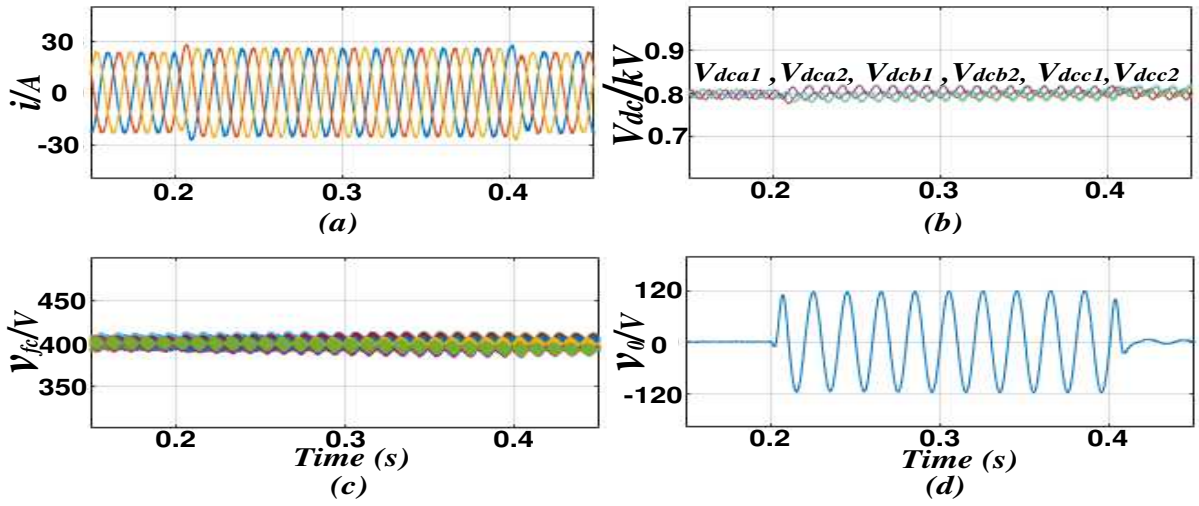

Fig. 6: Simulation results of SSBC-MMCC STATCOM; (a) STATCOM phase currents (b) Capacitor voltages, (c) inner flying capacitor voltages and (d) Zero sequence voltage.

To compare between SSBC-MMCC and hybrid MMCC, *k=2* sub-modules are connected per phase. The system parameters of the hybrid MMCC are applied for the SSBC MMCC. The SSBC is tested under 30% phase a voltage sag. The SSBC-

MMCC STATCOM also injects the same current to the grid as highlighted in Fig. 6(a). Comparing the dc capacitor voltages of the SSBC to the hybrid STATCOM, the hybrid has two capacitors fewer than the SSBC. Also, the voltage variation of the SSBC is ±4% which is higher than the hybrid capacitor voltage variation of ±2.5%. The dc capacitor fluctuations for both configurations are still within the acceptable ±10% tolerance. Fig. 6(d) shows that the zero-sequence voltage magnitude that maintains the sub-module capacitor voltages of the MMCC is $V_0 = 120V$ compared to the $60V$ required by the hybrid counterpart. This test highlights the voltage requirement benefit of using the hybrid MMCC over SSBC-MMCC under unbalance grid voltage application.

7. Conclusion

This paper presents a control scheme in using the hybrid MMCC for grid applications particularly under unbalance voltage condition. This scheme is capable of providing the dc voltage balancing of both the sub-modules and 2-level H-bridge altogether even during grid faults without disturbing the STATCOM operation. The hybrid MMCC is further compared with single star connected MMCC under grid voltage unbalance condition. This analysis highlights the voltage requirement superiority of the hybrid MMCC over the star-connected MMCC. The simulation results are shown, and they validate the effectiveness of the hybrid MMCC for unbalanced voltage condition.

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