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Jiang, S., Lee, K.B. orcid.org/0000-0002-5374-2767, Pinchbeck, J. et al. (2 more authors) (2020) A 624 V 5 A all-GaN integrated cascode for power-switching applications. physica status solidi (a), 217 (7). 1900783. ISSN 1862-6300

https://doi.org/10.1002/pssa.201900783

This is the peer reviewed version of the following article: Jiang, S., Lee, K.B., Pinchbeck, J., Yin, Y. and Houston, P.A. (2020), A 624 V 5 A All-GaN Integrated Cascode for Power-Switching Applications. Phys. Status Solidi A, 217: 1900783, which has been published in final form at https://doi.org/10.1002/pssa.201900783. This article may be used for noncommercial purposes in accordance with Wiley Terms and Conditions for Use of Self-Archived Versions.

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624 V 5 A All-GaN Integrated Cascode for Power Switching Applications

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Keywords: power electronics, semiconductor devices, semiconductor switches, semiconductor heterojunctions

Abstract— An all-GaN integrated cascode device with an output current of 5 A, threshold voltage of +0.65 V and breakdown voltage of 624 V is demonstrated. Compared to the commercial 600 V hybrid GaN plus Si cascode device (TPH3202), the integrated cascode exhibits a significantly reduced delay time when switched at 200 V and 2.7 A. This is attributed to the absence of a Si MOSFET driver, leading to a much smaller input capacitance as indicated by the high voltage capacitance measurements. In addition, the integrated cascode device shows a reduced ringing effect due to monolithic integration. When compared to commercial 600 V standalone GaN devices (GS66502B and GS-065-004), a reduced Miller effect is observed for the integrated cascode when switched under low gate driving current conditions. The results demonstrate the advantages of the cascode device to switch with low gate driving current using cheaper, faster and more efficient gate drivers.

1. Introduction

The realisation of the concept of the cascode configuration for GaN power devices was first introduced in 2013 and subsequent release of the first commercially available hybrid GaN plus Si cascode power transistor.^[1] Since then, the hybrid cascode has attracted great attention and has become one of the most successful topologies to realise true enhancement-mode (E-mode) operation for GaN lateral power devices.^[2-8] In addition, the reduced Miller effect originating from the nature of the cascode configuration has enabled the hybrid cascode to achieve faster switching speed and lower switching losses compared to state-of-the-art Si MOSFETs [8-10]. With the advancement of E-mode technologies,^[11-23] commercial GaN standalone E-mode devices are now available.^[11] However, there are significant drawbacks in the Si-based hybrid cascode device due to parasitic inductance and the requirement to have a large Si device to maintain current capability comparable to the GaN component. These reduce the speed advantage of the hybrid cascode when compared to the GaN standalone device.

In our previous study, we reported an all-GaN integrated cascode by replacing the Si MOSFET with a low voltage GaN E-mode device.^[24] We have exploited the speed advantage in the cascode structure and demonstrated a 33% faster switching speed for the integrated cascode compared to its equivalent standalone GaN E-mode device at 200V. However, direct comparison with commercial 600 V GaN power devices has not been presented. This comparison could potentially clarify the advantages of the integrated all-GaN cascode configuration. In this study, we demonstrate a 5 A all-GaN integrated cascode device with a breakdown voltage of 624 V and compare its switching performance to similarly rated commercial 600 V GaN devices including Transphorm's hybrid GaN plus Si (TPH3202) and GaNsystems' standalone E-mode devices (GS66502B) and (GS-065-004).

2. Device Fabrication

Figure 1 shows the schematic of the all-GaN integrated cascode device by monolithic integration of a low voltage GaN E-mode part and a high voltage GaN D-mode part. Devices were fabricated using a similar fabrication procedure as described in the previous study,^[24] on a 6 inch Si substrate. Cl₂ based inductively coupled etching was used to form mesa isolation. After that, a metal stack of Ti/Al/Ni/Au was deposited by thermal evaporation and annealed at 775 °C for 1 min to form ohmic contacts for the source and drain electrodes. A CHF₃ based fluorine-based treatment in a reactive ion etching system was used to achieve the E-mode operation.^[13,24] A nominally 20 nm of SiNx was then deposited using plasma-enhanced chemical vapour deposition to form metal-insulator-semiconductor (MIS) structures for both the E-mode and D-mode gates. The cascode device benefits from optimising the threshold voltage of the MIS D-mode part to give improved current handling as discussed previously.^[24] The device was then passivated with 50 nm of SiN_x to support the gate-connected field plate (GFP) before the deposition of Ni/Au metal stack to form the T-shaped gate electrode for both the D-mode and E-mode parts. A second passivation of 200 nm SiNx was then deposited before the final step of field plate (FP) and bond pad formation. The fabricated device features a gate width of 32 mm, gate length of 1.5 µm for both E-mode and D-mode gates, an E-mode source drain separation of 6.5 μ m, an internode ohmic contact of 10 μ m (for voltage monitoring) and a D-mode source drain separation of 16 µm. Both E-mode and D-mode parts have a GFP extension of 1 µm, while only the D-mode part has an additional FP extension of 2 µm connected to the internode pad of the cascode, as similarly adopted in our previous work.^[25]

3. Results and Discussion

The fabricated device was wire bonded to a commercial QFN package for electrical characterisation. **Figure 2(a)** shows the gate transfer characteristic of the 32 mm cascode device. V_{DS} is kept the same as V_{GS} , during the sweep of V_{GS} from 0 V to 2.4 V. A positive threshold voltage of +0.65 V, defined at $I_{DS} = 1$ mA and $V_{DS} = V_{GS}$, was obtained. An output

current close to 5 A was achieved at $V_{GS} = +6$ V and $V_{DS} = 6$ V with an on-state resistance of 0.75 ohm, as shown in the pulsed I-V characteristic in **Figure 2(b)**. The device exhibits a breakdown voltage of 624 V with a leakage current below 10 μ A/mm, as shown in **Figure 2(c)**. Note that the integrated cascode devices were designed for 600 V-class with higher breakdown voltages, as shown in the breakdown characteristics of a reference device with gate width of 100 μ m with same field plate designs and geometries, where no breakdown is observed up to 1000 V. The lower breakdown voltage measured on the 32mm cascode devices is caused by source leakage current. This is possibly due to leakage via GaN buffer as a result of epitaxial growth non-uniformity across the GaN wafer which affects the large area devices and it is subject to further investigation.

A standard double pulse tester (DPT) was used to compare the switching behaviour between the 32 mm cascode device, the commercial GaN + Si hybrid cascode (TPH3202) and the commercial GaN standalone E-mode devices (GS66502B and GS-065-004). From the datasheets provided by the suppliers, TPH3202 is rated at 600 V, 9 A with Ron of 0.29 ohm (TO-220 package), while GS66502B and GS-065-004 are rated at 600 V, 7.5 A with Ron of 0.2 ohm (GaNPX® Bottom-Side Cooled package) and 600 V, 3.5 A with Ron of 0.5 ohm (PDFN package), respectively. The relevant specifications for all devices are summarised in Table 1. The design of the DPT was similar to that described in our previous work,^[25] but with enhanced load current capability. Figure 3(a) shows the schematic diagram of the DPT. A 470 uH, 7 A choke inductor and a 600 V freewheeling diode were used as the inductive load. A 0.5 ohm current sensing resistor (R_{SENSE}) T&M SDN-414-05 was connected to the source of the device under test (DUT). The drain current (I_{DS}) was monitored by measuring the voltage drop across R_{SENSE}, via a Rigol DS6104 digital oscilloscope. The gate voltage (V_{GS}) and drain voltage (V_{DS}) were also measured. Figure 3(b) shows the assembled PCB of the DPT. The gate driver circuitry was fabricated on a separate PCB and stacked above the DUT, as shown in Figure 3(c). This design reduces the physical distance between the components and therefore minimizes the parasitic inductance in both the gate loop and the power loop as highlighted in Figure 3(b). All devices were driven by a commercial gate driver IX2204 with 10 V swing from $V_{GS} = -4$ V to +6 V. An external resistor was used to control the switching speed.

For the comparison, the test conditions for all devices are kept as close as possible. However, as each commercial device has different packaging, it is difficult to achieve identical test conditions. Moreover, despite the fact that devices are similarly rated, the differences in e.g. maximum current can still influence the comparison of the switching speed, even under the same nominal conditions. Nonetheless, the switching comparison in this study can be used to qualitatively demonstrate the potential advantages in the integrated cascode devices.

Figure 4(a) shows the waveforms of V_{GS} , V_{DS} and I_{DS} during the full cycle of double pulse measurement for the integrated cascode at a drain voltage of 200 V, load current of 2.7 A and gate resistance of 100 ohm. The first pulse of V_{GS} builds up the load current to the desired value (2.7 A), and the turn-off transient is measured at the end of the first pulse. The turn-on is measured at the beginning of the second pulse. To illustrate the advantage of the cascode,^[24] only the turn-off transient, where the advantages are greatest, was studied in detail. Figure 4(b) and (c) compares the turn-off switching performance between our integrated cascode with the commercial hybrid cascode device. A significant delay time of 60 ns was observed for the hybrid cascode before the drain voltage starts to increase, which can effectively limit the maximum switching frequency of the device. Note that the current handling of TPH3202 is larger than the integrated cascode as listed in Table 1, as a result, the intrinsic capacitance should be larger in TPH3202 which can influence the switching performance. However, it is still reasonable to believe that this significant delay is mainly attributed to the use of the Si device as the low voltage E-mode part, which introduces considerably larger input capacitance compared to the GaN E-mode part in the integrated cascode device. In addition, the integrated cascode exhibits a reduced 'ringing' effect compared to the hybrid cascode with the same assembly, which we attribute to the monolithic integration.

To compare the integrated cascode with the commercial GaN standalone devices, gate resistance of 270 ohm was used in order to observe the Miller-effect in the commercial devices. **Figure 5** shows the turn-off transients for the integrated cascode, GS66502B, and GS-065-004, respectively. A clear sign of the Miller effect controlling the switching speed can be observed for both commercial standalone devices, as indicated by the slope changes in the drain voltage in Figure 5(b) and Figure 5(c). This can effectively degrade the switching performance of the devices, leading to an increased switching energy loss. Compared to GS66502B, GS-065-004 shows a reduced Miller effect, attributable to smaller Miller capacitance (C_{GD}). On the other hand, a much reduced Miller effect is observed for our integrated cascode under the same gate drive condition, owing to the nature of the cascode configuration.^[24] These results indicate that the cascode device can switch with low gate driving current using cheaper, faster and more efficient gate drivers.

To further explain the switching behaviour observed in Figure 4 and Figure 5, a high voltage capacitance measurement was conducted for all devices. The input capacitance (C_{iss}) and reverse capacitance (C_{rss}) were measured by an Agilent 4284A LCR meter. A separate DC power supply was used to bias the device up to 200 V via a bias-tee. C_{iss} was measured up to 30 V as it is less dependent on the drain bias. **Figure 6(a)** shows comparisons of C_{iss} for all devices. The hybrid cascode shows the largest C_{iss} mainly due to the incorporated Si MOSFET, which is the main reason for the significant delay observed in Figure 4(c). On the other hand, the integrated cascode and the GaN standalone device exhibit much smaller C_{iss} , exploiting the advantage of GaN transistors. It is noted that the cascode device has a similar input capacitance as GS66502B despite lower drain current and a higher input capacitance than GS-065-004 with similar drain current in Figure 6(a). This is likely due to different designs in the gate on the source-side which results in different gate-source capacitance and/or different drain current density between the cascode device and GaNsystems devices.

 C_{rss} (C_{GD}) was measured up to 200 V and the results are shown in Figure 6(b). Both the integrated and hybrid cascode devices show a step drop in C_{rss} at around 10 V, which corresponds to the threshold votlage of the D-mode gate in the cascode. This is due to the pinchoff of the D-mode channel, after which the effective Miller capacitance (C_{GD} of the E-mode part) is shielded from the drain voltage. The charging current of the effective Miller capacitance is therefore, bypassed to the source of the cascode (ground), independent from the gate loop.^[24] This behaviour is a signature of the cascode configuration and reflects the advantage of the reduced Miller-effect.^[24] As a result, no sign of the Miller effect controlling the switching speed is observed for the integrated cascode device as shown in Figure 5(a), even with very low gate driving current, despite a larger C_{rss} compared to the commerical standalone devices (GS66502B and GS-065-004). In contrast, such behaviour is not observed for the standalone devices where C_{rss} gradually decreases and the shape of the curve is determined by the depletion, and subsequent pinch-off of the 2DEG channel under field-plate. The transients due to C_{rss} in GS66502B and GS-065-004 also explain well the Miller effect observed in Figure 5(b) and (c). The slope of the drain voltage (GS66502B and GS-065-004) increases gradually at the beginning of the V_{DS} transient ($V_{DS} < 50$ V), which corresponds to a gradual change in C_{rss} of the devices when the bias is below 50 V. At V_{DS} of 50 V, as shown in Figure 6(b), C_{rss} of both commercial standalone devices reduce significantly due to the pinch-off of 2DEG channel under the field plate. As a result, the drain voltage slope (GS66502B and GS-065-004) recovers and the Miller effect has little influence on the switching speed afterwords, as highlighted in Figure 5(b) and (c).

4. Conclusion

We demonstrated a high current high voltage (5 A and 624 V) all-GaN integrated cascode device for power switching applications. The switching performance is qualitatively compared to the state-of-art 600 V GaN commercial transistors. The integrated cascode exhibits less 'ringing' and significantly improved delay time compared to the hybrid cascode (TPH3202)

due to monolithic integration and the elimination of the Si MOSFET with much higher input capacitance. Compared to the commercial standalone devices (GS66502B and GS-065-004), a much reduced Miller effect is observed for the integrated cascode, resulted from the nature of the cascode configuration with its effective Miller capacitance shielded from the high drain voltage. These results suggest potential advantages of conventional GaN devices when incorporated into the cascode configuration, allowing them to operate at low gate driving conditions with improved switching speed and energy efficiency.

Acknowledgements

The authors acknowledge financial support from the UK Engineering and Physical Sciences Research Council (EPSRC) under projects EP/K014471/1 and EP/N015878/1.

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Figure 1. A schematic diagram of the 32 mm integrated cascode device.



Figure 2. (a) Gate transfer characteristics of the 32 mm cascode device with V_{GS} swept from 0 V to 2.4 V and $V_{DS} = V_{GS}$, and threshold voltage is define at $I_{DS} = 1$ mA and $V_{DS} = V_{GS}$, (b) Pulsed I-V characteristics of the 32 mm cascode device, with pulse width of 1 ms and duty cycle of 0.01 and (c) breakdown voltage results of the 32 mm cascode and 100 µm cascode (reference device) with device pinched off at $V_{GS} = -4$ V.



Figure 3. (a) A circuit diagram of the DPT used for switching measurements, (b) assembled PCBs of the DPT and (c) highlighted picture of DUT soldered underneath a separate gate driver board, to minimize the physical distance between components.



Figure 4. Switching waveforms of V_{GS}, V_{DS} and I_{DS} for (**a**) 32 mm cascode during a full cycle of double pulse measurement, (**b**) 32 mm cascode during turn-off transition and (**c**) hybrid cascode (TPH3202) during turn-off transition at $V_{DS} = 200$ V $I_{DS} = 2.7$ A and $R_G = 100$ ohm, captured at 5 V/div, 50 V/div and 50 mV/div, respectively.



Figure 5. Switching waveforms of V_{GS} , V_{DS} and I_{DS} during turn-off transition for (a) 32 mm cascode and commercial standalone device (b) GS66502B and (c) GS-065-004 at $V_{DS} = 200$ V $I_{DS} = 2.7$ A and $R_G = 270$ ohm, captured at 5 V/div, 50 V/div and 50 mV/div, respectively.



Figure 6. Comparison of (a) C_{iss} and (b) C_{rss} between Sheffield cascode device, TPH3202, GS66502B and GS-065-004.

Table 1. Summary of relevant device specifications for Sheffield cascode, TPH3202,GS66502B and GS-065-004.

	Sheffield	GS-065-004	TPH3202	GS66502B
	Cascode			
V _{br}	624 V	600 V-class*	600 V-class*	600 V-class*
$I_{DS}(DC)$	-	3.5 A*	9 A*	7.5 A*
IDS	5 A (pulse	6 A (pulse	35 A (pulse	18 A (pulse
(pulsed)	width 1 ms)	width 1 ms)	width 10 µs)*	width 100
				μs)*
Ron	0.75 ohm	0.55 ohm	0.29 ohm*	0.2 ohm*

*data provided from suppliers from device datasheets.